Time intervals measurements and generation methods review

Pablo Alvarez CERN AB/CO

Time interval measurement
Phase measurement
Delay generation
Phase generation

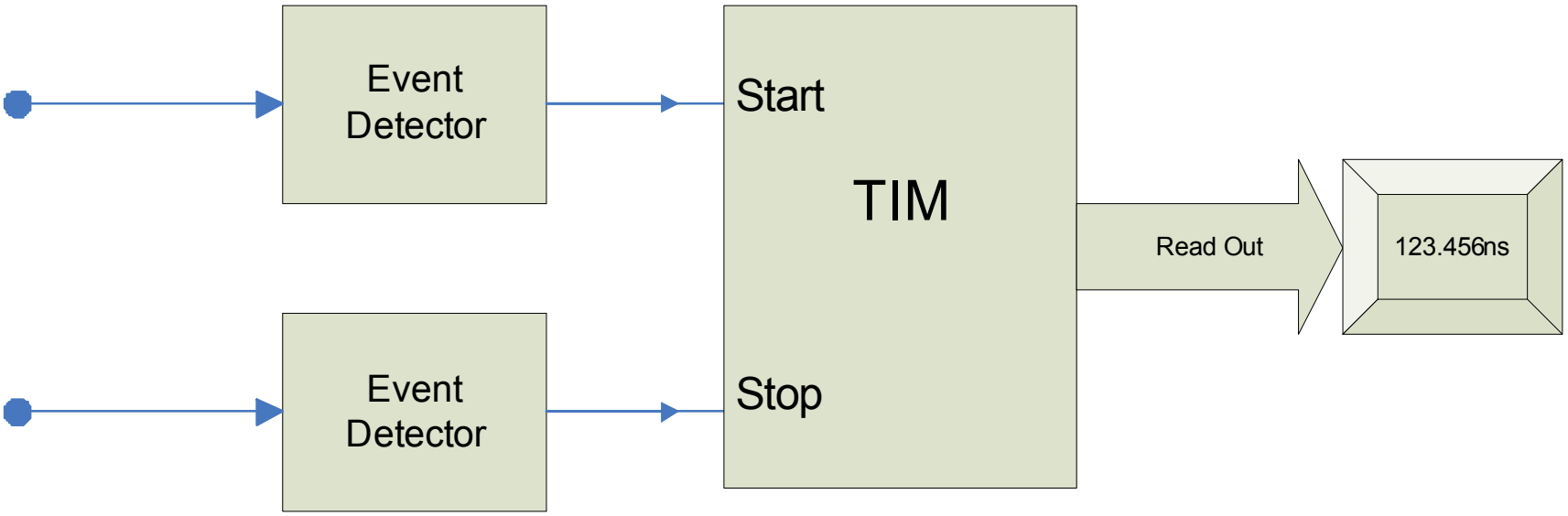
- Time interval measurement ←
- Phase measurement
- Delay generation
- Phase generation

Time Interval Measurements Techniques

1. Specifications
2. Course counting
3. Fine time interval measurement
4. Interpolation
5. Calibration

Based on “Review of methods for time interval measurements with picosecond resolution” Josef Kalisz, Metrologia 41 (2004) 17-32

Principles

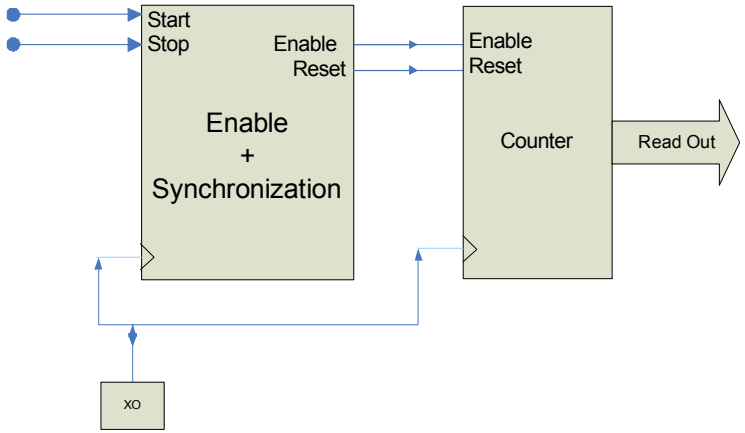

Event
Detector
Event
Detector
Start
TIM
Stop
Read Out
123.456ns

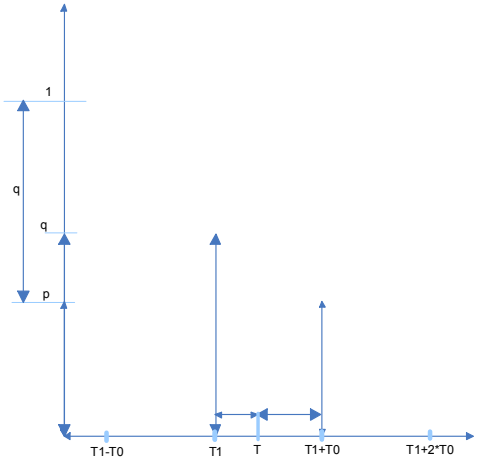
Specifications

- Measurement range (MR)
- Standard measurement uncertainty or random error or precision (s)
- Non linearity. Differential (DNL) and integral (INL)
- Quantization step (q)
- Dead time (Td) or the shortest TI between the end of a measurement and the start of then next one.
- Read out speed
- Stability

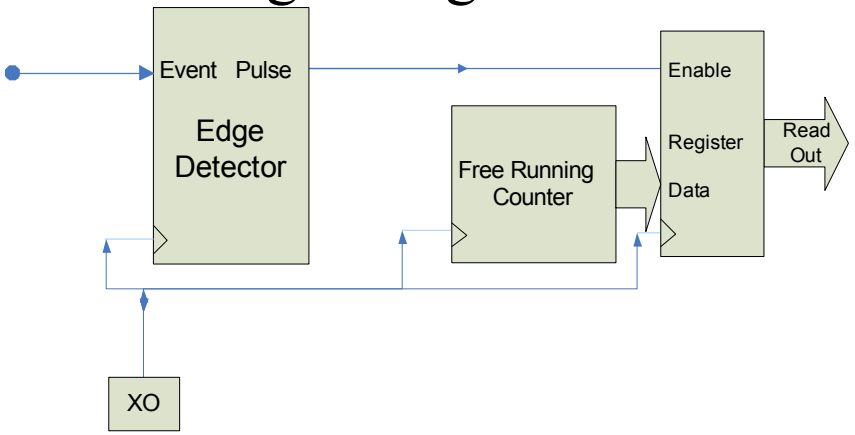
Coarse counting

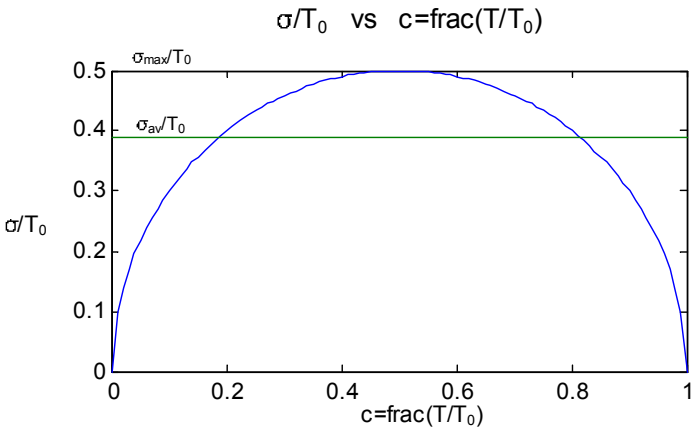
Time interval configuration





Time tag configuration





Fine analogue TIM 1

- TI stretching + counter
- Time to amplitude + ADC
  - Charge capacitor
- Periodic function sampling
- Vernier method with 2 startable oscillators
- Tapped delay line

TI streching

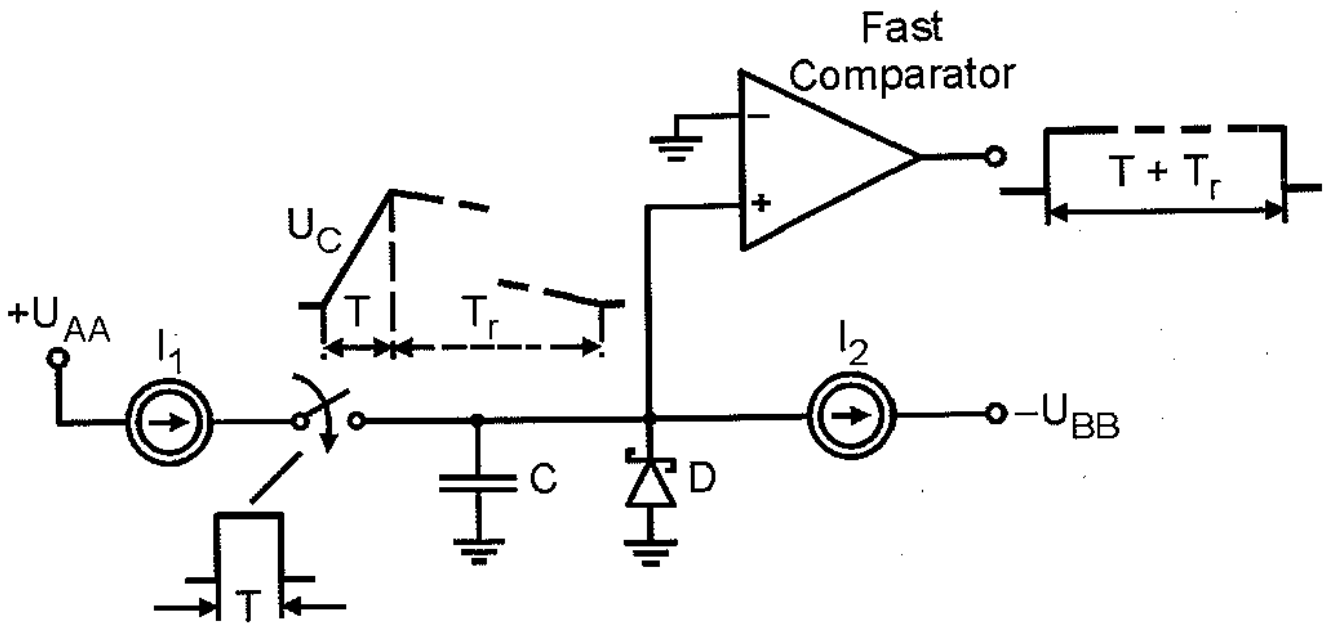


Figure 4. Linear stretching of the measured time interval T for subsequent counting.

TI to amplitude

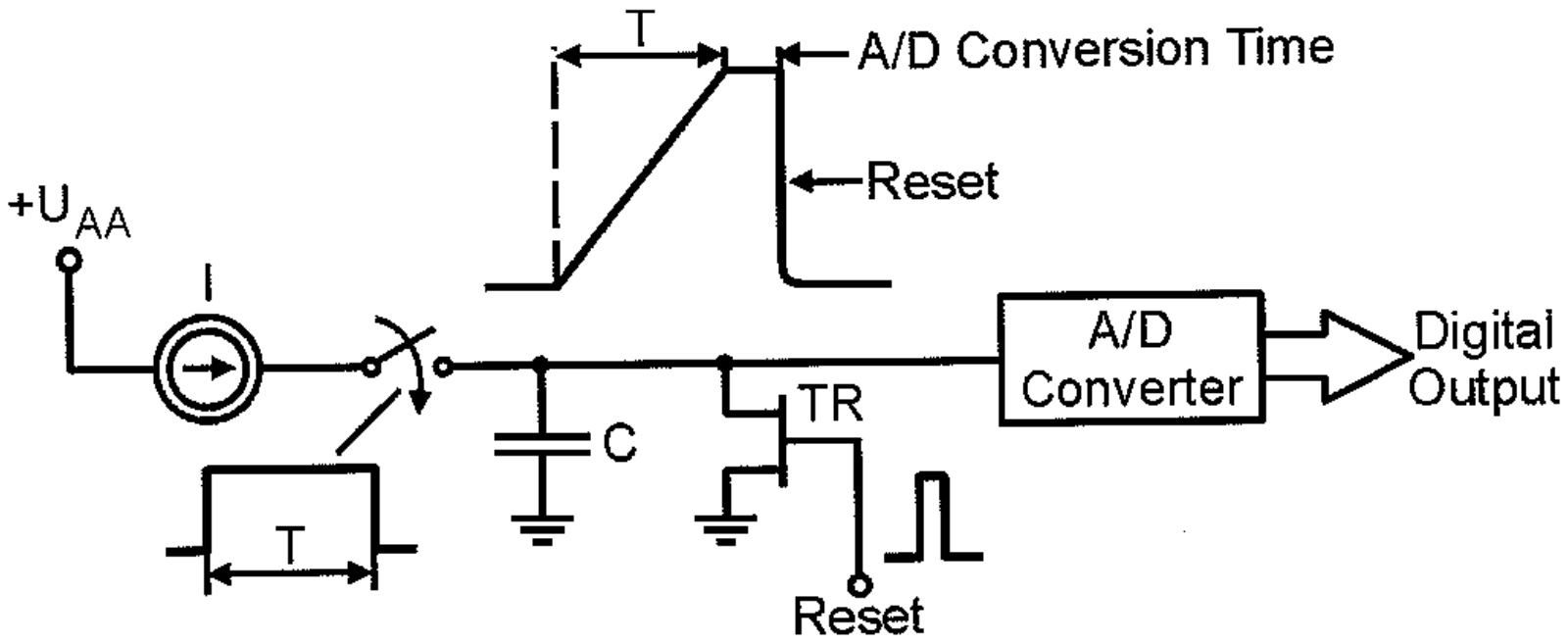


Figure 5. Conversion of TI to amplitude followed by a typical A/D conversion.

Periodic function sampling

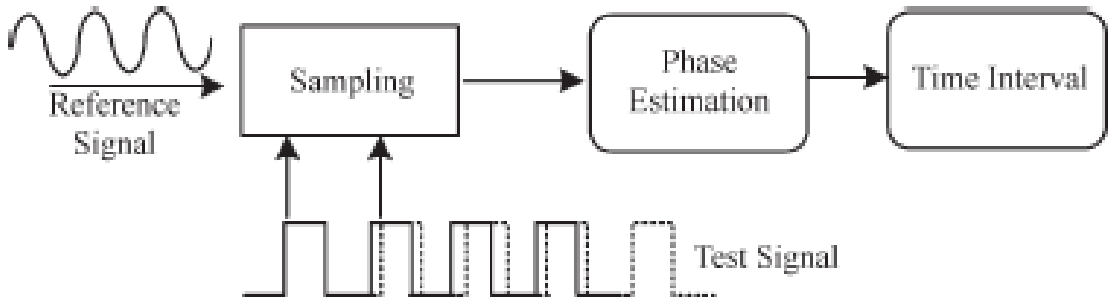


Fig. 1. High accurate time interval measurement block diagram.

Tapped delay line

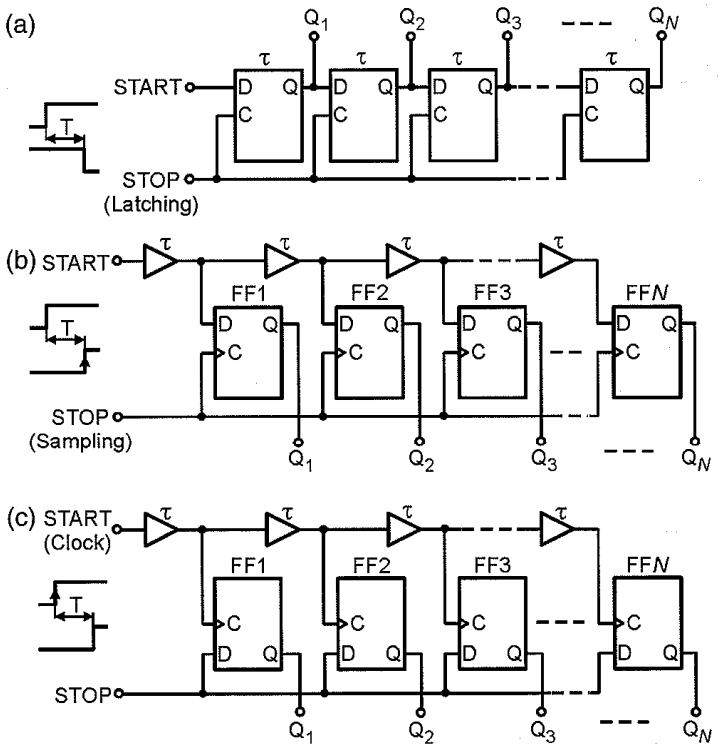


Figure 7. TDC utilizing the tapped delay line: (*a*) line comprising latches, (*b*) line comprising buffers with simultaneous sampling of its state, (*c*) line comprising buffers with successive sampling of the state of the STOP input.

CERN HPTDC
Low resolution: 32 channels with 100ps resolution
High resolution: 8 channels with 25ps resolution

Comercial TDC-GPX offers 10ps

Some designs in FPGAs have reached a precision of 200ps. See "Field Programmable Gate Array based time to digital converter with 200-ps resolution" Kalisz J et al, 1997

50-60 ps on a XC4VSX35 FPGA
Upgrading of Integration of Time to Digit Converter on a Single FPGA
Young ZHANG1,2, Peicheng HUANG1 and Renjie ZHU1,2
Abstract-A Time to Digit Converter (TDC), which can achieve resolution 50-60 picoseconds, is integrated on a single FPGA. Implementation a TDC on FPGA provides not only higher precision and shorter dead time compared to traditional methods….

Nutt interpolation method

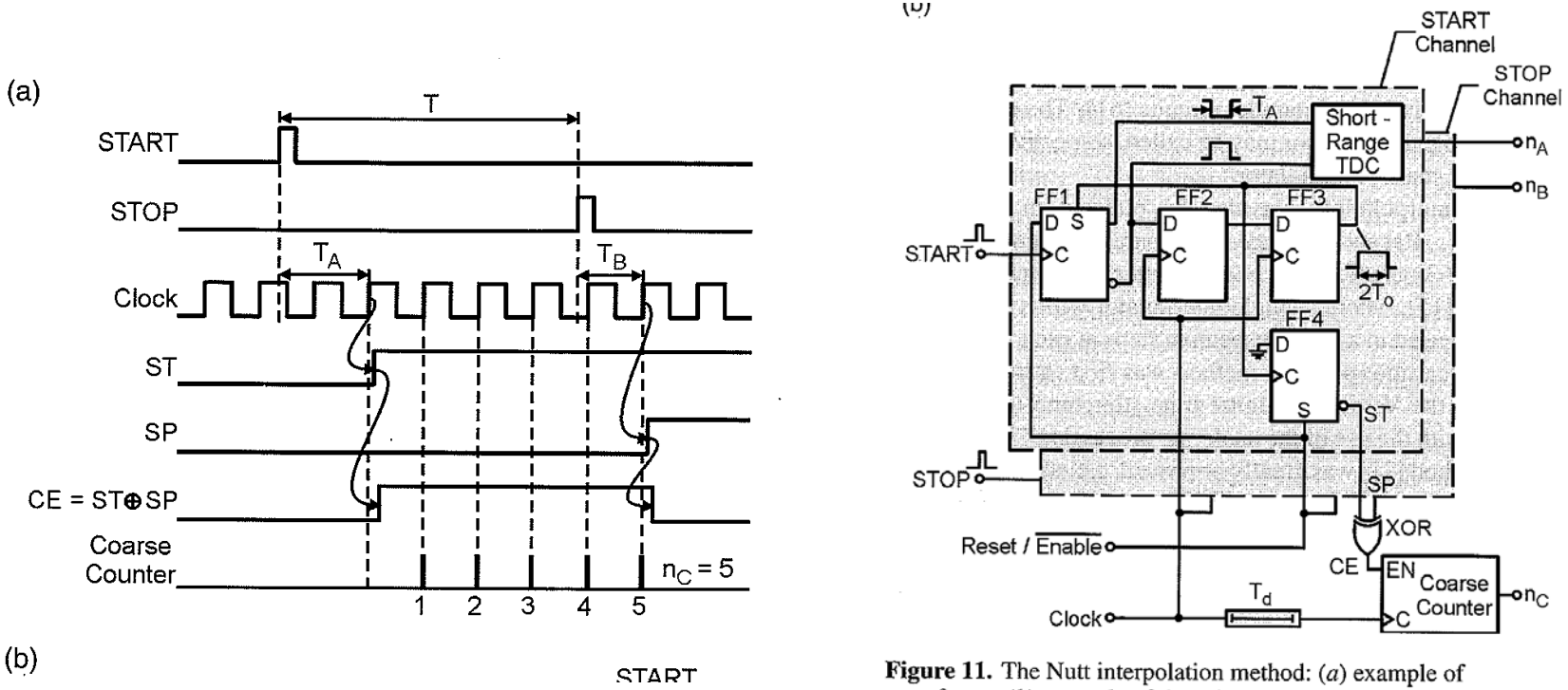


Figure 11. The Nutt interpolation method: (*a*) example of waveforms, (*b*) example of the relevant circuit diagram.

Calibration

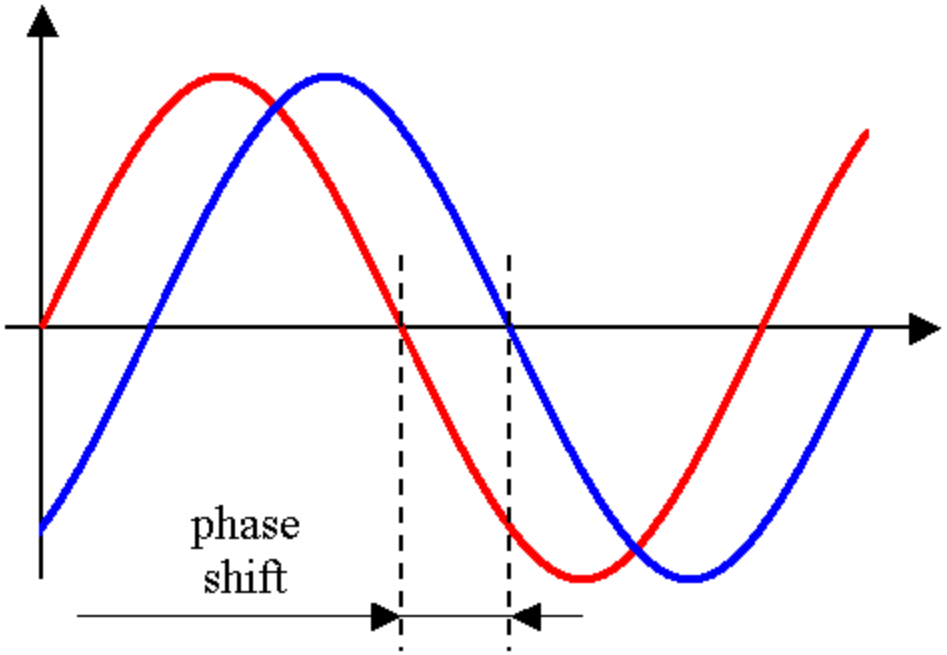
- Non linearity is measured with a “statistical code density test”
  - A random oscillator generates events that should be evenly distributed along the different TIM codes. The frequency of a code is proportional to the code size.
- Offset error is measured shortening the Start and Stop inputs

- Time interval measurement
- Phase measurement ←
- Delay generation
- Phase generation

Phase Measurement

- Principles
- Specifications
- Direct Measurements
- Feedback Based Measurements
- Calibration

Principles



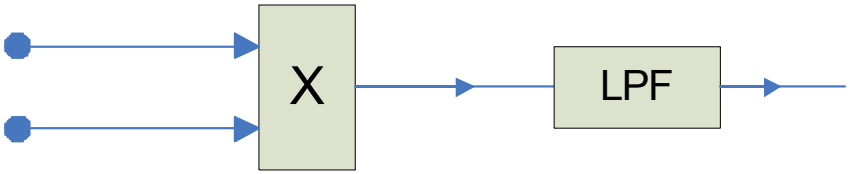
- Sinusoidal signals →$Y=A*\sin(2\pi f \cdot t-\varphi)$
- Any periodic signal →$\varphi= 2\pi\ tc/T$
  - tc: time between equal level crossings
  - T: period

Specifications

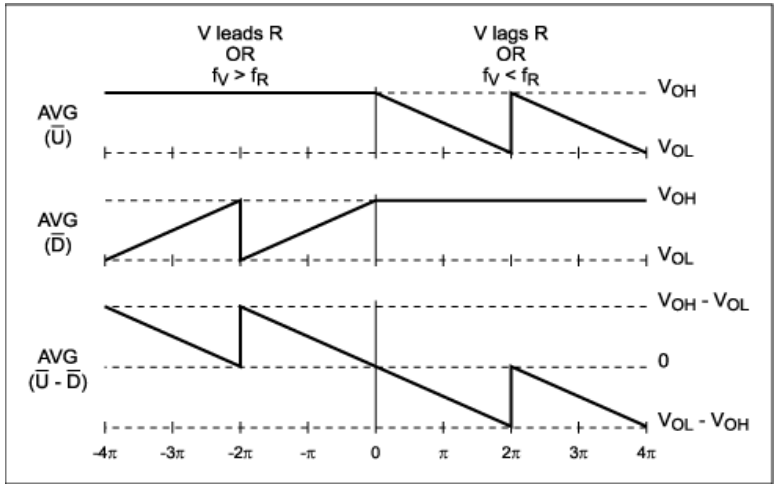
- Transfer Gain (V/rad)
- Maximum frequency
- Phase offset
- Added random jitter
- Cycle−to−Cycle jitter
- Stability (sometimes an Allan deviation plot of the two inputs wired to the same reference)

Classical PHDs

Multiplier $V=K*\sin(\Phi)$



Phase frequency detector



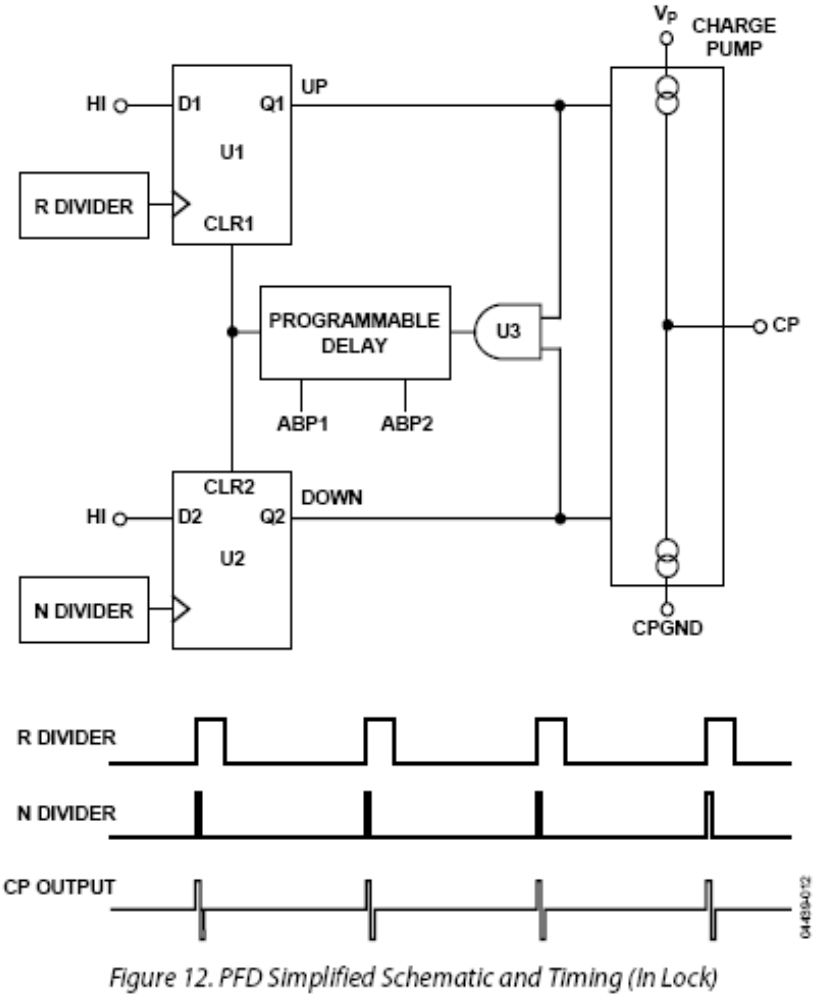


Figure 12. PFD Simplified Schematic and Timing (In Lock)

Dual Mixer Time Difference System

Y=A*sin(2π(f-fb)·t-θ)·sin(2πf·t-φ)=A/2(cos(2π(2f-fb)·t+(θ-φ))-cos(2π(fb)·t-(θ-φ))
Tshift=φ/2πf --> Tshiftb=φ/2πf b
For f=100MHz and fb=100Hz the time shift is increased by 1e6

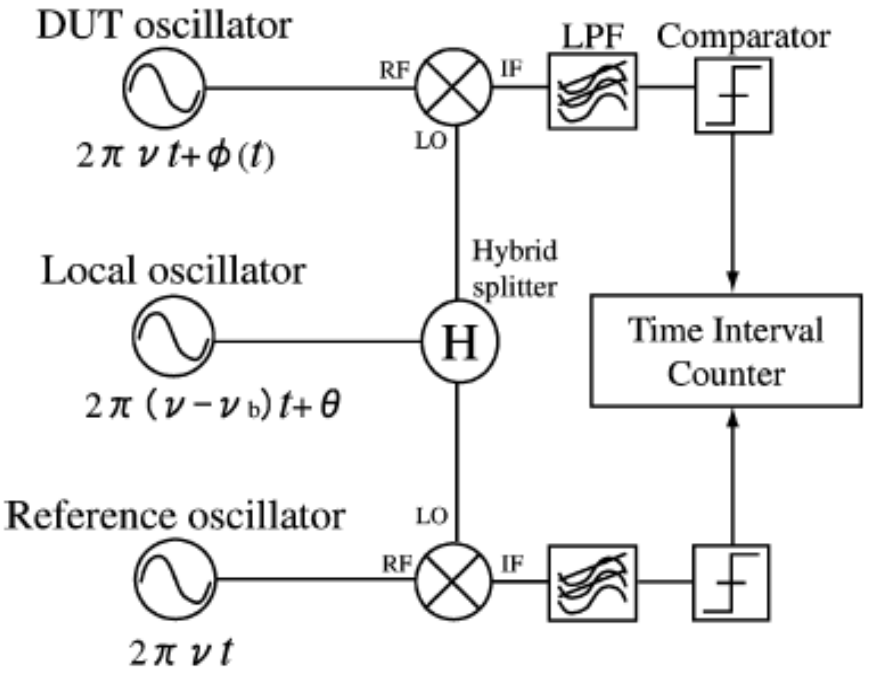


Fig. 1. Block diagram of general DMTD system.

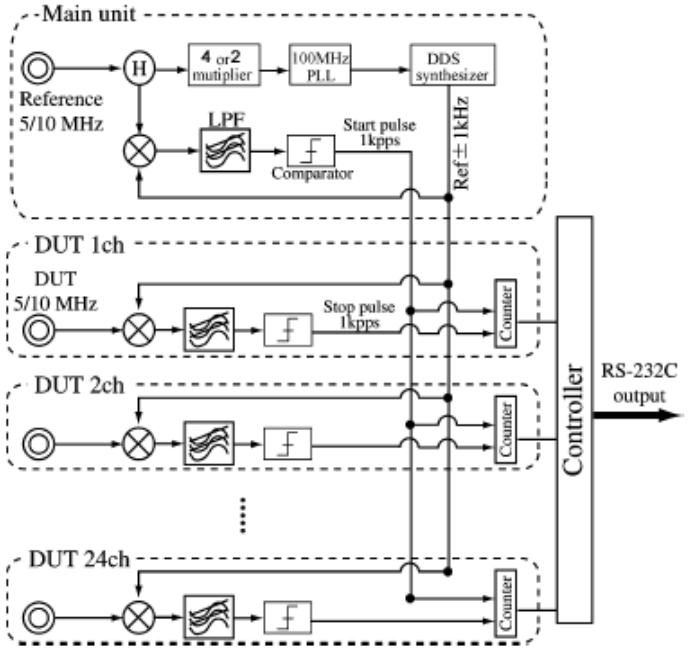


Fig. 2. Block diagram of multichannel DMTD developed in the NICT.

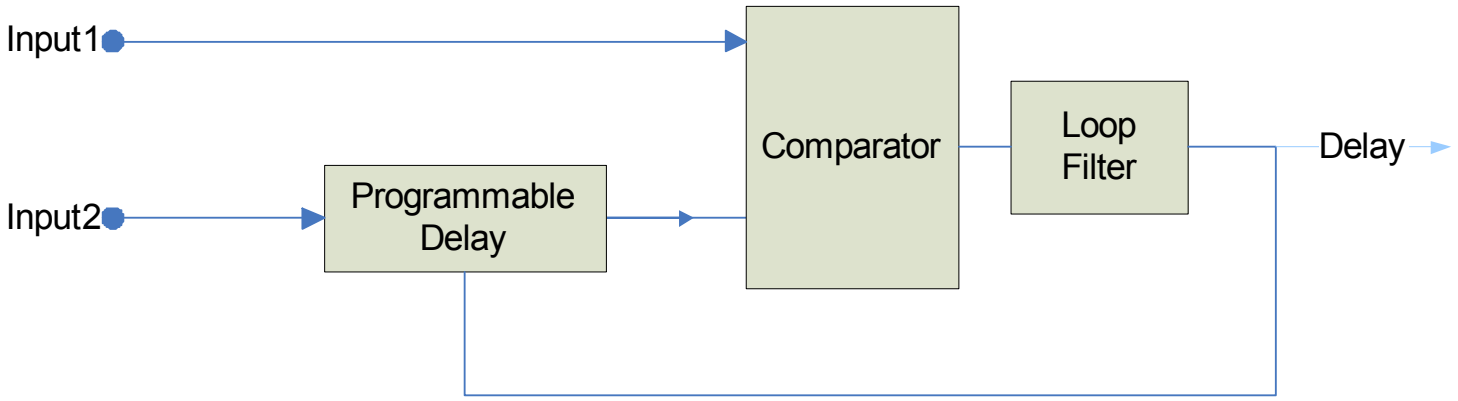
Development of Multichannel Dual-Mixer Time Difference System to Generate UTC (NICT)
Fumimaru Nakagawa, Michito Imae, Yuko Hanado, and Masanori Aida

Time interval meters

Any TIM with low dead time can do a good job

- Tapped Delay Lines. Typically used in FPGAs.
- Asynchronous free running counter. Counting at high frequencies and averaging can provide with a good phase estimate. Beware of Injection locking of the "independent" oscillator to the system clock.

Programmable delay loop



Calibration

- There is not an easy response to calibration for phase detectors
- Gain and non linearity errors can be corrected with a TIM, a fine delay generator or a better phase detector.
- Dual Mixer Time Difference Systems are per se linear. Possible problems will normally show up in Allan variance plots.

- Time interval measurement
- Phase measurement
- Delay generation←
- Phase generation

Delay generation

- Ramp + comparator
- Programmable passive delay line
- Triggered phase locked oscillator
- TIM + oscillator + Fine delay

Ramp + comparator

- A constant current source that loads a capacitor generates a voltage ramp. A comparator will trigger the output at a selected voltage.

- The voltage ramp is nowadays normally generated with a high precision DDS.

Programmable passive delay line

- Normally it is formed by a configurable capacitor and a programmable current source
- Very used in clock distribution ICs

Triggered phase locked oscillator

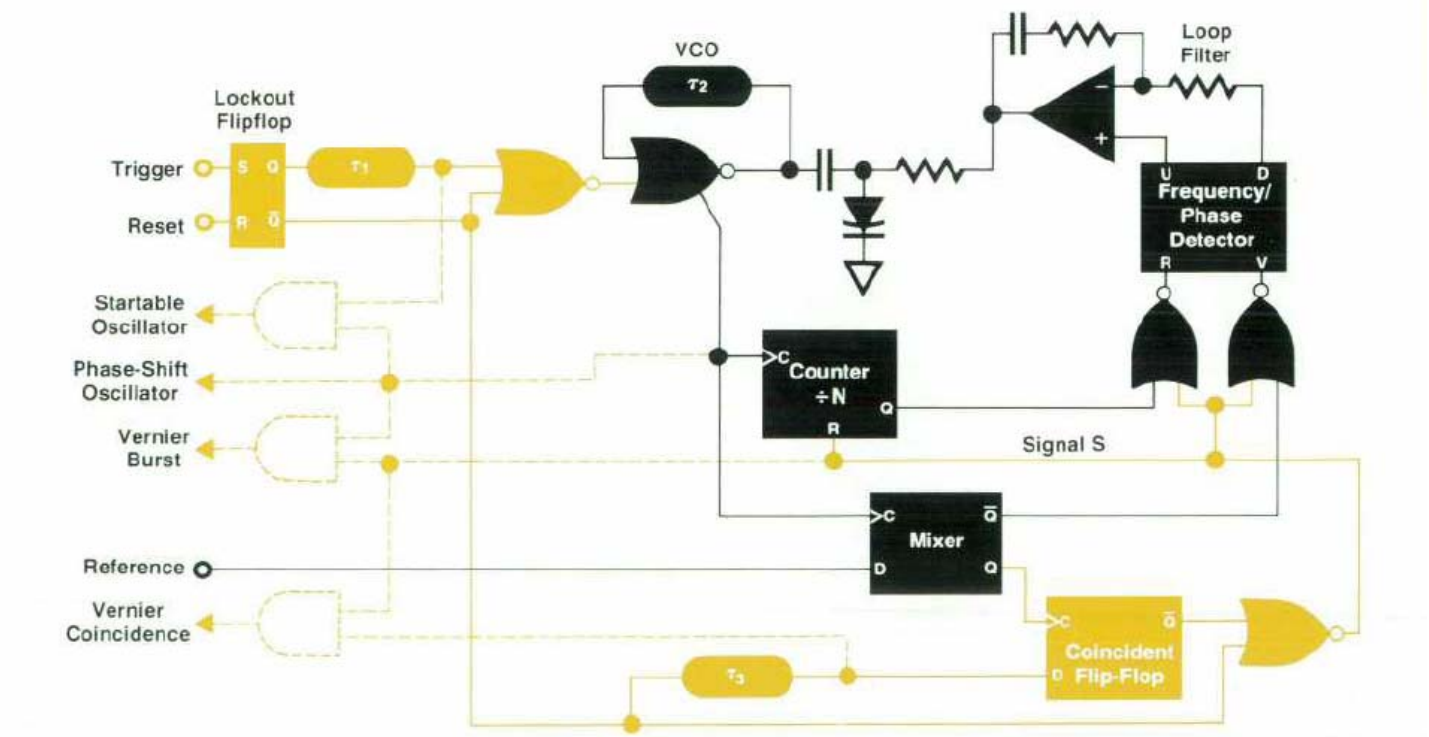


Fig. 1. *Simplified block diagram of a triggered phase-locked oscillator with interpolation factor N. The black components are active during quiescent (pre-trigger) conditions. Solid-color components become active when the oscillator is triggered. Dashed gates show how the oscillator can be configured for different applications.*

Hewlett Packard journal august 1978. David C. Chu

TIM + oscillator + Fine delay

- The incoming pulse can be time tagged respect to a local oscillator. The delay generator can calculate the corresponding output phase respect to the local oscillator and program a fine delay

- Time interval measurement
- Phase measurement
- Delay generation
- Phase generation ←

Phase generation

- Phase can be generated starting from delay generators
- Phase generation systems can also be based on a feedback from a phase measurement

Phase generation from phase measurement loop