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TEST2 = GND -> VREF = 0.765
TEST2 = V5FILT -> VREF = 0.758
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1V, 14A, 500kHz, 86%

Project/Equipment: AMC FMC Carrier v4

Power P1V0

10x 22uF 10V 1206
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DAC Vih = 2.5V and accepts 2.5V CMOS signal.
DAC output range: 0V to 2.5V
Vc 1.65V +/- 1.65V

Optional RC filter for 1-bit DAC from FPGA output. Can be used to fine tune Si571, which has a control voltage input.

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Apply to all AMC ports: see table 6-1 PICMG AMC.0 R2.0 1.5.11.2006

RXes are CARRIER-OUTPUT
TXes are CARRIER-INPUT

Carrier is a HOST

OPTIONAL AMC PORTS ROUTING TO THE LVDS - CERN timing system requirement

OPTIONAL SATA/SAS PORTS ROUTING TO THE MGT
I2C switch footprint is compatible with MAX7358 which has interesting anti-lock capabilities.

The resources are FPGA I2C and MMC I2C2, available from TCA9548s SW:

- MMC I2C1, addr 1110 A2 A1 0
- addr 1110 A2 A1 1
- where A2=P2[28], A1=P2[29]
- default addr is 0x70 and 0x71

---

I2C_MUX_ADDR[2..1]

mux address 1110 A2 A1 0 from FPGA side 0x70
mux address 1110 A2 A1 1 from CPU side 0x71

---

I2C device address map

Hereinafter are available devices: FPGA I2C and MMC I2C1 addr 1110 A2 A1 0 FPGA I2C and MMC I2C2 addr 1110 A2 A1 1

- address 0x70 FPGA I2C
- address 0x71 FPGA I2C
- address 0x70 MMC I2C1
- address 0x71 MMC I2C2

---

Temp sensors

- LM75: 0x4D
- LM75: 0x4C
- LM75: 0x4E
- LM75: 0x4F

- EUI-ID: 0x59
- EEPROM 2k: 0x50
- SRAM/RTCC reg: 0x6F
- RTC EEPROM: 0x57

- INA3221AIRGV: 0x42
- INA3221AIRGV: 0x41
- INA3221AIRGV: 0x40

- 8V54816ANLG: 0x5B

---

Power

- MUX Port 2

- MUX Port 3

- MUX Port 4

- MUX Port 5

- MUX Port 6

- MUX Port 7

- FMC1
- EEPROM 0x52
- FMC2
- EEPROM 64k: 0x51
- EEPROM 2k: 0x50