WRS Low Jitter Daughterboard Report

SEVEN SOLUTIONS
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1. Executive summary

This document summarizes the tests performed in SevenSolutions to evaluate the WRS Low Jitter Daughter board developed by Mattia Rizzi and the BE-CO-HT group at CERN. Key aspects such as performance, assembly of the board on the SCB and documentation have been evaluated and the issues related with the inclusion on the company portfolio have also been discussed.

2. Assembly procedure

In this section we present our impressions about the assembly process for the daughter board.

2.1 SCB’s modifications

The Low Jitter Daughterboard is designed as a pluggable part for the WRS’s SCB board. It takes advantage of the unused J3 connector in the SCB (unsoldered) to drive all the needed signals from the WR logic but the external clock reference. Besides soldering the J3 connector (SAMTEC QSS-025-01-L-D-A) it is also needed replacing the main XO for a U.FL connector.

Soldering modifications over the SCB are not very difficult, so it could be accomplished by people with good soldering skills and experience. It just requires a standard precise soldering iron. Instructions on the web page of the project are concrete enough and allow to perform the proposed task. It could be improved by providing a better picture for the U.FL placing.

After doing the modifications on the SCB, the daughter board is ready to be screwed into the SCB. It requires using two of the four back holes for this purpose. Due that this operation consumes two of the original fixing holes of the SCB to the backplane, the SCB assembly to the backplane will be weaker after installing the daughterboard. It should be studied if there exits some kind of “double side screws” that make possible to keep original fixation mechanism and at the same time adding the mechanical support for the daughterboard.

2.2 Additional assembly modifications

In addition to the adaptations in the SCB for plugging the daughter board, they are also needed two modifications more:

- Providing power supply to the daughter board from the main power supply.
- Drilling the front of the WRS for the external SMA connector needed in the GM mode.
The daughterboard needs an external 12V power supply. The WRS has many free pins on his main power supply connector so it can easily be obtained from there. **There are no instructions on the web page to perform this step neither a bill of materials needed.** The part name of the power supply connector should be added to the material list provided.

The Fig. 1 shows how, in Seven Solutions, we set up the power supply connection. This way would be the best: using a free pin slot and crimping the power cables. Because of no many people own a crimping tool, there’re alternative ways for getting power supply such as soldering the cables from J7 connector (power supply of the backplane), or provide the power supply connector with the daughter board cables along with the low jitter board.

The second modification is related to the external SMA connector needed to input an external 10 MHz dock for the GM mode. It is not very complicated to drill a hole for the connector in the front, but a drilling tool is needed. There’s another option: extract an SPF’s cage (it is not soldered to the PCB) and use the port hole for the SMA connector. The second option is not recommended because the connector is not fixed to the box and an accidental pulling would remove the U.FL connector from the daughter board hurting the SCB board.

Finally, the user must connect the U.FL connector from the SCB to the CLK_BUFF connector in the daughter board, the external SMA connector and place in the proper way the jumpers in the connectors W1-5. **This step is not documented at all.** Although an advanced user could guess the meaning of the W1, W2 and W3, it’s not the case for W4 and W5 and it would require some support or including this information on the existing documentation.
Note that in our assembly test, we hadn’t used the 5mm spacers. Because of that, we cannot evaluate the join strength of the two boards in a proper way although we do not foresee any mayor issue here.

In summary, the assembly process is not specially complicated but some soldering skills are needed. It’s important to remark and inform to the users that they will lose the WRS’s warranty if they perform the process by their own and it is not clear how this process can deteriorate the operation of the board. This is an issue to take into account also for manufacturing companies.

Regarding the assembly instructions, there is some missing information that we recommend to explain better. Current documentation is not well suited for most of the users who may want to accomplish these modifications on their WRSs. Our recommendation is to provide the details commented above, explaining the process in a more detailed way, with a step by step guide. Moreover, the components list should contain all the necessary elements such as the power connectors or spacers.

### 3. Usability and performance evaluation

After installing the new board the WRS should start as a standard BC using the XO of the daughter board. To take advantage of the improved GM mode, the user must replace the binaries for the FPGA and for the LM32 software.

The project’s web page provides precompiled binaries but the instructions to replace the existing binaries in the WRS are not very well detailed. For the case of the WRPC-SW a succinct line is included to do it (maybe enough for advanced users), but there are no comments about how to perform the modification of the FPGA’s binary. For the sake of completeness, some extra command line options should be provided.

![Figure 2. Phase noise results](image-url)
An important issue to remark in our tests is that **WRS needed several reboots before it gets locked to the external reference when set the GM mode.** From the support provided by Mattia Rizzi we know this is a “standard behavior”. It is normal. We’ve reproduced the same setup as depicted in the project’s web page (Experimental results section) but using an OCXO Morion MV89 as clock reference (the best one available our our lab). Our results validate the results obtained by Mattia on his tests. We have some additive noise over 20-60 Hz because we maintained the Ethernet port connected during the tests and as Mattia explained us, this could affect the system performance. A phase noise plot is included in Fig. 2 including the results we got.

As final concern, we evaluate the thermal impact of adding this board to be WRS. It was expected that the daughter addition affects the airflow and the refrigeration of the SCB, increasing the FPGA’s temperature as consequence. In our tests we’ve seen **no significant variation** between the temperature in the WRS with the Low Jitter Board and an unmodified WRS probably because the airflow is still good and therefore the impact on the dissipation has not been relevant.

### 4. Conclusions

The performance improvement achieved by the inclusion of an external PLL for the GM frequency locking and a better coated main XO is indisputable. Many WR users will be delighted with this development but as a commercial product, some key points should be improved beyond the obvious performance gain.

Users who already have a standard WRS would need to open the equipment and accomplish some manual modifications which are not easy for all the people: a good soldering equipment is desirable in addition to good soldering skills. This process will void the product warranty, which may be not desired by all the users.

The documentation of the assembly process should be improved in order to keep under control the support emails and avoid receiving hundreds of emails. A step-by-step guide would be preferable than cover all the components separately. Information about power supply must be added in order to avoid problems with customers (burned boards) and on the use of the jumpers for the connectors W1-5.

The new GM mode is well integrated in the standard management tools, so the users should not experience any difficulties for using it. We’ve experienced some errors at WRS’s startup sometimes, but rebooting the device (typically a couple times) should fix it.

The Low Jitter Daughterboard offers a notably reduction on the overall noise when locking to an external clock reference but the design is too experimental and not suitable for all users. The manual process required to host the new board should not be accomplished by
unexperienced personal because errors can produce undesired noise on the clock system and thus, decreasing the performance expected.

From the commercial point of view, offering such modification to customers is very complicated. In one side, warranty is a big issue. We cannot offer such modified system as a final product with the typical two year operation warranty because it is at very preliminary stage and some weakness on the assembly process and thermal consideration can compromise the device operation and durability. Additionally, it could be required an upgrade of software/firmware to latest WRS versions. It could be complicated on some cases and customers need to be properly informed about related issues.

The other concern is about the market size. The production of the daughter board, including BOM for assembly is a feasible commercial option. It does not suffer of the previous warranty issue and we are happy to provide. Nevertheless, our preliminary impression is that just 2-3 institutions have already expressed its interest to play with the new features. Therefore, it looks that there is not a business opportunity to provide such modification as a standard product.

As final conclusion, we think that we can provide such modification to the few institutions willing to play with it (and pay a high NRE cost) but it does not make sense to include as a new product option. For future version of WRS, it will be very interesting including such features on the new hardware in a fully integrated and robust way.
Appendix I: Pictures of the assembly
Figure 3 Home-made solution without spacers (use spacers better!)