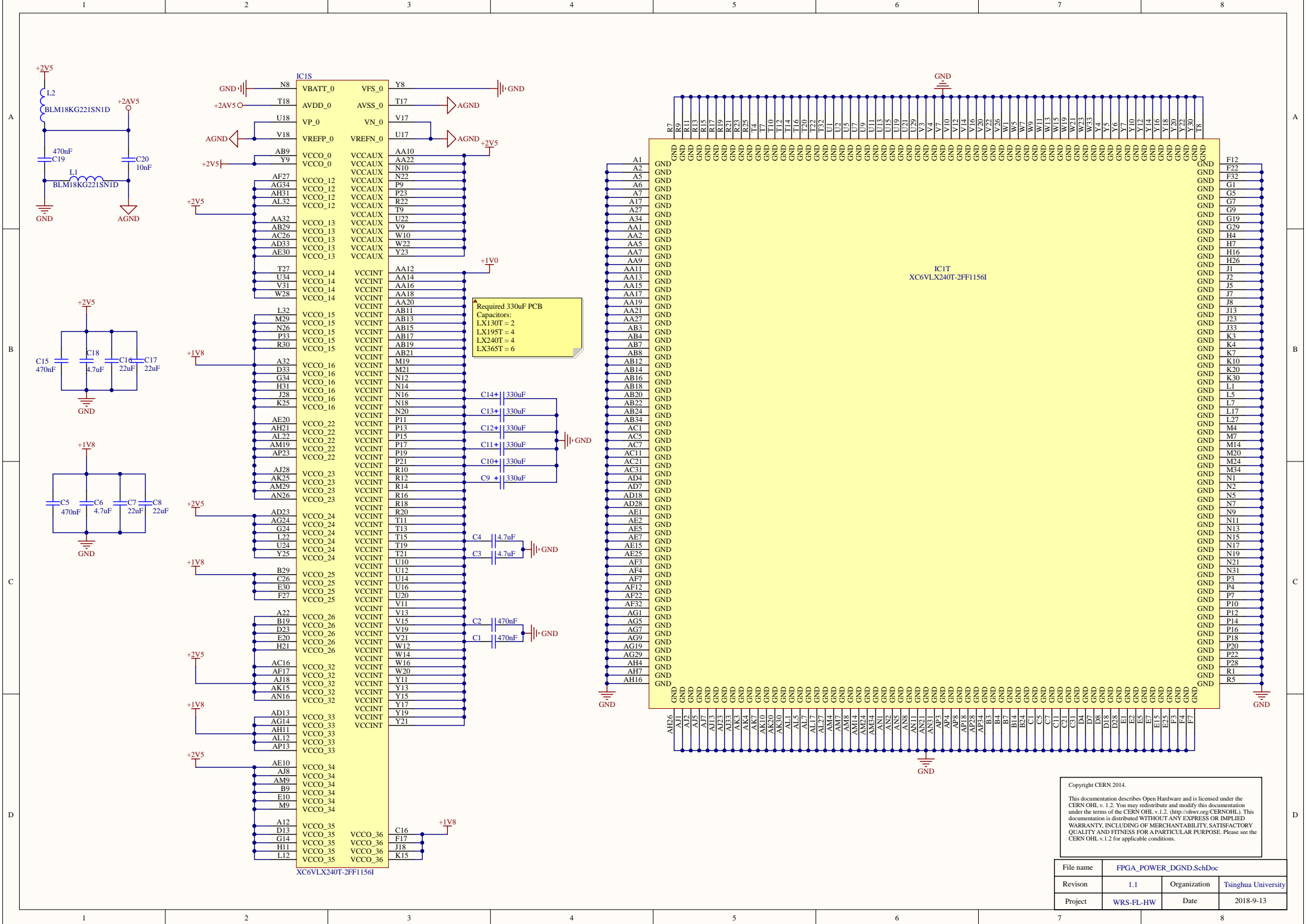


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| File name | FPGA_Configuration.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



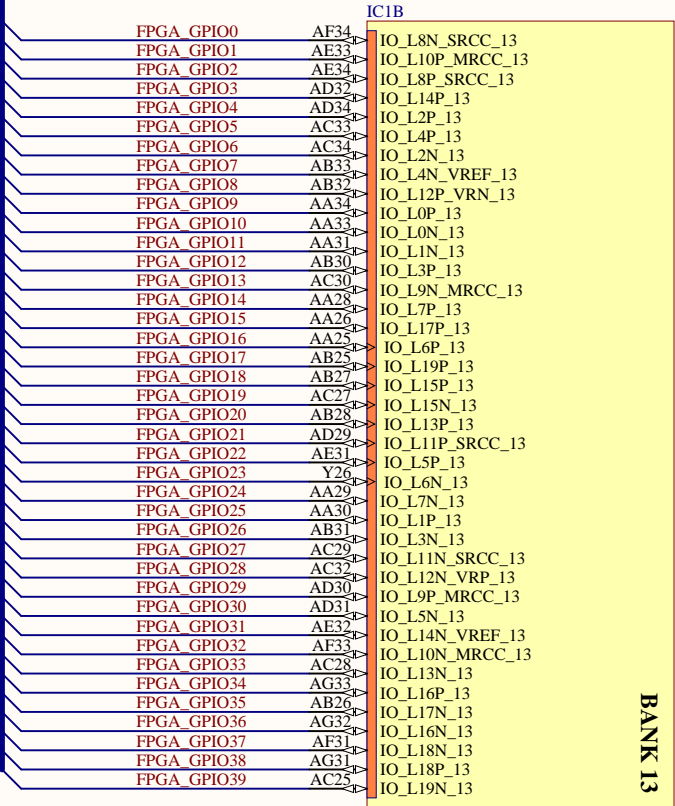
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| File name | FPGA_POWER_DGND.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |

FPGA_GPIO[0..39]

FPGA_GPIO[0..39]



IC1B

BANK 13

XC6VLX240T-2FF1156I

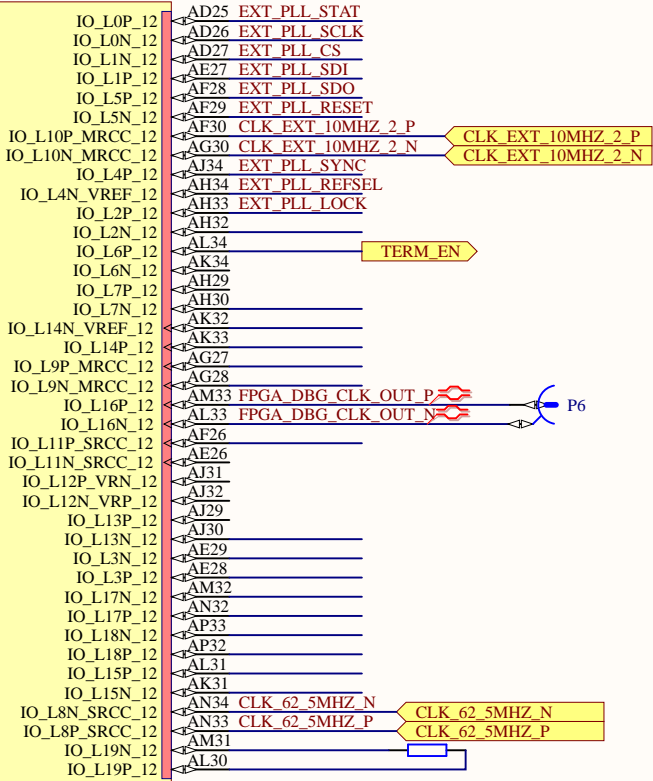
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| File name | FPGA_GPIOs.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |

IC1A

BANK 12



XC6VLX240T-2FF1156I

R36 100R

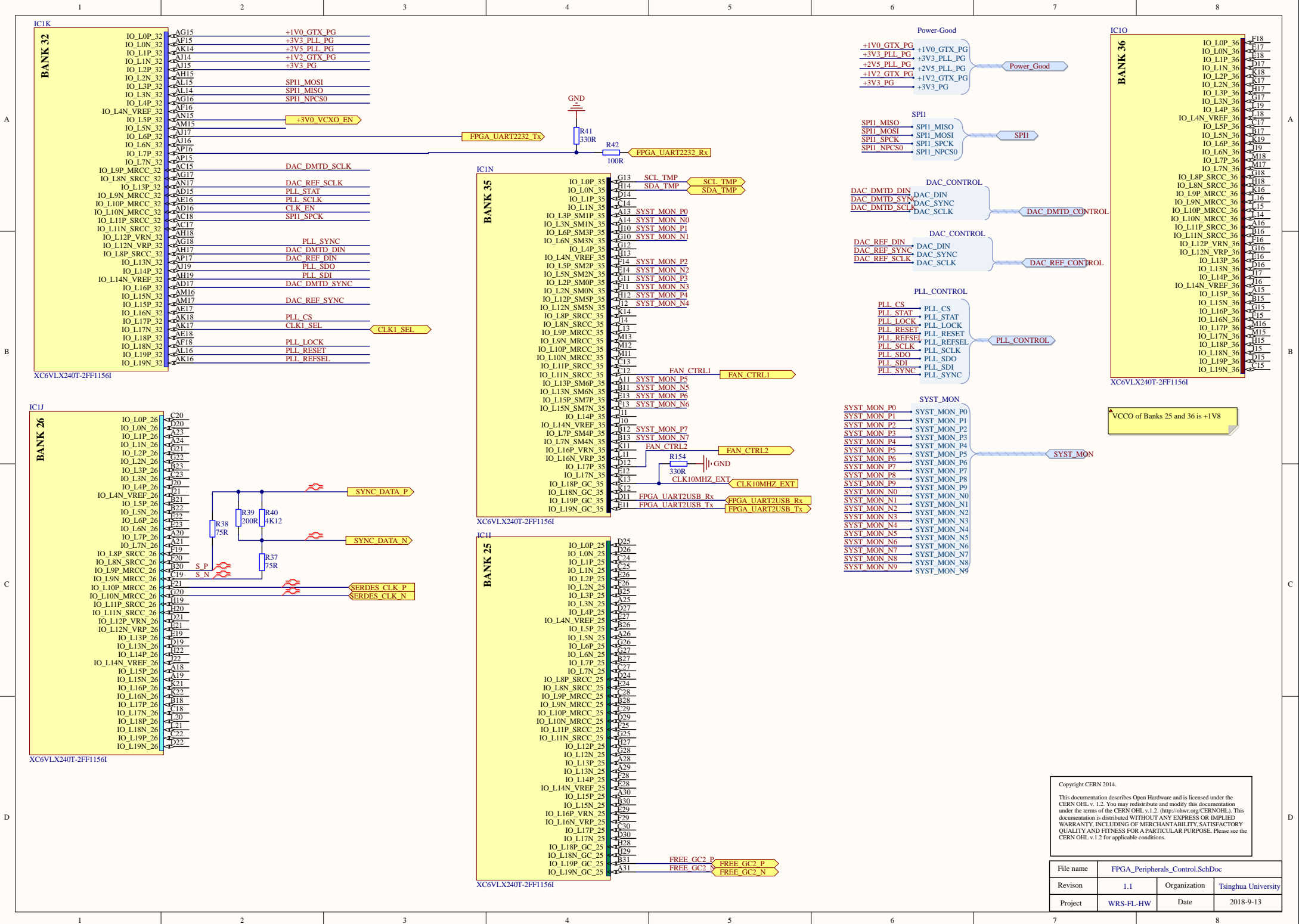
EXT_PLL_CTRL

- EXT_PLL_SYNC
- EXT_PLL_SDI
- EXT_PLL_SDO
- EXT_PLL_SCLK
- EXT_PLL_REFSEL
- EXT_PLL_RESET
- EXT_PLL_LOCK
- EXT_PLL_STAT
- EXT_PLL_CS

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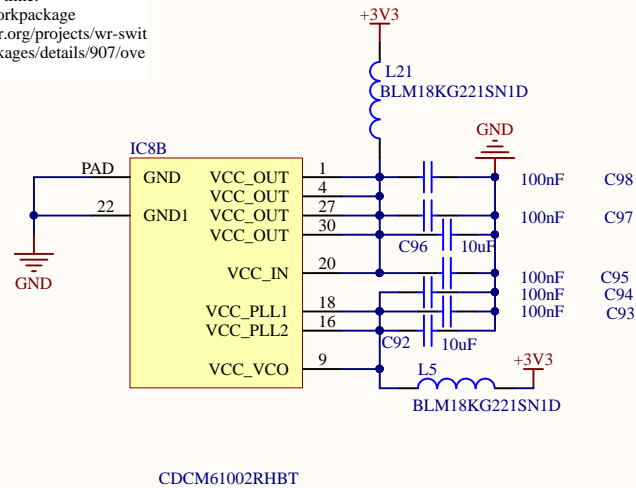
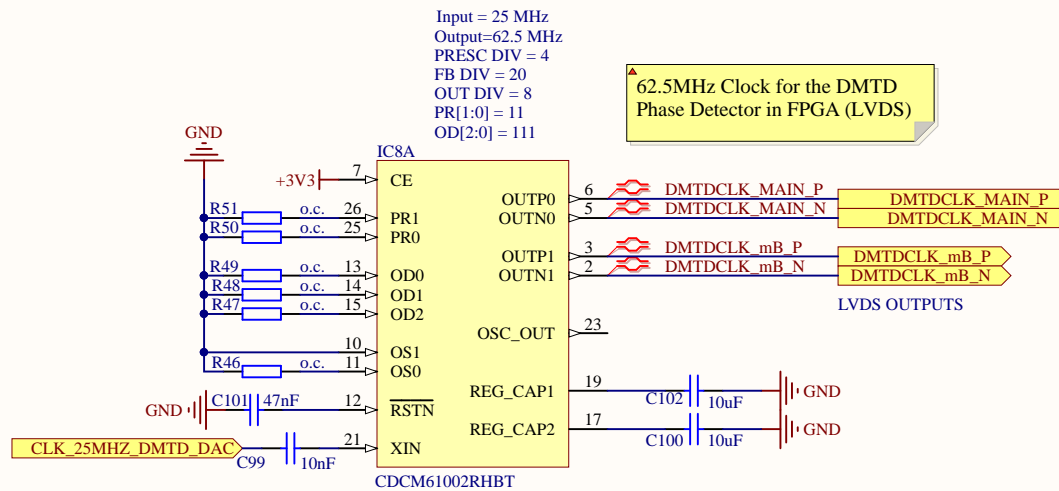
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| File name | FPGA_EXT_PLL.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



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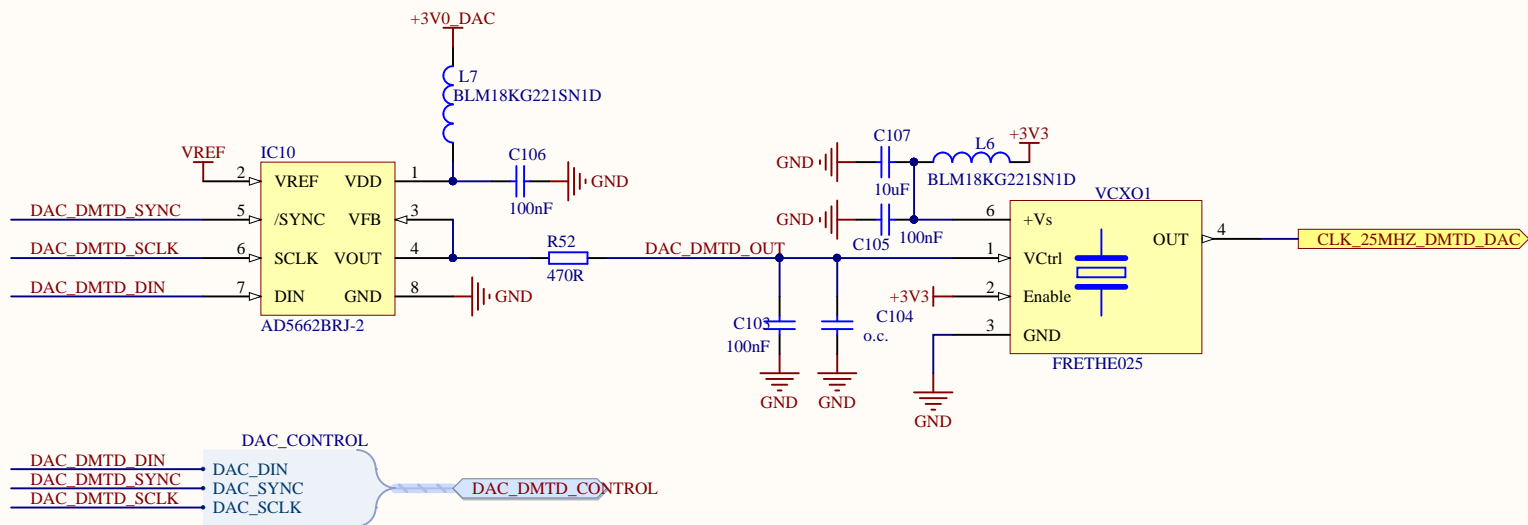
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| File name | FPGA_Peripherals_Control.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



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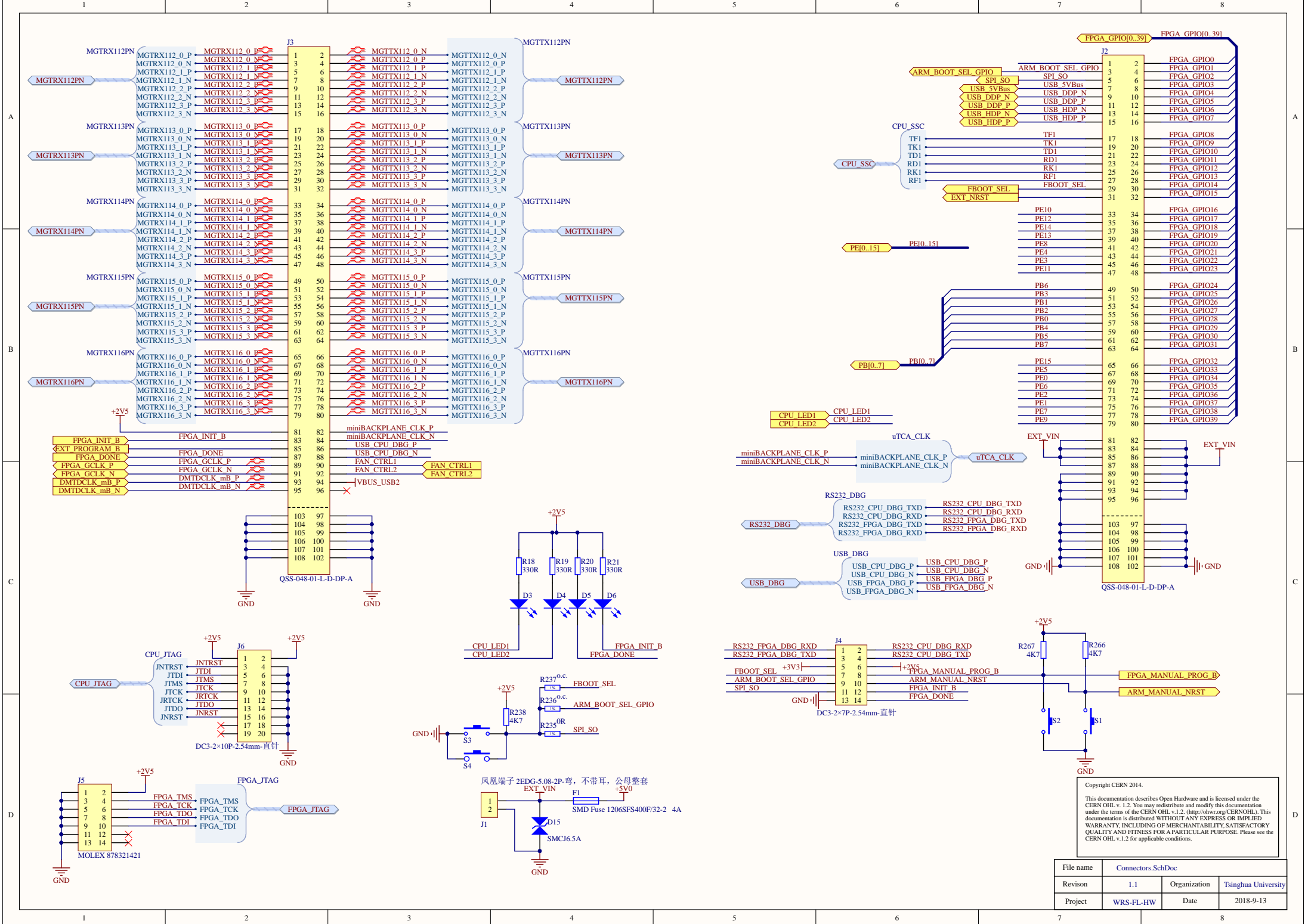
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| File name | CDCM61002.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



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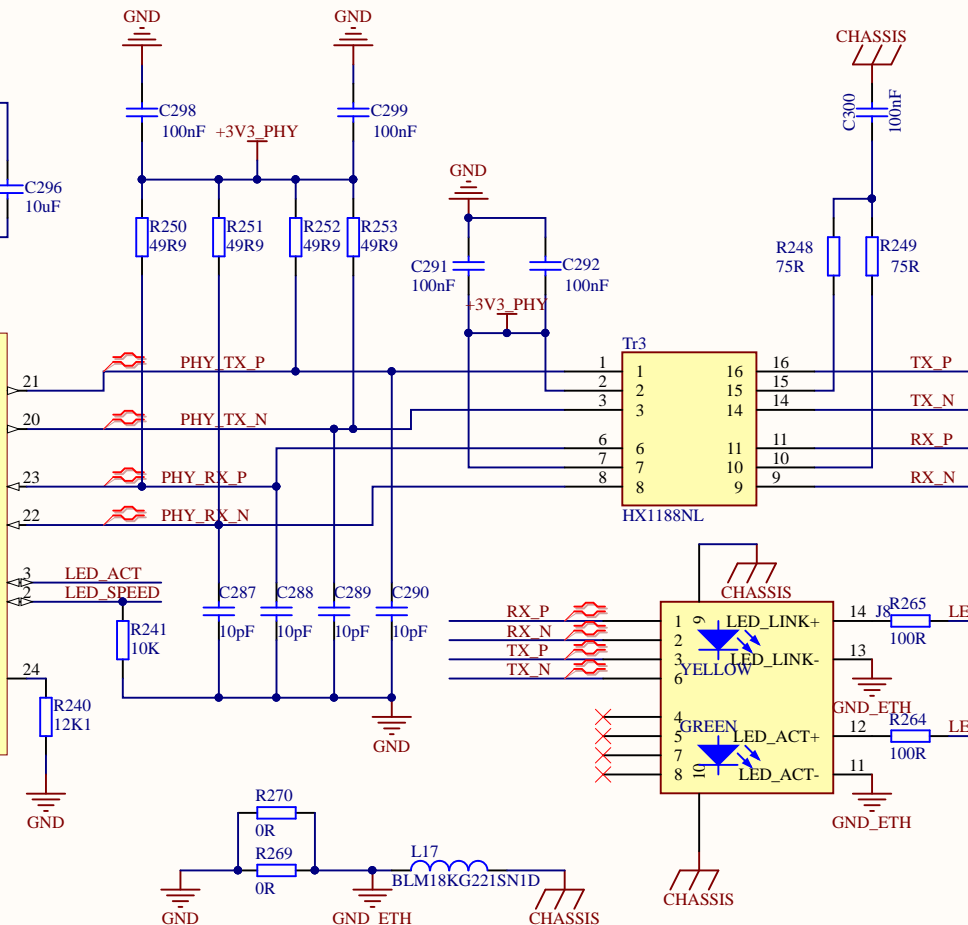
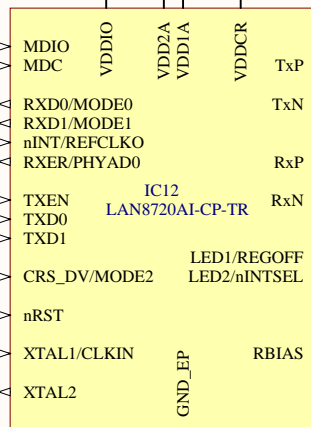
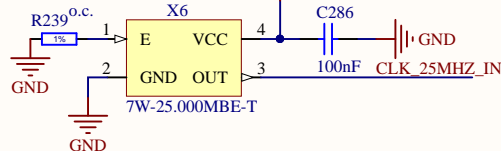
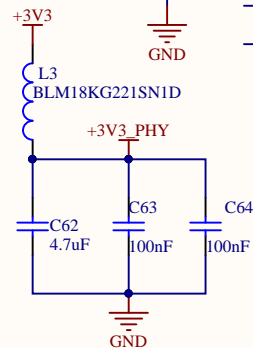
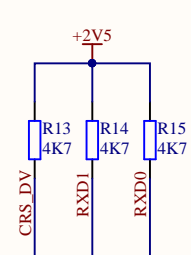
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| File name | CLK_25M_DMTD.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



IC2L

PA10/ETX0
PA11/ETX1
PA12/ERX0
PA13/ERX1
PA14/ETXEN
PA15/ERXDV
PA16/ERXER
PA17/ETXCK
PA18/EMDC
PA19/EMDIO
PA27/MCI1_DA4/ETXER
PA28/MCI1_DA5/ERXCK
PA29/MCI1_DA6/ECRS
PA30/MCI1_DA7/ECOL
(Power Supply VDDIO0)

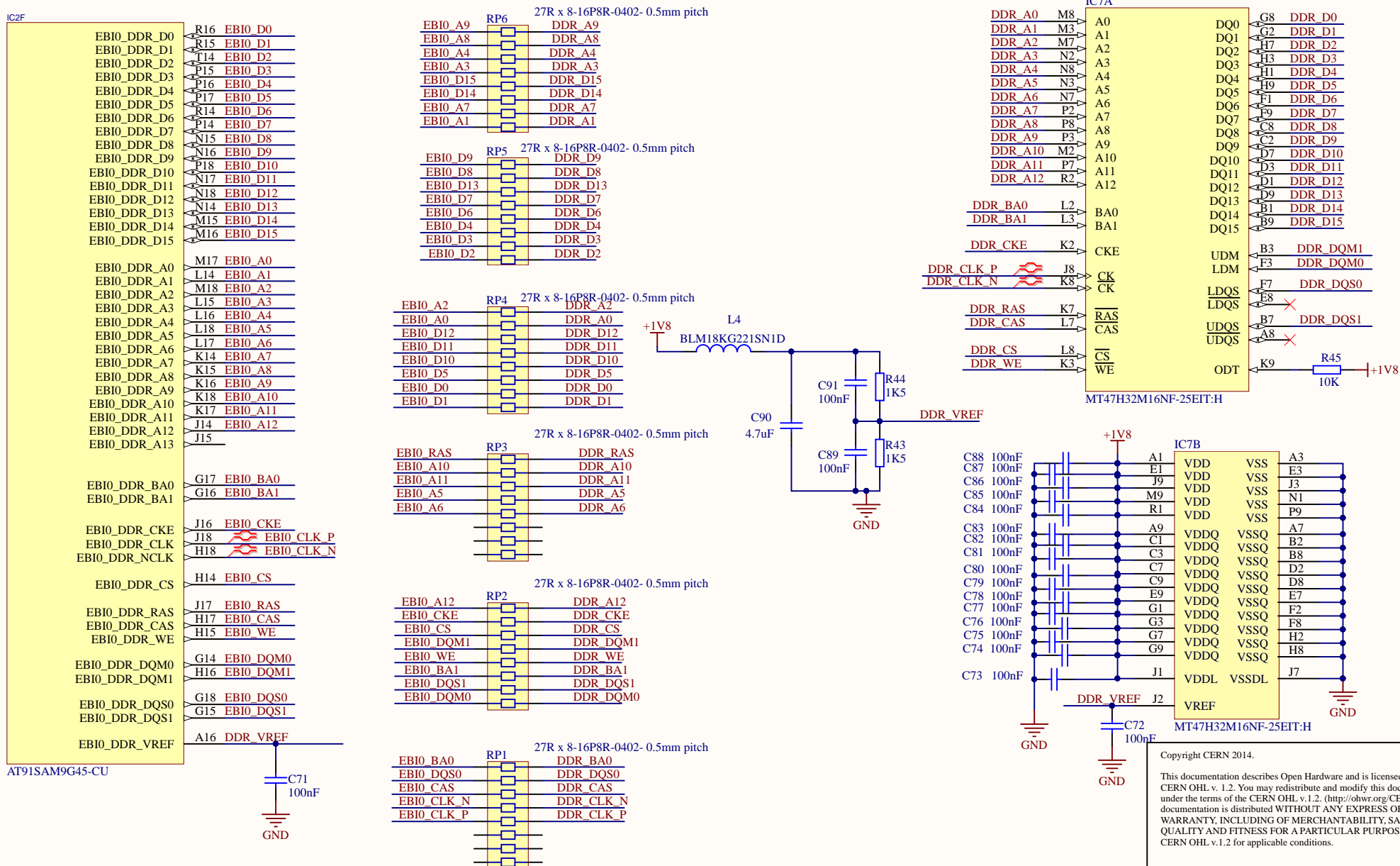
AT91SAM9G45-CU



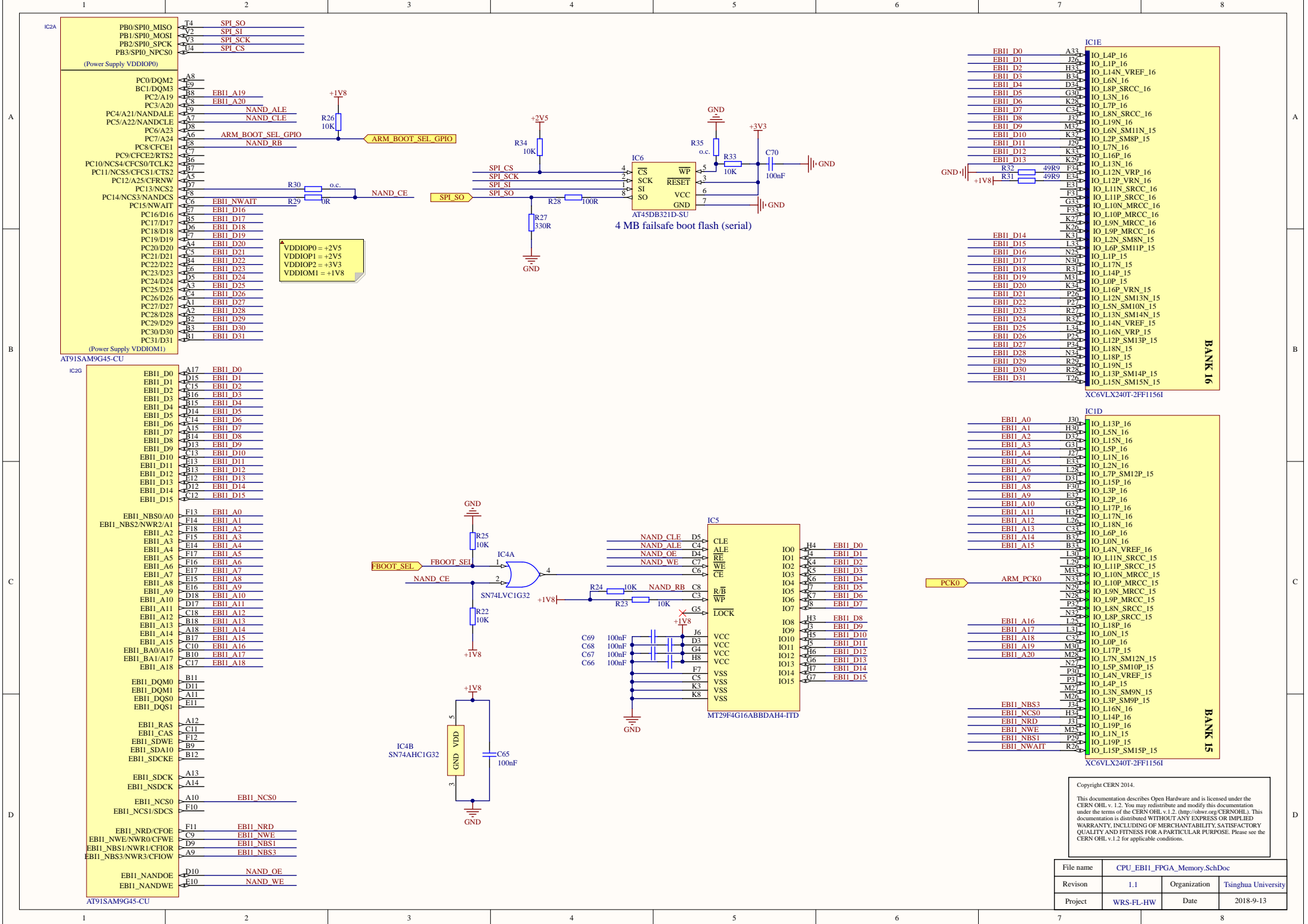
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|-----------|--------------------------|--------------|---------------------|
| File name | CPU_100M_Ethernet.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



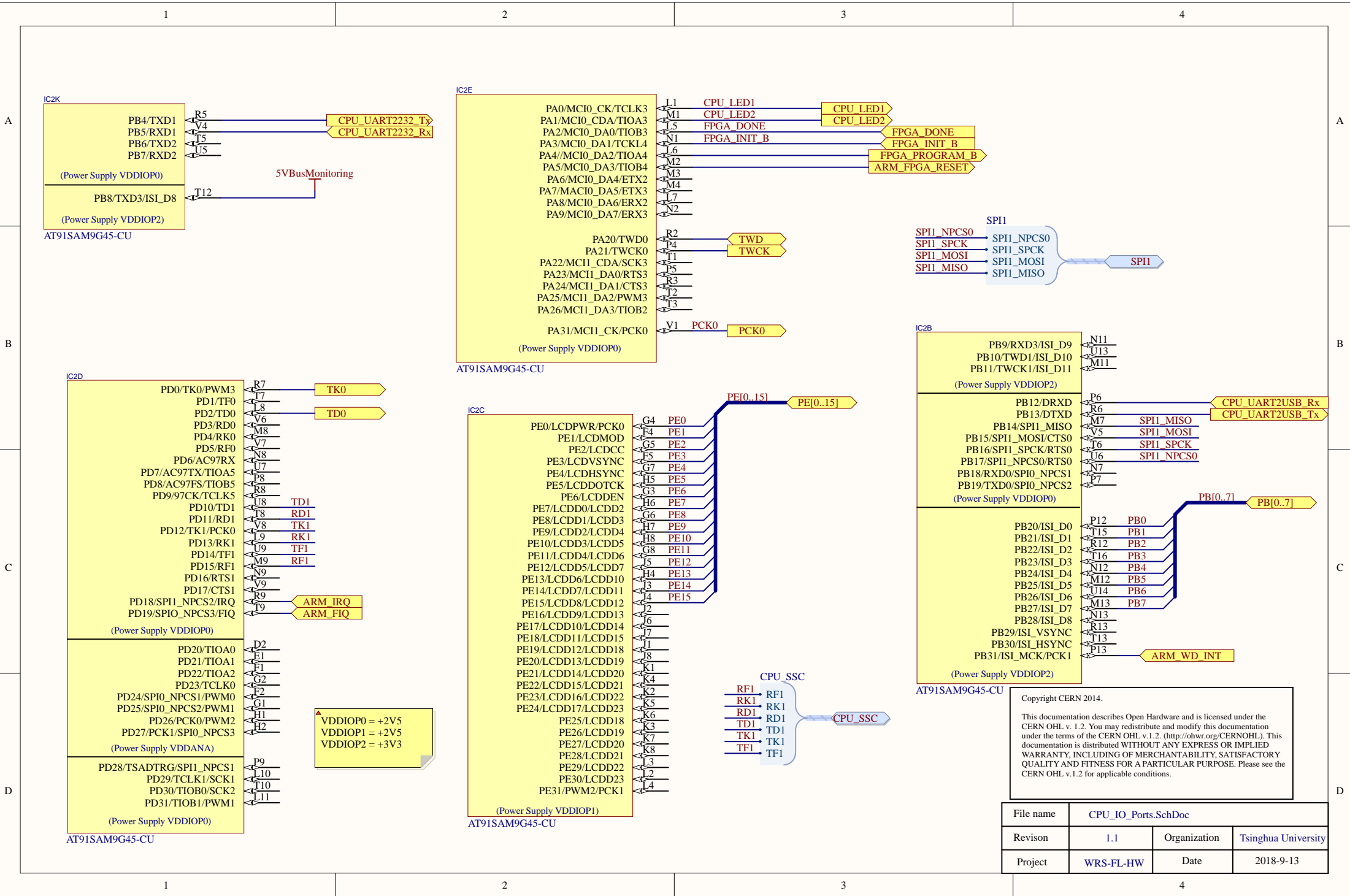
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| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |

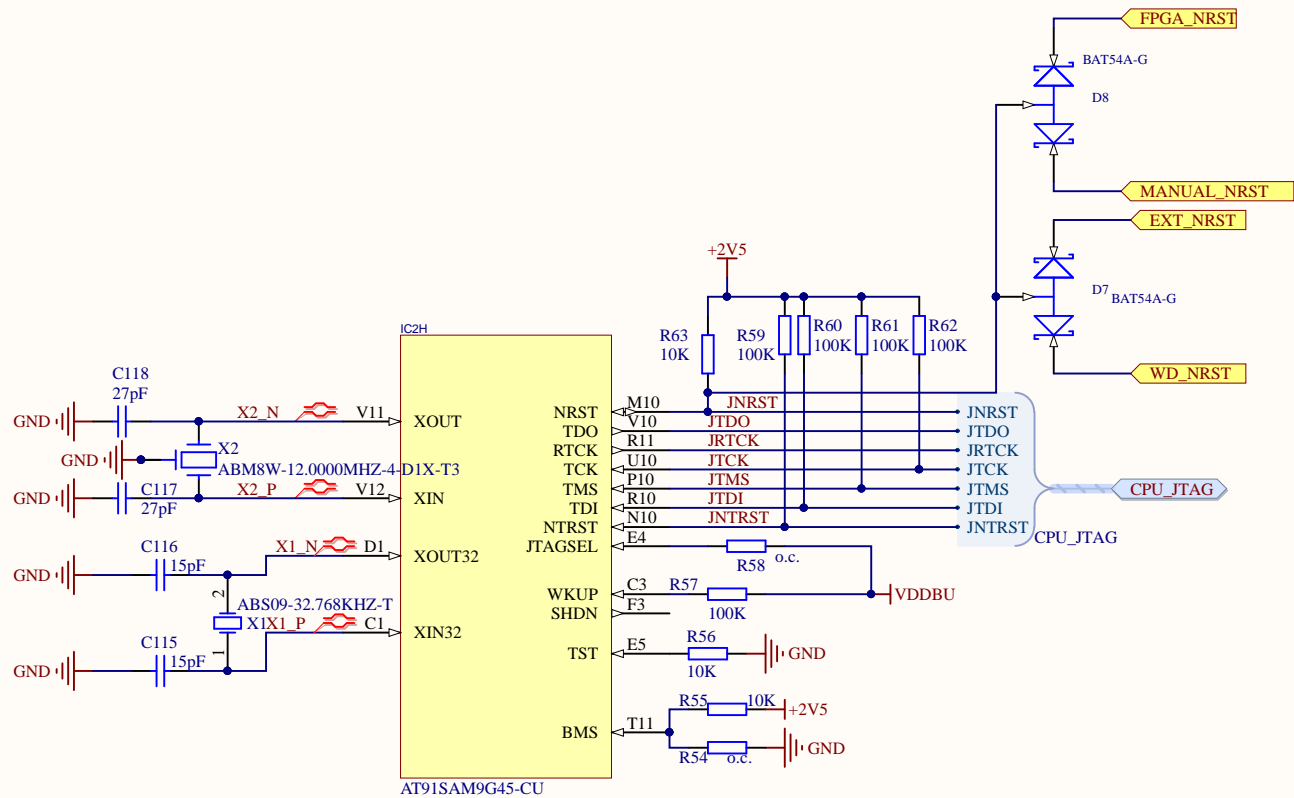


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| File name | CPU_EB11_FPGA_Memory.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |

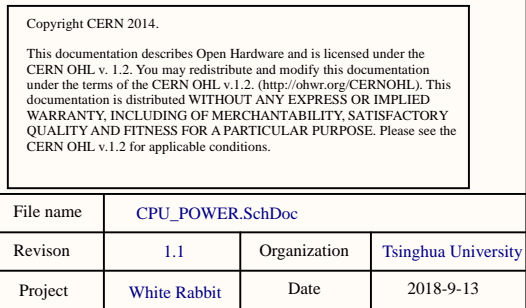


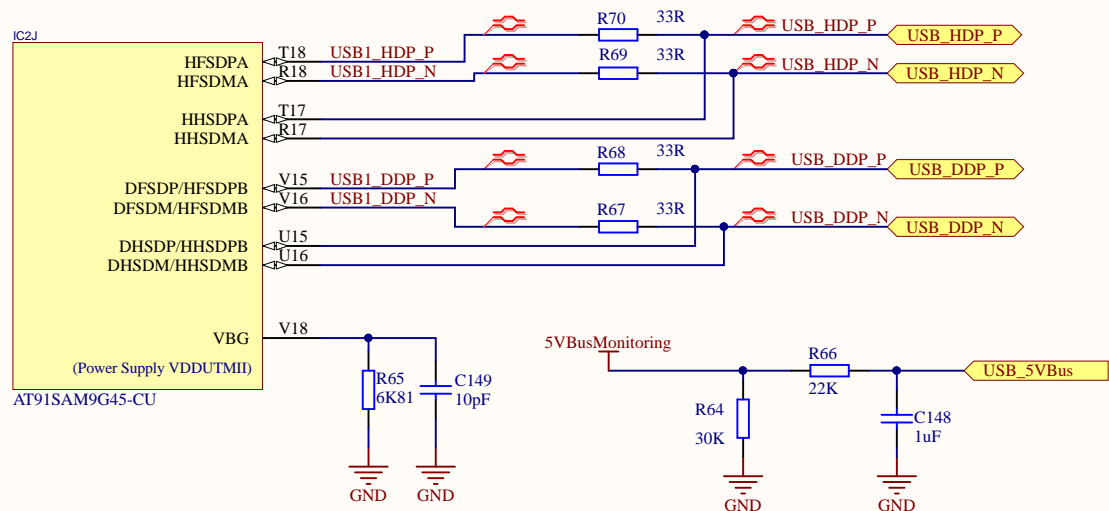


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| File name | CPU_JTAG.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | White Rabbit | Date | 2018-9-13 |

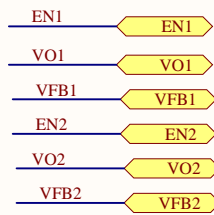
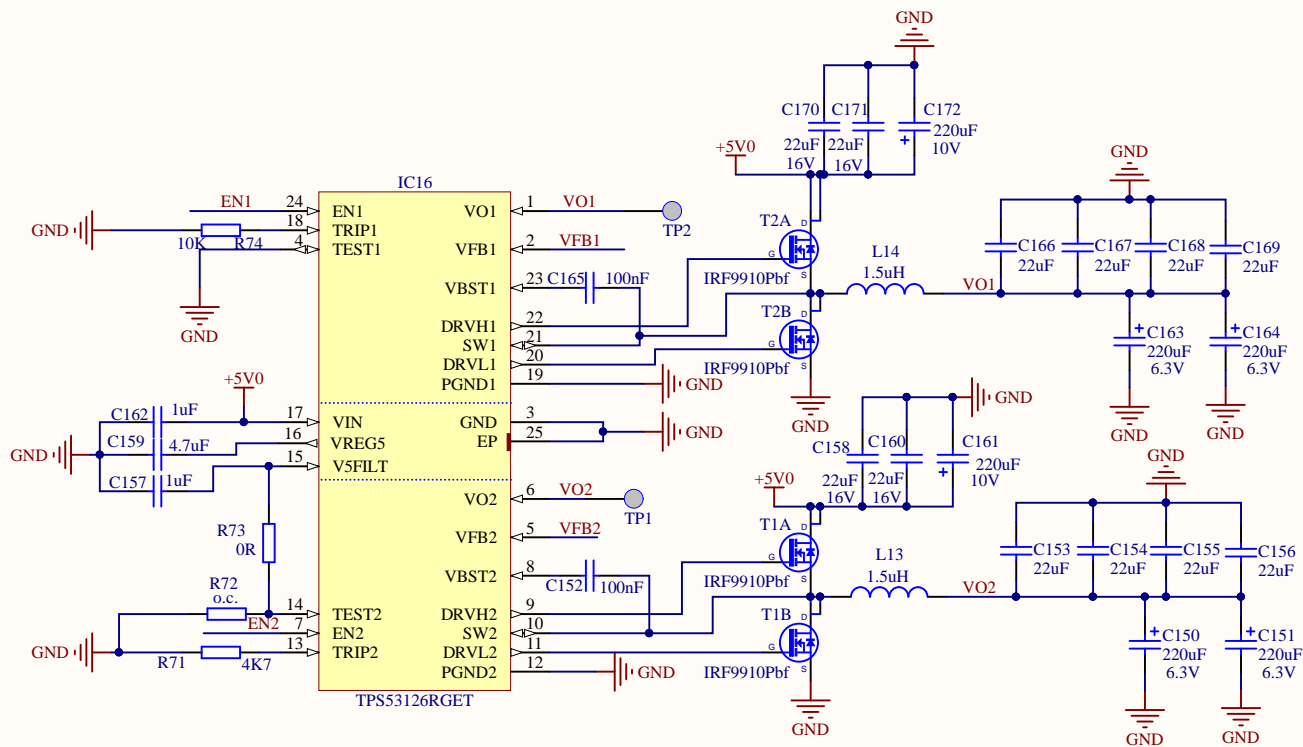




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| File name | CPU_USB.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | White Rabbit | Date | 2018-9-13 |



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|-----------|-------------|--------------|---------------------|
| File name | DCDC.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |

A

B

C

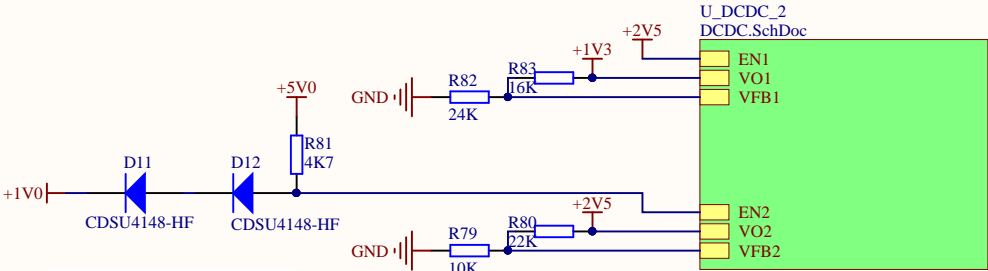
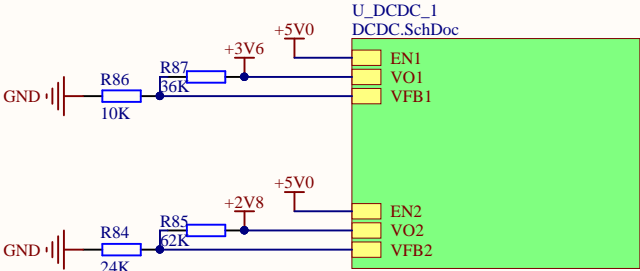
D

A

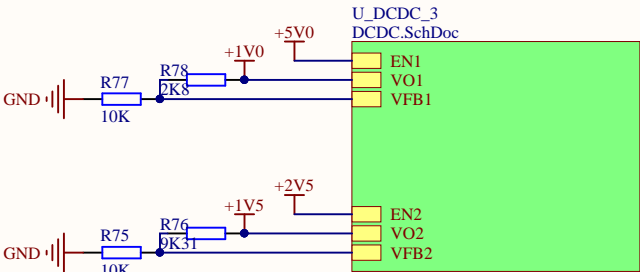
B

C

D



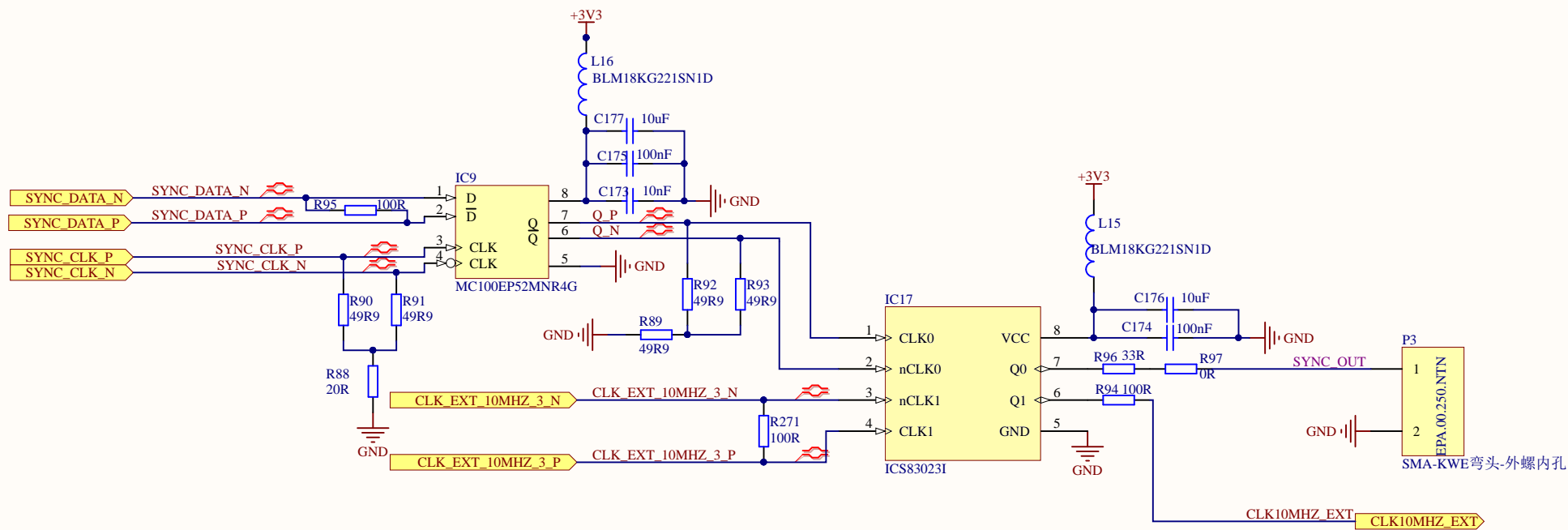
The voltage threshold of EN is 2.0V, the Vf-max of D4148 is 1V. Very critical, measurement shows that the 2.5V and 1.0V ramps the same speed.



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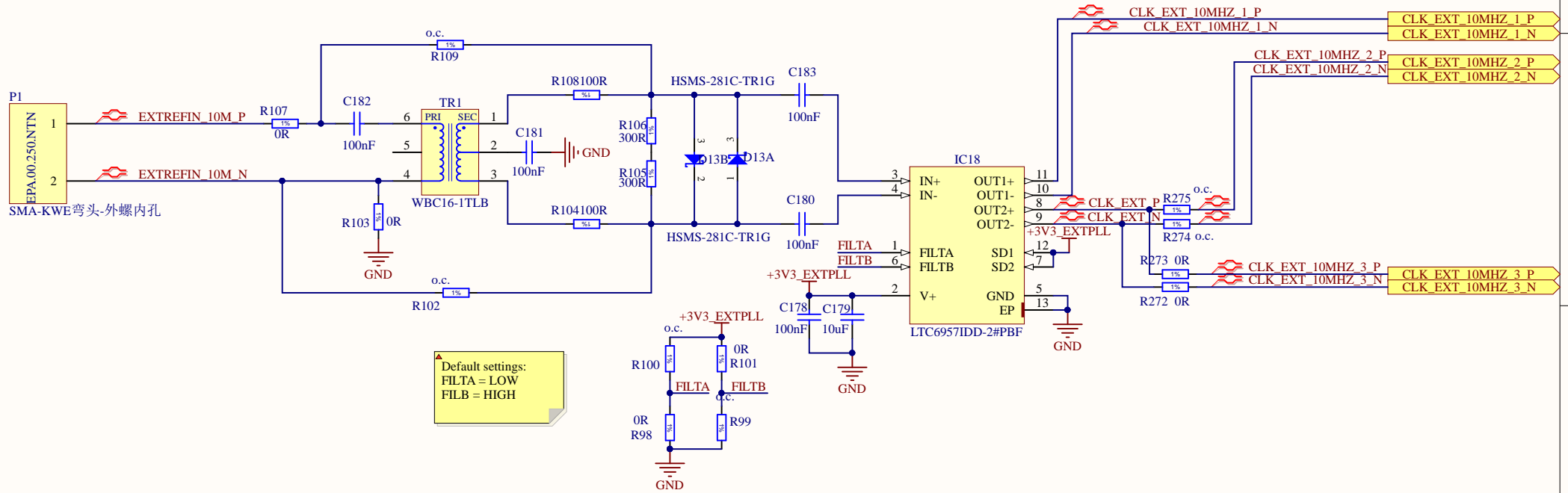
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| File name | DCDC_ALL.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



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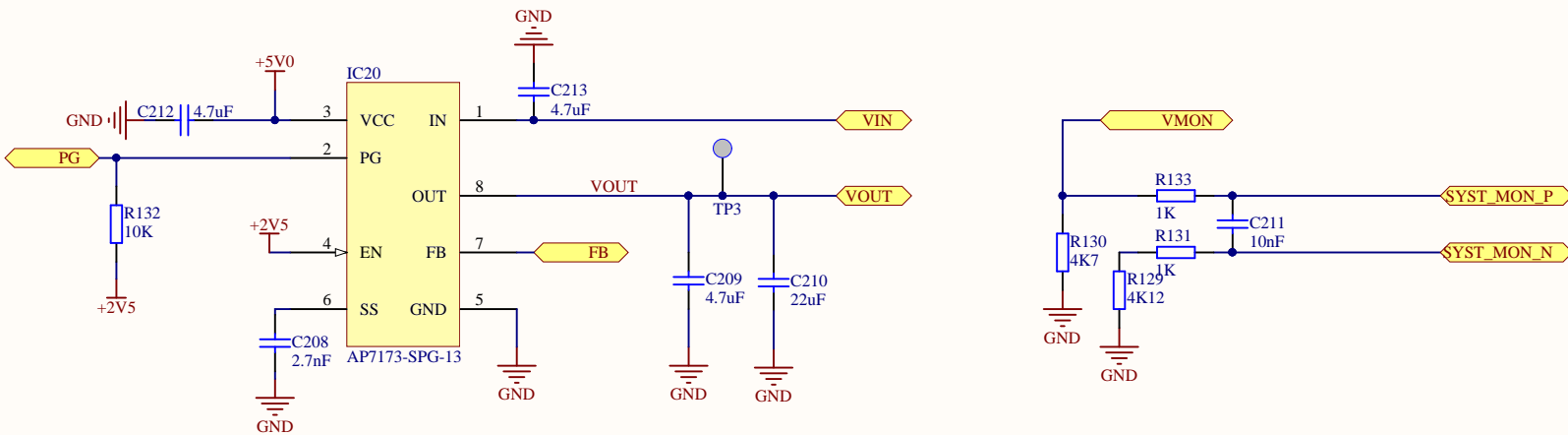
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| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



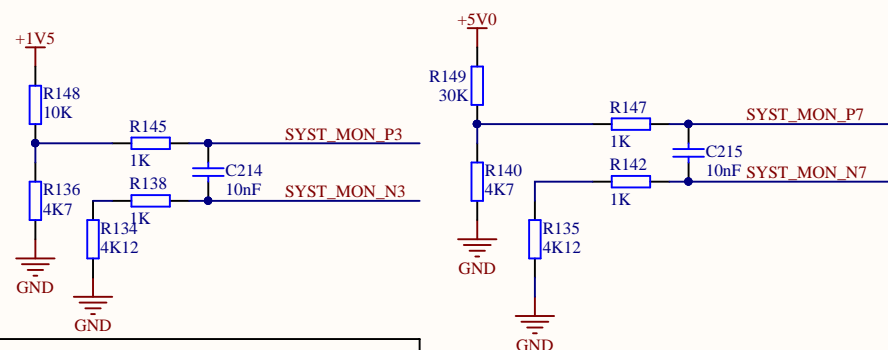
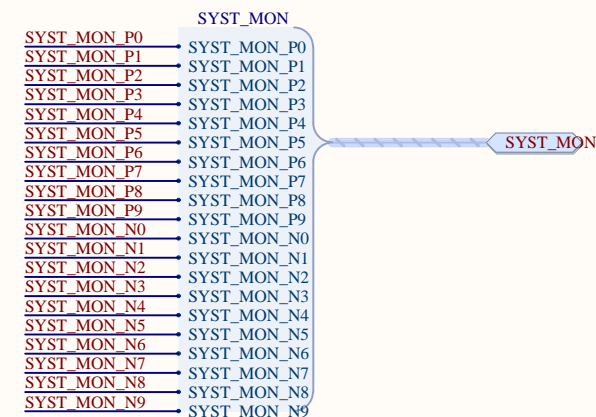
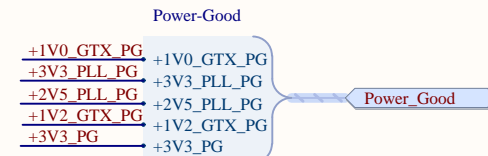
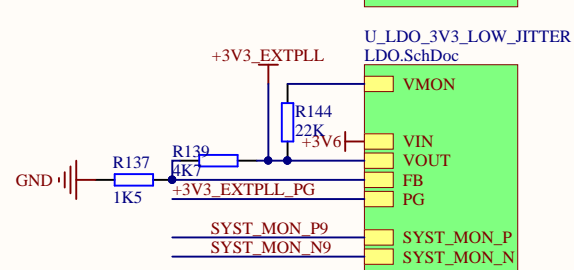
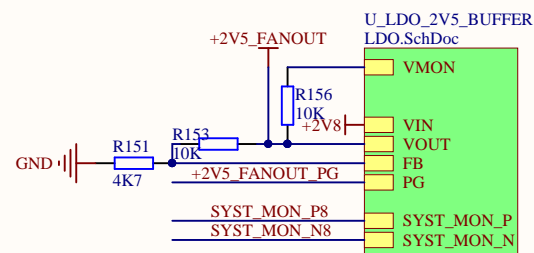
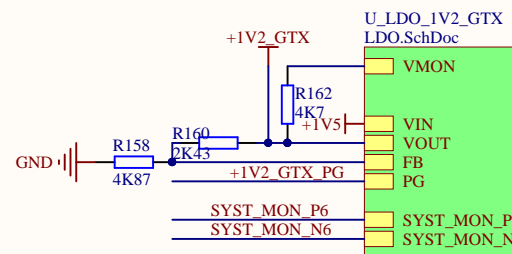
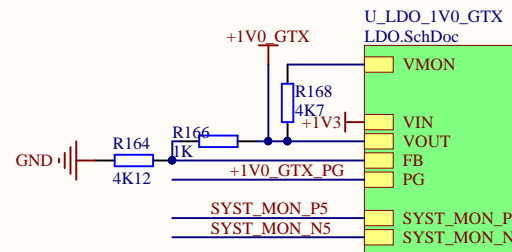
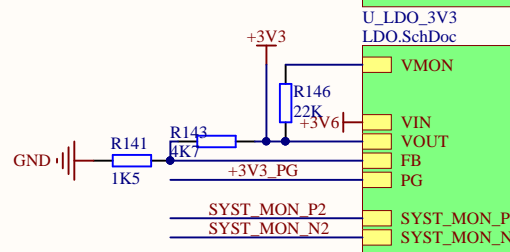
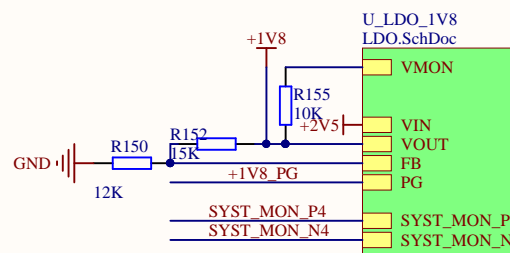
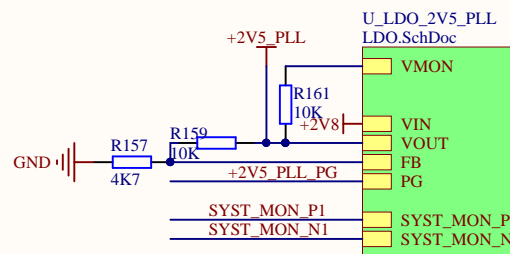
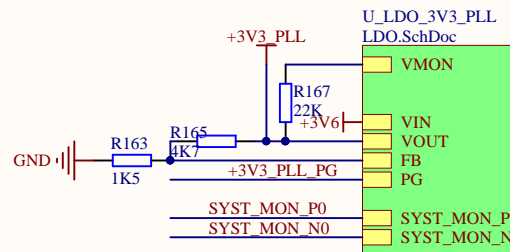
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| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



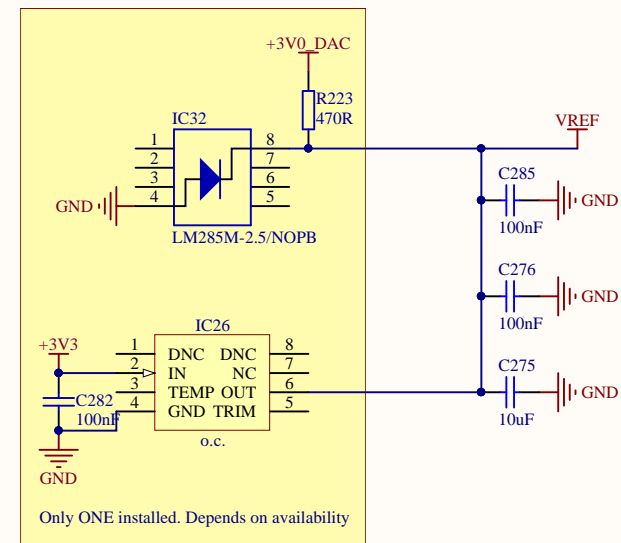
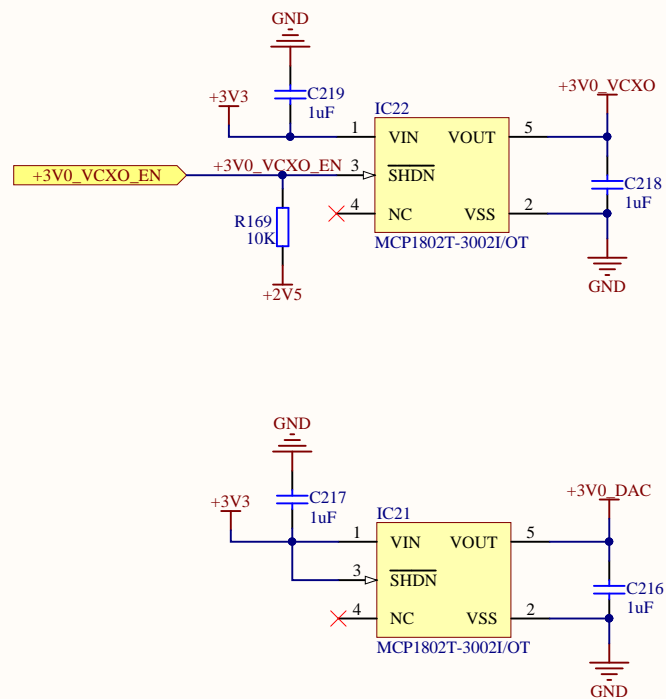
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| Size | Number | Revision |
| A4 | | |
| Date: | 2018-9-13 | Sheet of |
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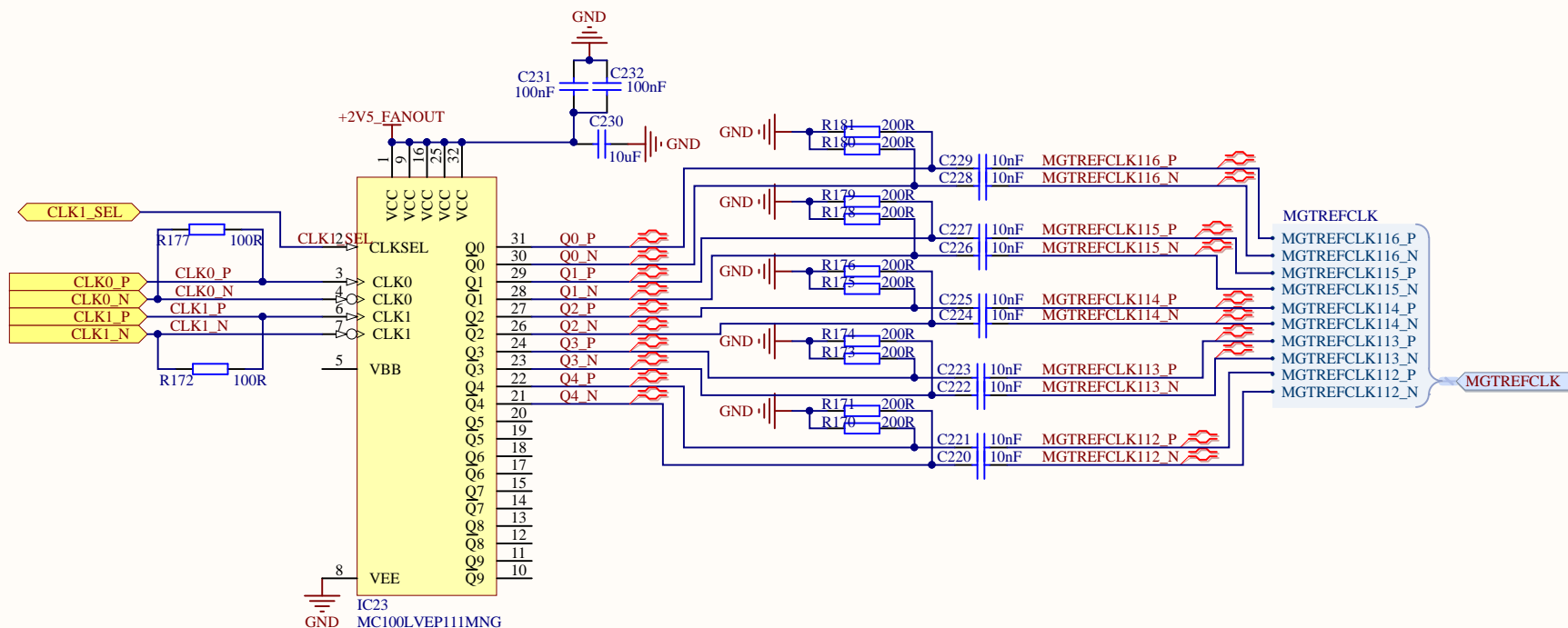
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| File name | LDO_ALL.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



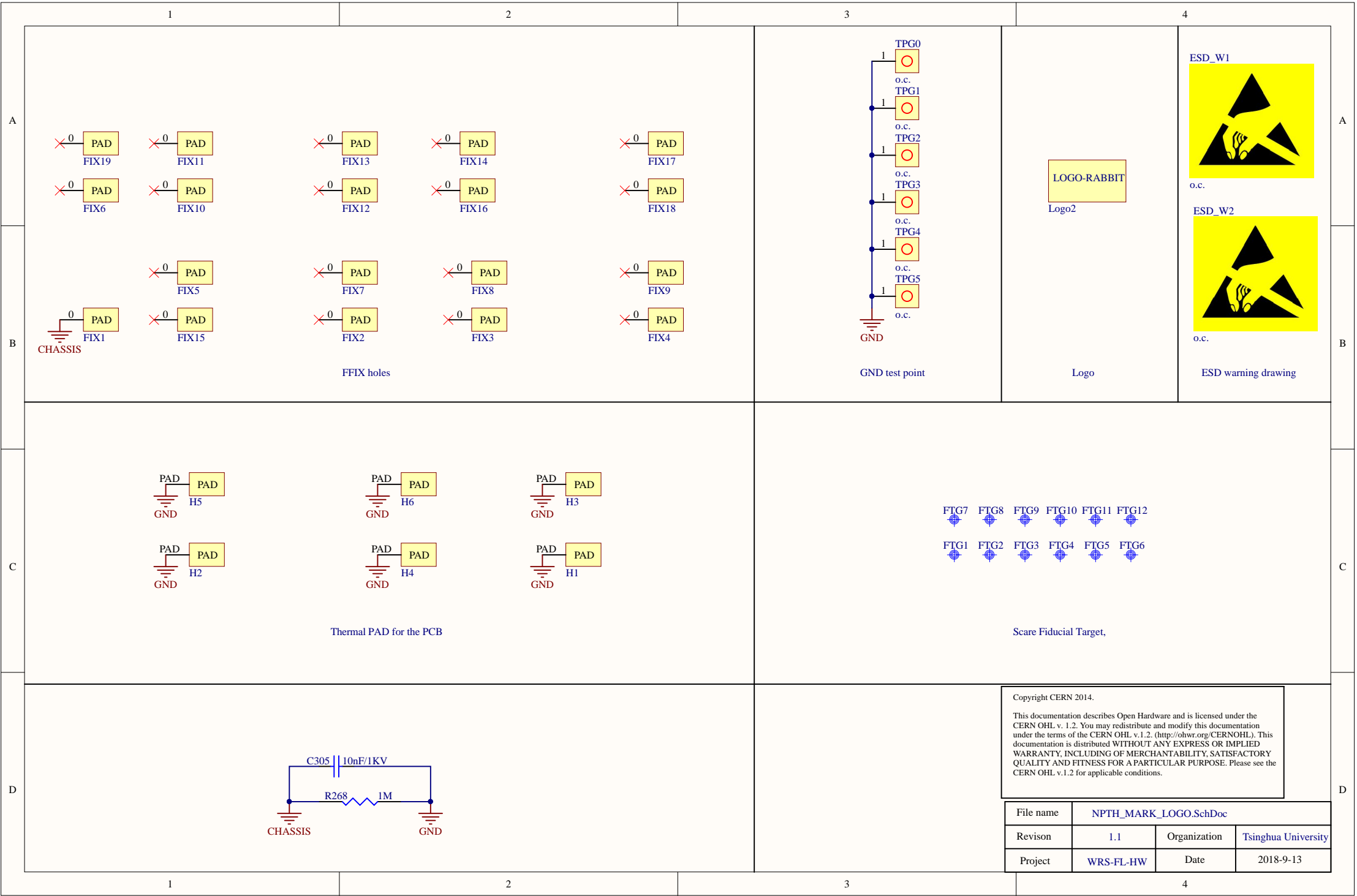
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| File name | LVPECL_FANOUT.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



0

PAD

FIX1

✗

0

PAD

FIX15

✗

0

PAD

FIX2

✗

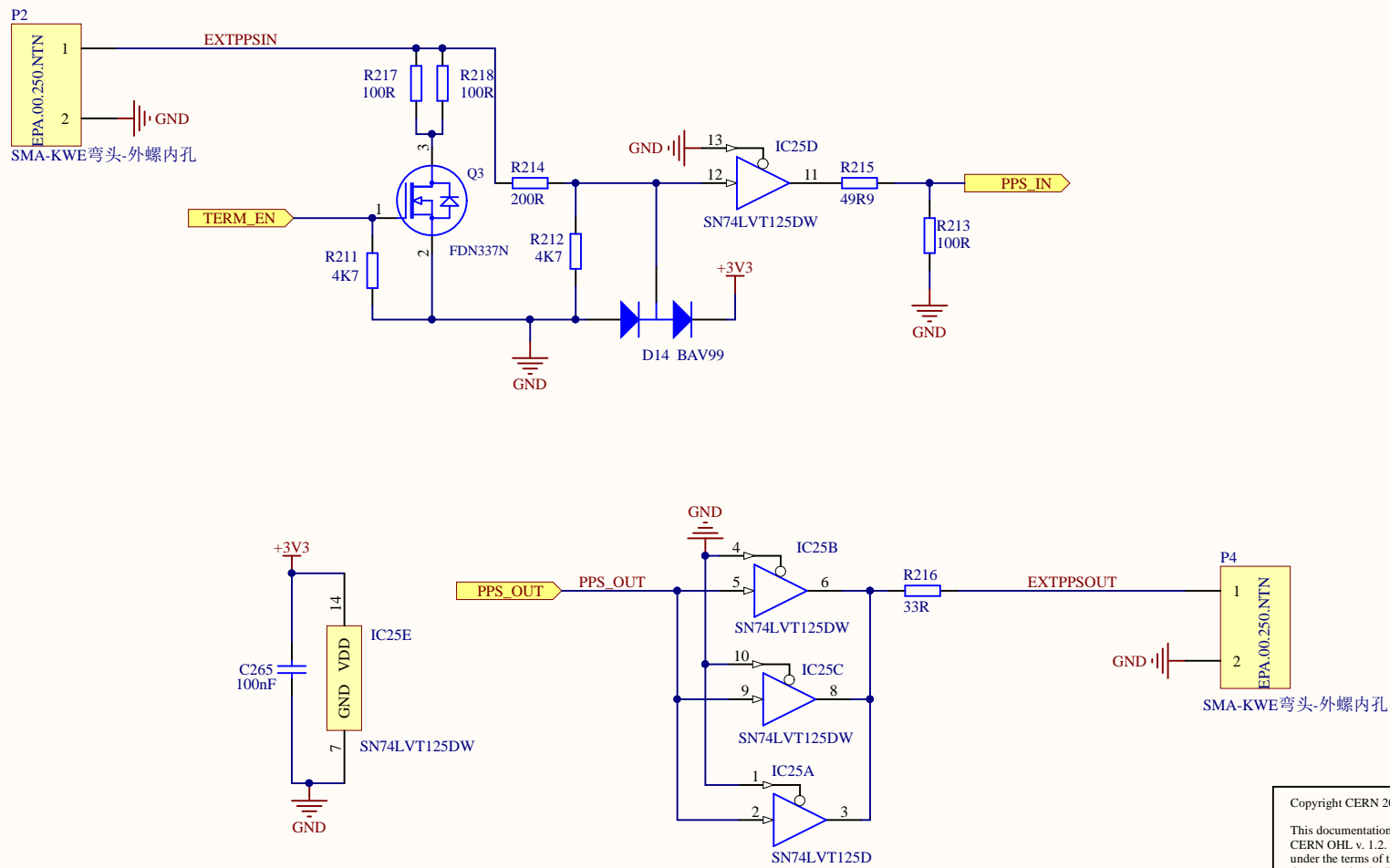
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PAD

FIX3

FFIX holes

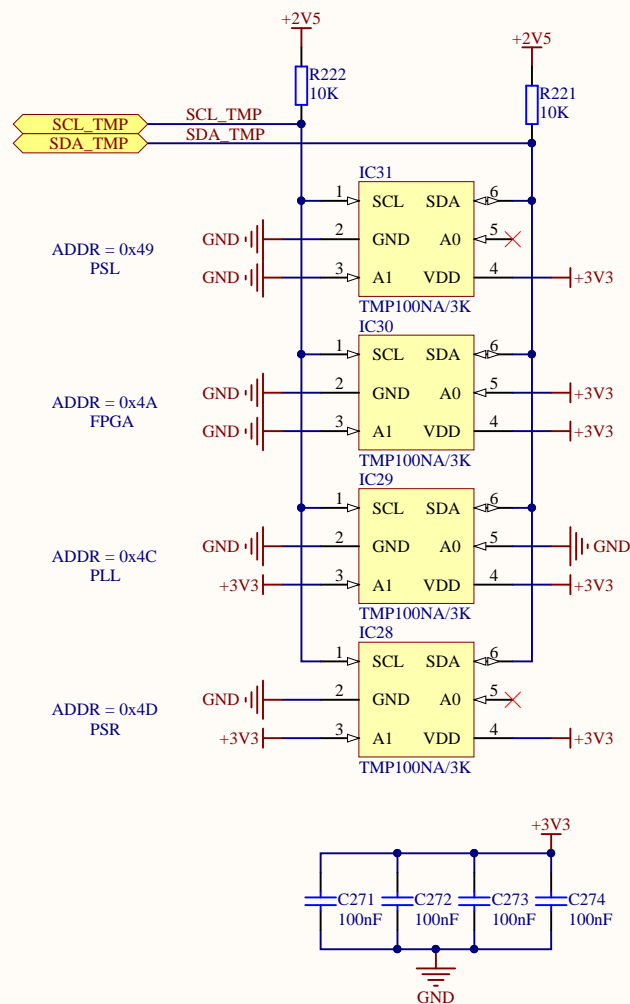
Thermal PAD for the PCB



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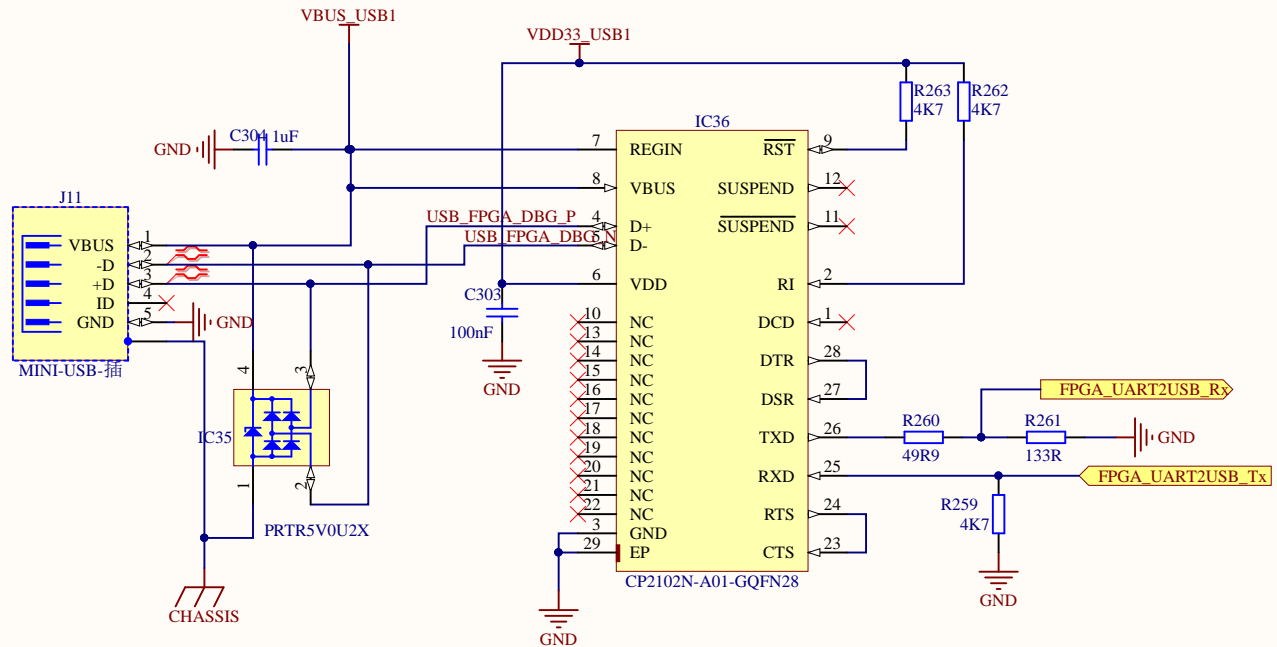
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| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



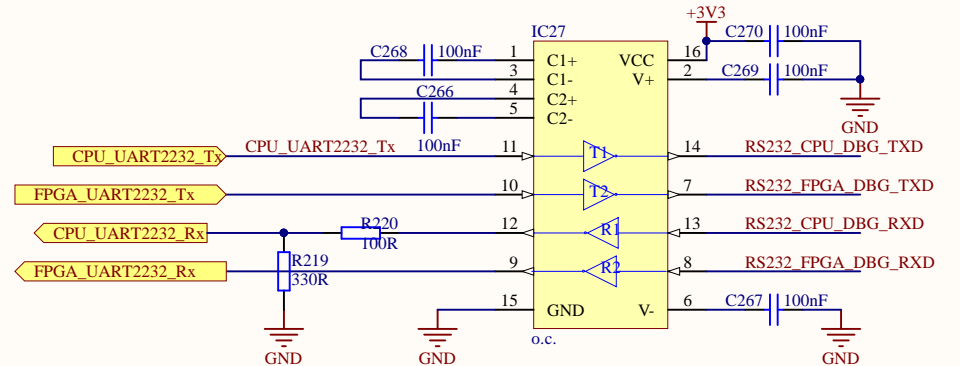
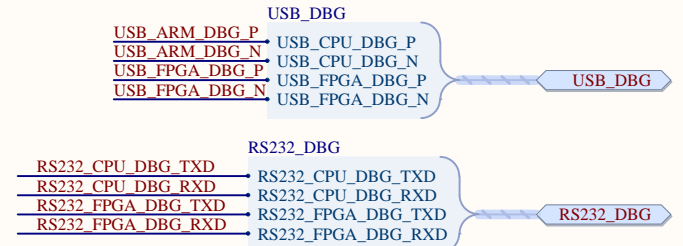
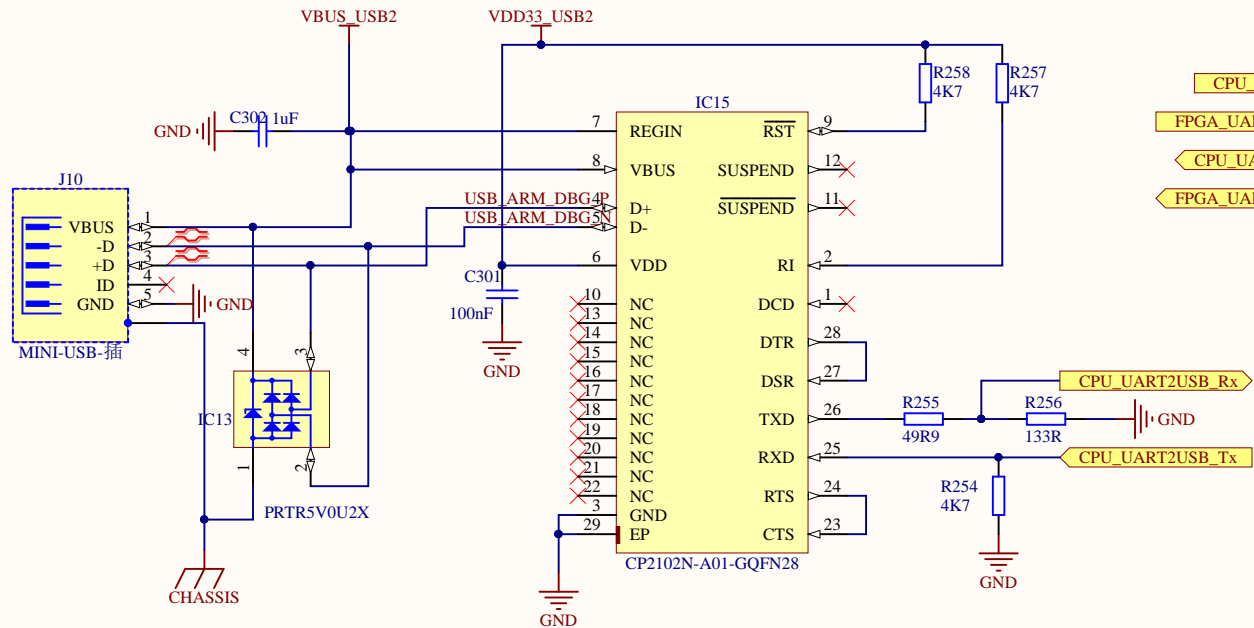
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| File name | SENSOR.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



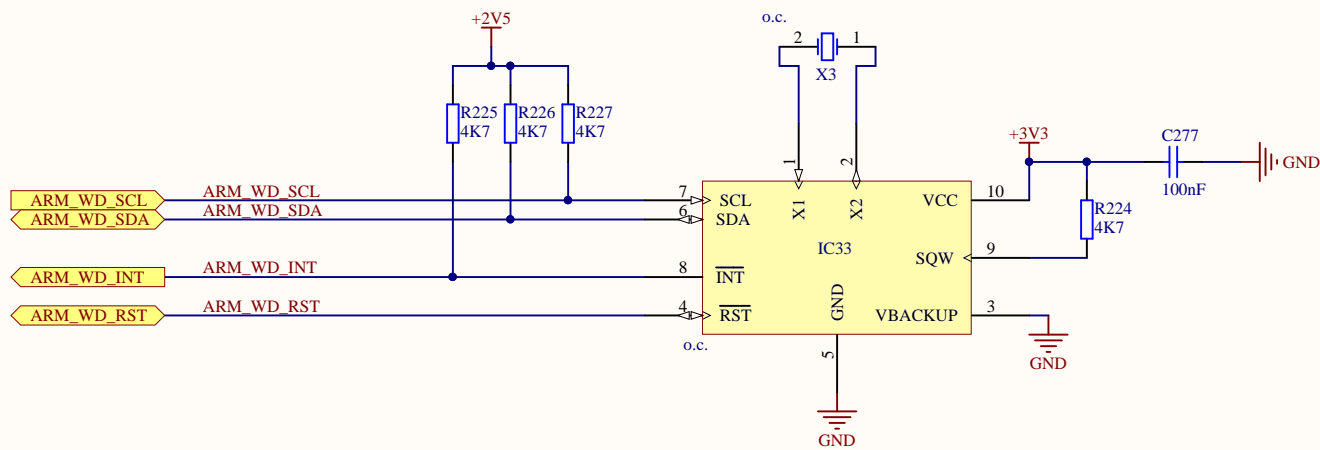
CP2102N work in BUS-power mode.



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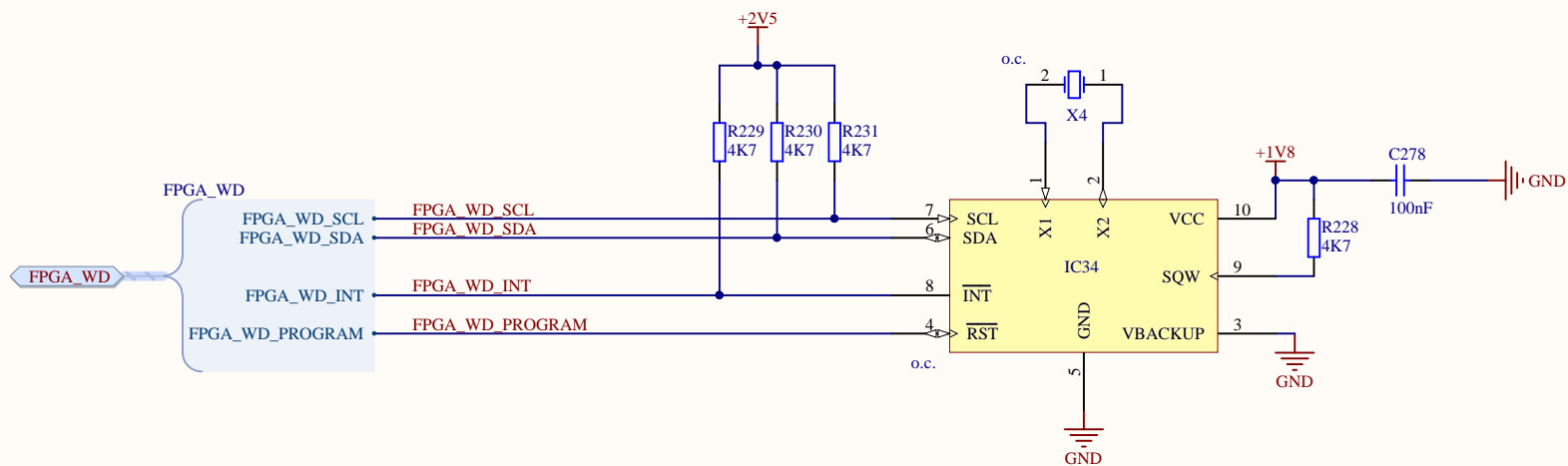
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|-----------|--------------------|--------------|---------------------|
| File name | UART_TO_USB.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |



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| File name | WDT_ARM.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | White Rabbit | Date | 2018-9-13 |



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|-----------|-----------------|--------------|---------------------|
| File name | WDT_FPGA.SchDoc | | |
| Revision | 1.1 | Organization | Tsinghua University |
| Project | WRS-FL-HW | Date | 2018-9-13 |