White Rabbit Switch

Production Test Suite

User Manual

Revision Table

Revision	Date	Author	Comments
0.1	30/03/2017	Bert Gooijer	Initial version.
0.2	03/05/2017	Bert Gooijer	Comments 21/04/2017 applied
0.3	16/05/2017	Bert Gooijer	Comments 15/05/2017 applied
0.4	29/05/2017	Bert Gooijer	Comments 26/05/2017 applied
1.0	31/07/2017	Grzegorz Daniluk	Official PTS release

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1. Introduction

Welcome to the Production Test Suite for the White Rabbit Switch – White Rabbit Switch PTS.

The White Rabbit Switch Production Test Suite (PTS) allows to perform production tests on White Rabbit Switch boards after manufacturing. It assures that the boards comply with a minimum set of quality rules, in terms of soldering, mounting and fabrication process of the Printed Circuit Boards (PCB).

It is important to note that the White Rabbit Switch PTS covers only to the production tests of the boards and does not cover any verification or validation tests of the design. This document describes the White Rabbit Switch PTS components and its use.

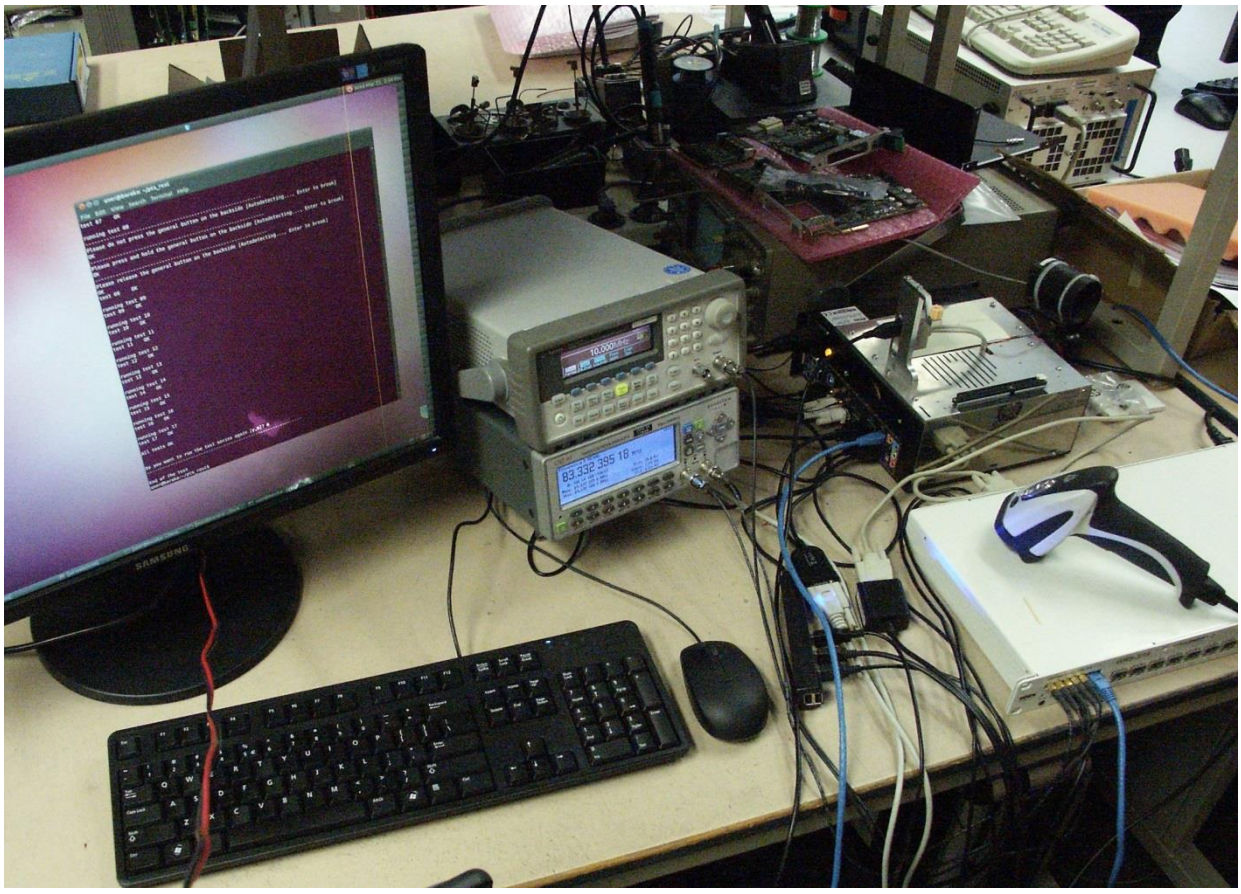


Figure 1: White Rabbit Switch PTS view

The main elements of the PTS are listed in Table 1.

Table 1: White Rabbit Switch PTS elements

Item	Comments
Computer	
Monitor	
Keyboard, Mouse	
Barcode reader	With USB connection to the computer
ESD wrist strap	
White Rabbit Switch	Device under test
Pendulum CNT-91	For frequency measurement, connected with USB cable A-B
Agilent 33250A	For frequency generation, connected with USB-RS232 adapter + RS232 cable
1x SMC – SMC custom cable	PPS in/out cable, see picture in Figure 4
3x SMC – BNC custom cable	Clock in/out, see picture in Figure 4
Custom SFP loopback adapter	Pin 3 shorted to pin 6
Sharp small pin	For flash button, for example dental stick
2x RS232-RS232 cable	Female – Female cross cable, Male – Female straight cable
2x USB – RS232 adapter	2 different types for automatic identification
USB hub	If your pc doesn't have enough USB ports
1x Ethernet cable	
3x USB A – USB mini B cable	
1x USB A – USB B cable	
Documentation	This user guide plus the one-page testing procedure

In terms of software, the computer is equipped with the following:

Table 2: PTS software requirements

Ubuntu Linux 11.04 (2.6.38)
Python 2.7 + python-dev
Git
Python-pip pexpect numpy pyro4 ptyprocess
Dnsmasq
Nfs-kernel-server

The user login is:

Table 3: Computer login

Username	user
Password	baraka

Note that after the software installation the computer should be disconnected from the network and no updates should be allowed.

The following paragraphs provide an overview of the required items.

Figure 2: All needed cables/parts

To be able to test all lines a small modification has to be done to the SFP loopback adapter.

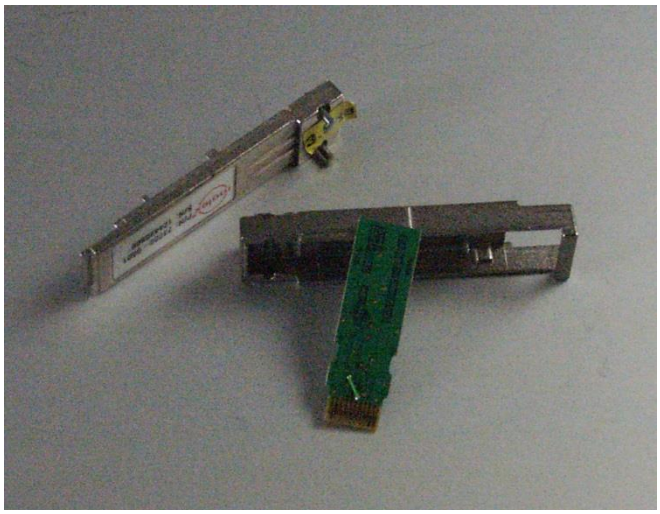


Figure 3: Custom SFP loopback

Custom SMC to BNC and SMC to SMC cables are needed for testing the front intefaces.

Figure 4: Custom SMC cables

The Agilent and Pendulum can be remotely controlled and are used for verifying clock in and outputs.

Figure 5: Pendulum + Agilent

The test setup is shown on Figure 6.

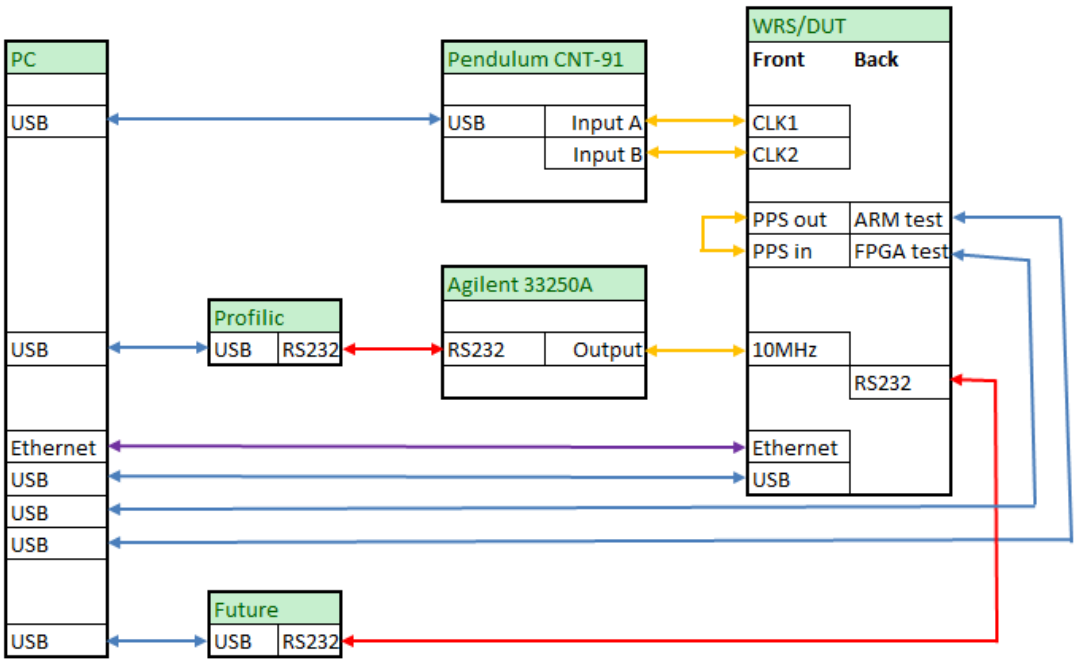


Figure 6: Test setup connections. USB-USB cable is marked blue. RS232-RS232 cable is marked red. Custom SMC-BNC/SMC cables are marked yellow. Ethernet-Ethernet cable is marked purple.

The complete duration of the test is around **forty minutes.**

In brief, the operator needs to:

- connect the cables between the DUT-Pendulum, DUT-PC, DUT-Agilent and the control lines for the Agilent+Pendulum
- run the software
- at certain points of the tests an intervention needs to be done by the operator (e.g.: scan the board's barcode, check the front panel LED); the interventions are explicitly signaled by the PTS software and this manual.

At the end of the functionality tests the operator receives a PASS/FAIL notification. In case of a FAILED board, information is provided on the failing components.

All test results are automatically saved in a folder on the computer.

A board is considered to have passed the PTS testing if it has successfully completed all the functionality tests.

For a FAILED board, you can repeat the test only one more time! If a board FAILs twice, please report to the CERN responsible.

2. White Rabbit Switch Functionality

White Rabbit Switch is an open hardware design of an **18-ports Ethernet switch** licensed under CERN OHL 1.2. It is a central element of a White Rabbit network and was designed as a part of the White Rabbit project.

The White Rabbit Switch (WRS) is the key component of the White Rabbit System that provides precision timing and high accuracy synchronization in an Ethernet-based network. The WRS-3/18 version is a standalone version with 18 SFP connectors. The WRS distributes the clock of a WRS master (or its internal clock) to all the nodes in the network using a hierarchical architecture.

Figure 7: Front, back and inside views of the White Rabbit Switch

3. PTS Functionality Tests

The PTS consists of a set of seventeen independent tests, each one checking a different part of the White Rabbit Switch. Table 4 gives a short description of each one of them. Note that the same firmware is used for all the tests, loaded at test00.

Table 4: List of tests

Test	Short Description	Operator's Intervention
00	Flash PTS firmware	Yes
01	DDR2 test	No
02	Hwinfo edit and install	(Yes)
03	Init hardware test	No
04	CPU-FPGA bridge test	No
05	Fans test	Yes
06	Leds test	Yes
07	General button test	Yes
08	SFP lines test	Yes
09	Voltage levels check	No
10	Dataflash test	No
11	NAND test	No
12	AD9516 test	No
13	Internal clocks check	No
14	SMC connectors test	No
15	USB ports + RS232 port test	No
16	Temperatures test	No
17	Flash final firmware	No

4. Log files retrieval

Log files with detailed descriptions of the tests are automatically generated and archived in a .zip file called: zip_run_<run id>_<timestamp>_ WRS_<serial number>.zip.

The log files need to be delivered to CERN after completing the tests for all of the boards. To do so, please follow the instructions below:

- Plug the USB memory key in to the computer.
- Wait until Ubuntu mounts automatically the device.
- Using the file explorer navigate to **~/pts/log_wrs/ directory.**
- Select all the .zip files, right click and select copy.
- Using the file explorer, click on the USB device that appeared on the left column, right click and selecting paste.
- Click on the eject button on the left of the file explorer window and remove the USB key.
- Transfer the data to another computer with Internet access.
  Finally, send the .zip file by email to the responsible of tests at CERN.

5. Custom loopback preparation

Before first setup a custom SFP adapter must be prepared. Schematics are shown below.

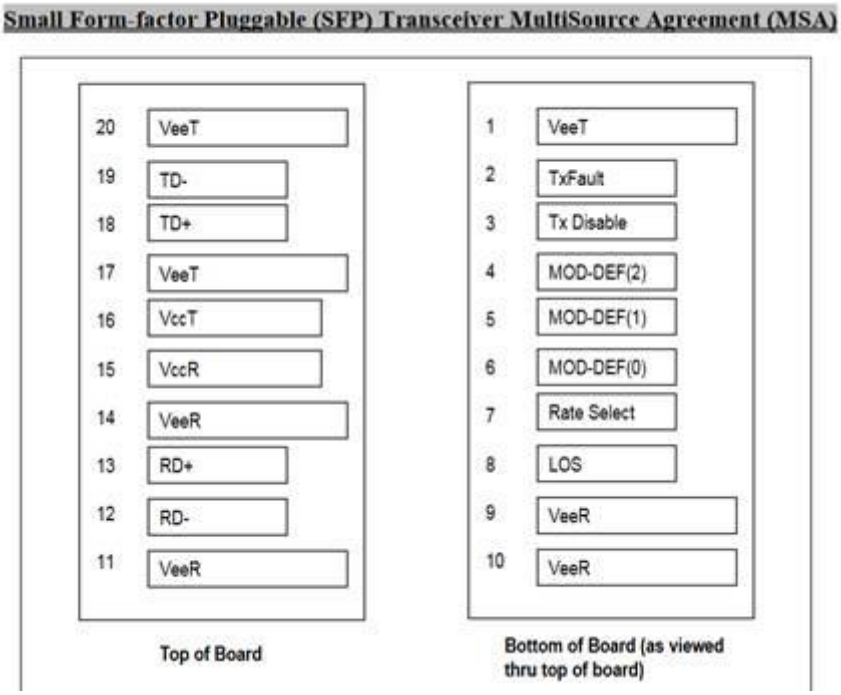


Figure 8: SFP pinout

Pin 3 (Tx Disable) should be connected to pin 6 (MOD-DEF(0))

See Figure 3: Custom SFP loopback for an example.

6. First Time Setup

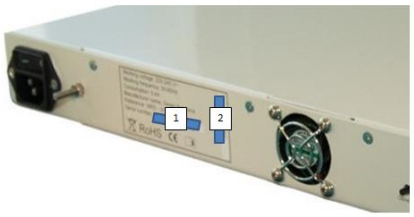
The following list explains how to setup the environment for the first time.

1) Plug all the USB cables with connector A (6x) into available USB slots of the provided computer. Eventually use a usb hub to extend the number of ports as at least 9 ports are needed.
2) Plug the USB cables with mini B connectors (3x) into the WRS/DUT.
3) Plug the USB cable with B connector into the Pendulum.
4) Connect the Agilent with an RS232 cross-cable to an USB-RS232 converter
5) Power up the Pendulum and Agilent.
6) Connect the straight RS232 cable to the other USB-RS232 converter and the WRS/DUT.
7) Connect the Ethernet cable between the PC and the WRS/DUT.
8) Connect 2 SMC-BNC cables from the CLK 1/2 of the WRS/DUT to the Pendulum A/B.
9) Connect the other SMC-BNC cable from the Agilent output to the 10MHz of the WRS/DUT.
10) Connect the SMC-SMC cable between the PPS in and output.
11) Power up the WRS/DUT
12) Plug the barcode-reader into an available USB slot of the computer.
13) Connect the monitor, keyboard and mouse to the computer.
14) Power up the PC.
15) Follow instructions from ~/pts/test/wrs/doc/ubuntu_setup_note.txt
16) Copy the startfiles (wrs.sh / wrs-non_destructive.sh/wrs-select.sh) from ~/pts/test/wrs to ~/pts/
17) Check in ~/pts/test/wrs/python/utilfunctions.py the USB vendor/device ID's for the USB-RS232 converters

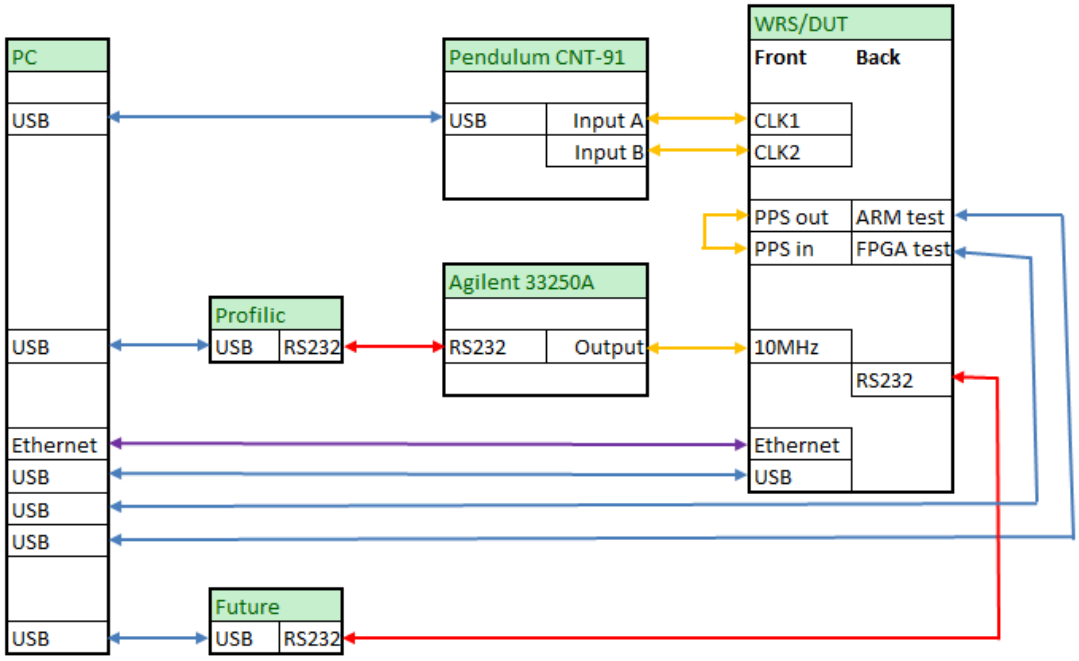
7. Testing Procedure

Place the ESD strap on your wrist.

Put the (barcode) stickers on the backside of the WRS/DUT. In position 1 the WRS/DUT identifier, on position 2 the MAC addresses



Connect the cables according to schematic below



Switch ON the WRS/DUT.

- Verify that the “Power” LED on the WRS/DUT is ON and green. This will confirm that the WRS/DUT is properly powered on.
- If the LED is OFF or red there is a problem with the power supply.

Switch ON the Agilent and Pendulum	
After the computer has finished with the booting procedure: • Start the test by opening a terminal window and type cd ~/pts/ and ./wrs.sh or ./wrs-non_destructive.sh or ./wrs-select.sh • When asked, type the password: “baraka” and [ENTER]	
• The program asks for the barcode of the board. • Check that the cursor is on the terminal, press th button/trigger on the barcode reader. • The code will appear on the terminal. Press [**ENTER**]. • The program will ask for a second barcode, in case the manufacturer has a different serial number system. • Scan the second barcode and press [**ENTER**], or if there is none, just press [**ENTER**].	
The program will automatically execute tests 00 to 17. The non_destructive variant doesn’t execute 00/02/10/11/17 to prevent wear of the storage. The select variant let you choose the tests you want to execute. If the non-destructive or select variant is chosen please make sure the switch has booted from NFS.	
Tests 00/(02)/05/06/07/08 ask for the user‘s intervention. • Test 00 will ask to boot the switch into the bootloader • Test 02 will ask to enter data of the switch and the manufacturer (test00 used in sequence) • Test 05 will ask to check the fans • Test 06 will ask to check the leds • Test 07 will ask to press the general button • Test 08 will ask to plug the SFP loopback	
At the end the operator is informed of the results of all the tests and is asked if he wants to repeat the whole process. • If no error has occurred, type [**n**] and then [**ENTER**]. • In case of error, you could repeat the tests once by typing [**y**] and [**ENTER**].	

8. Building Gateware

You need to make sure that you have all the tools for the switch synthesis. You will need:

git - to download the sources from our official repository
hdlmake and make - to create a project file and run the synthesis
64-bit version of Xilinx ISE 14.5 or above - for the actual synthesis and bitstream generation

1. First you need to setup your environment
   /opt/Xilinx/<version>/ISE_DS/settings64.sh
   export XILINX=/opt/Xilinx/<version>/ISE_DS

2. Download the HDL sources
   git clone git://ohwr.org/white-rabbit/wr-switch-hdl.git
   cd wr-switch-hdl
   git checkout wr-switch-sw-pts
   git submodule init
   git submodule update

3. Generate SDB Metadata package with synthesis information
   cd top/pts_scb
   ./gen_sdbsyn.py --user <your name> --project WRS_18p --ver <ISE version>

4. Run the synthesis
   cd ../../syn/pts_scb

   a) If you use the ISYP version of hdlmake, run the hdlmake with proper arguments
   hdlmake --ise-proj --make-ise
   make

   b) If you use the version v2.1 of hdlmake, you need to add the following line to the Manifest.py file located in syn/pts_scb
   syn_tool="ise"

   and only then run the hdlmake (no arguments)
   hdlmake
   make

   This can take ~3 hours

9. Building Software

For building the software which will run on the CPU inside the WRS:

You need to make sure that you have all the tools for the switch synthesis. You will need:
git - to download the sources from our official repository
packages libncurses5-dev, byobu, m4, bison, flexm4

1. Download the SW sources
   git clone git://ohwr.org/white-rabbit/wr-switch-sw.git
   cd wr-switch-sw
   git checkout wr-switch-sw-pts

2. Run the compilation
   cd ..
   ./wr-switch-sw/build/wrs_build-all 2>&1 | tee logfile | grep "^20..-..-.. ..:"

For building the software which will run on the softcore inside the FPGA on the WRS:

You need to make sure that you have all the tools for the switch synthesis. You will need:
git - to download the sources from our official repository

1. Download the WRPC sources
   git clone git://ohwr.org/hdl-core-lib/wr-cores/wrpc-sw.git
   cd wrpc-sw
   git checkout wrpc-pts

2. Prepare environment
   export CROSS_COMPILE=/home/user/Downloads/wrs_pts/
   lm32_toolchain/lm32/bin/lm32-elf-

3. Apply config
   make wr_switch_defconfig

4. Compile
   make

10. Common Causes of Test Failure

Once the testing has finished, all the failed tests will be listed on the screen. Detailed information can be found in **~/pts/log_wrs/** where an detailed report per test is written. In the last lines there is an summary with an indication of the failed part.

Test 00

Flashes the test firmware into the WRS/DUT through the bootloader.

Common problems:

- wrs-firmware-pts.tar not correct
- USB ports or Ethernet port not functioning

Test 01

Tests the DDR2 memory and afterwards inserts a default hwinfo and boots the switch to NFS

Common problems:

- DDR2 memory soldering fault

Test 02

Let the user compose the hwinfo and installs it in the switch.

Common problems:

- Wrong pattern in user provided data

Test 03

Initializes all hardware interfaces later used for several tests.

Common problems:

- One of the hardware interfaces not correctly soldered, check log for specific part indication

Test 04

Tests the FPGA-CPU address and datalines.

Common problems:

- Address and/or datalines are not connected or open or shorted

Test 05

Tests the fans and the control of the fans.

Common problems:
- Fans not working
- Control lines not connected

Test 06

Tests the leds in all possible modes.

Common problems:
- I2C problems
- Leds faulty

Test 07

Tests the general button which is situated on the backside of the WRS/DUT.

Common problems:
- Button stuck or not connected

Test 08

Tests the SFP lines.

Common problems:
- SFP loopback not correctly modified
- SFP connections not ok

Test 09

Tests the voltage levels.

Common problems:
- Power supply not ok

Test 10

Tests the dataflash.

Common problems:
- Bad sectors
- Bad connections

Test 11

Tests the nand.

Common problems:
- Bad sectors
- Bad connections

Test 12

Tests the ad9516 PLL.

Common problems:
- Command interface to pll not ok

Test 13

Checks the internal clocks.

Common problems:
- Internal clock circuitry not ok, check log which clock was faulty

Test 14

Tests the SMC connectors situated at the front of the WRS/DUT

Common problems:
- SMC connector not ok
- Test cable not prepared well
- Agilent or Pendulum not connected or switched on

Test 15

Tests the USB/RS232 ports on the WRS/DUT.

Common problems:
- Wrong vendor/device id's in utilfunctions.py
- Not all ports connected

Test 16

Tests the temperature sensors inside the WRS/DUT.

Common problems:
- Fans not ok
- I2C problem
- Sensor problem

Test 17

Flashes the final firmware into the WRS/DUT through update partition.

Common problems:

- wrs-firmware-final.tar not correct

11. Hardware coverage of PTS

Power_Supplies

+5VCC_IN

Net	Validated	Through	Controlled	Through
+5VCC_IN	SYST_MON_P7	XC6VLX (B12)		

+1V8 and +2V5

IC47 TPS53126RGET

Net	Validated	Through	Controlled	Through
+1V8	SYST_MON_P4	XC6VLX (H12)		
+2V5	VCCAUX	XC6VLX (internal)		

+1V0 and +1V5

IC46 TPS53126RGET

Net	Validated	Through	Controlled	Through
+1V0	VCCINT	XC6VLX (internal)		
+1V5	SYST_MON_P3	XC6VLX (G11)		

+3V3

IC48 AP7173

Net	Validated	Through	Controlled	Through
+3V3	SYST_MON_P2 +3V3_PG	XC6VLX (F14) XC6VLX (AJ15)		

+3V3_PLL

IC35 AP7173

Net	Validated	Through	Controlled	Through
+3V3_PLL	+3V3_PLL_PG	XC6VLX (AF15)		

+2V5_PLL

IC34 AP7173

Net	Validated	Through	Controlled	Through
+2V5_PLL	+2V5_PLL_PG	XC6VLX (AK14)		

+1V2_GTX

IC32 AP7173

Net	Validated	Through	Controlled	Through
+1V2_GTX	SYST_MON_P6	XC6VLX (E13)		

	+1V2_GTX_PG	XC6VLX (AJ14)		

+1V0_GTX

IC39 AP7173

Net	Validated	Through	Controlled	Through
+1V0_GTX	SYST_MON_P5 +1V0_GTX_PG	XC6VLX (A11) XC6VLX (AG15)		

+3V0_VM53

IC44 MCP1802T

Net	Validated	Through	Controlled	Through
+3V0_VM53	CLK_25MHZ_GTX_DAC	AD9516-4 (REF1)	+3V0_VM53_EN	XC6VLX (AN15)

+3V0_OSC

IC38 MCP1802T

Net	Validated	Through	Controlled	Through
+3V0_OSC	CLK_25MHZ_GTX_DAC CLK_25MHZ_DMTD_DAC	AD9516-4 (REF1) CDCM61002RHBT		

Clocks

PPS

IC1 SN74LVT125DW

Net	Validated	Through	Controlled	Through
EXTPPSIN	SMC connector PPS IN	XC6VLX (J25)	SMC connector PPS OUT	XC6VLX (U23)
EXTPPSOUT	SMC connector PPS IN	XC6VLX (J25)	SMC connector PPS OUT	XC6VLX(U23)

Externally EXTPPSIN is connected to EXTPPSOUT to test both circuits.

Not tested: TERM_EN is not used and not connected.

10MHz input

IC11 ADCMP600BRJZ-R2

Net	Validated	Through	Controlled	Through
EXTREFIN_10M	CLK10MHZ_EXT CLK10MHZ_EXT	XC6VLX (K13)	SMC connector 10MHz IN	Agilent 33250A

Externally a 10MHz reference has to be connected from the Agilent 33250A.

10MHz output

U1 MC100EP52DR2

IC9 ICS83023I

Net	Validated	Through	Controlled	Through
SYNC_OUT	SMC connector CLK2 OUT	Pendulum CNT-91	SYNC_DATA_P	XC6VLX (B20)
			SYNC_DATA_N	XC6VLX (C19)
			SYNC_CLK_P	AD9516-4 (OUT4)
			SYNC_CLK_N	

By default SYNC_OUT will be the 10MHz reference output clock which is validated by the Pendulum CNT-91

DMTD clock

IC8 AD5662BRJ

IC7 FRETHE025

IC13 CDCM61002RHBT

Net	Validated	Through	Controlled	Through
CLK_25MHZ_DMTD_DAC	DMTD_CLK_P	XC6VLX (L23)		
	DMTD_CLK_N	XC6VLX (M22)		
DAC_DMTD_SYNC				XC6VLX (AD17)
DAC_DMTD_SCLK				XC6VLX (AC15)
DAC_DMTS_DIN				XC6VLX (AH17)

Not tested: DMTDCLK_mB_P/N

25MHz GTX clock

IC5 AD5662BRJ

IC4 VM53S3

Net	Validated	Through	Controlled	Through
CLK_25MHZ_GTX_DAC		AD9516-4 (REF1)		
DAC_REF_SYNC				XC6VLX (AM17)
DAC_REF_SCLK				XC6VLX (AN17)
DAC_REF_DIN				XC6VLX (AP17)

25MHz FPGA main clock

IC22 FNETHE025

IC21 DS90LV011ATMF

Net	Validated	Through	Controlled	Through
FPGA_MAIN_CLK_P		XC6VLX (K24)		
FPGA_MAIN_CLK_N		XC6VLX (K23)		

Clock distribution

IC16 AD9516-4BCPZ

IC12 MC100LVEP14DT

Net	Validated	Through	Controlled	Through
AUX_CLK_P		XC6VLX (A10)		AD9516 (OUT3)
AUX_CLK_N		XC6VLX (B10)		
SYNC_CLK_P	SMC connector CLK2 OUT	Pendulum CNT-91		AD9516 (OUT4)
SYNC_CLK_N				
SERDES_CLK_P		XC6VLX (F21)		AD9516 (OUT5)
SERDES_CLK_N		XC6VLX (G20)		
REF_CLK_P		XC6VLX (J9)		AD9516 (OUT6)
REF_CLK_N		XC6VLX (H9)		
MGTREFCLK116_P		XC6VLX (H6)	CLKEN CLK1_SEL	XC6VLX (AD16) XC6VLX (AK17) AD9516 (OUT7) AD9516 (OUT8)
MGTREFCLK116_N		XC6VLX (H5)		
MGTREFCLK115_P		XC6VLX (P6)		
MGTREFCLK115_N		XC6VLX (P5)		
MGTREFCLK114_P		XC6VLX (V6)		
MGTREFCLK114_N		XC6VLX (V5)		
MGTREFCLK113_P		XC6VLX (AD6)		
MGTREFCLK113_N		XC6VLX (AD5)		
MGTREFCLK112_P		XC6VLX (AK6)		
MGTREFCLK112_N		XC6VLX (AK5)		
PLL_CLK_OUT	SMC connector CLK1 OUT	Pendulum CNT-91		AD9516 (OUT9)

PLL_SYNC				XC6VLX (AG18)
PLL_CS				XC6VLX (AK18)
PLL_SDI				XC6VLX (AH19)
PLL_SDO		XC6VLX (AJ19)		
PLL_SCLK				XC6VLX (AE16)
PLL_STAT		XC6VLX (AD15)		
PLL_LOCK		XC6VLX (AF18)		
PLL_REFSEL				XC6VLX (AK16)
PLL_RESET				XC6VLX (AL16)

Not tested: uTCA_TONGUE2_CLK1_P/N, uTCA_TONGUE2_CLK2_P/N, miniBACKPLANE_CLK_P/N.

RS232 and USB ports

ARM Management USB (Front)

J2 QSS-048-01-L-D-DP

mB: J2 QTS-048-04-L-D-DP

miniBackplane: IC1 PRTR5V0U2X, J6 USB Mini

Net	Validated	Through	Controlled	Through
USB_DDP_P			USB_DDP_P	AT91SAM (V15/U15)
USB_DDP_N			USB_DDP_N	AT91SAM (V16/U16)
USB_5VBus			USB_5VBus	AT91SAM (T12)

Not tested: USB_HDP_P/N

FPGA UART (USB) (Rear)

J1 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP

mB: IC2 CP2102-GM, IC3 PRTR5V0U2X, J9 USB Mini

Net	Validated	Through	Controlled	Through
FPGA_RXD				XC6VLX (D11)
FPGA_TXD				XC6VLX (E11)

ARM UART (USB) (Rear)

J1 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP

mB: IC8 CP2102-GM, IC9 PRTR5V0U2X, J4 USB Mini

Net	Validated	Through	Controlled	Through
ARM_DBG_RX			DBG_TXD	AT91SAM (R6)
ARM_DBG_TX			DBG_RXD	AT91SAM (P6)

RS232 Management (Rear)

J2 QSS-048-01-L-D-DP

mB: J2 QTS-048-04-L-D-DP

IC31 MAX3232CDBR, J3 D-SUB9

Net	Validated	Through	Controlled	Through
RS232_MNG_TXD				AT91SAM (R5)
RS232_MNG_RXD				AT91SAM (V4)

FPGA RS232 (Internal)

IC31 MAX3232CDBR, P2 MHDR2X3

Net	Validated	Through	Controlled	Through
FPGA_RS232_RXD		XC6VLX (AP16)		
FPGA_RS232_TXD				XC6VLX (AJ17)

Not tested. A jumper must be placed on P2 between pin 4 and pin 6.

Memories

Serial Boot Flash

IC25 AT45DB642D-CNU

Net	Validated	Through	Controlled	Through
SPI_SO			SPI0_MISO	AT91SAM (T4)
SPI_SI			SPI0_MOSI	AT91SAM (V2)
SPI_SCK			SPI0_SPCK	AT91SAM (V3)
SPI_CS			SPI0_NPCS0	AT91SAM (U4)

NAND Flash

IC30 MT29F4G16ABBDAHC:D TR, IC26 SN74LVC1G32

Net	Validated	Through	Controlled	Through
NAND_CE				AT91SAM (F8)
NAND_CLE				AT91SAM (A7)
NAND_ALE				AT91SAM (F9)
NAND_OE				AT91SAM (D10)
NAND_WE				AT91SAM (E10)
NAND_RB				AT91SAM (E8)
NAND_D[15:0]			EBI1_D[15:0]	AT91SAM

Not tested: ARM_BOOT_SEL_GPIO, FBOOT_SEL

DDR2

IC50 MT47H32M16HR-25E:G

RP15, RP16, RP17, RP18, RP19, RP20 27Rx8

Net	Validated	Through	Controlled	Through
DDR_D[15:0]			EBI0_D[15:0]	AT91SAM
DDR_A[12:0]			EBI0_A[12:0]	AT91SAM
DDR_BA[1:0]			EBI0_BA[1:0]	AT91SAM
DDR_CKE			EBI0_CKE	AT91SAM
DDR_CLK_P			EBI0_CLK_P	AT91SAM
DDR_CLK_N			EBI0_CLK_N	AT91SAM
DDR_CS			EBI0_CS	AT91SAM
DDR_RAS			EBI0_RAS	AT91SAM
DDR_CAS			EBI0_CAS	AT91SAM
DDR_WE			EBI0_WE	AT91SAM
DDR_DQM[1:0]			EBI0_DQM[1:0]	AT91SAM
DDR_DQS[1:0]			EBI0_DQS[1:0]	AT91SAM
DDR_VREF			+1V8	

Ethernet

CN1 Tyco 1888250-1, Tr1 TR_H1260NL, IC41 LAN8720A-CP, IC40 FNETHE025

Net	Validated	Through	Controlled	Through
TX_P TX_N			TXD0	AT91SAM (M5)
			TXD1	AT91SAM (P1)
			TX_CLK	AT91SAM (N6)
			TX_EN	AT91SAM (M6)
RX_P RX_N			RXD0	AT91SAM (N3)
			RXD1	AT91SAM (P2)
			RX_ER	AT91SAM (N5)
			CRS_DV	AT91SAM (N4)
MDC				AT91SAM (R1)
MDIO				AT91SAM (P3)
nRST				AT91SAM (U1)
LED_ACT	Observation			
LED_SPEED	Observation			

FPGA

FPGA Configuration

Net	Validated	Through	Controlled	Through
FPGA_DIN			TK0	AT91SAM (R7)
FPGA_CCLK			TD0	AT91SAM (L8)
FPGA_INIT_B		AT91SAM (N1)		
FPGA_DONE				AT91SAM (L5)
ARM_PROGRAM_B				AT91SAM (L6)
ARM_FPGA_RESET		XC6VLX (M10)		AT91SAM (M2)

Not tested: ARM_IRQ , ARM_FIQ , ARM_NRST, EXT_PROGRAM_B

CPU FPGA EBI

Net	Validated	Through	Controlled	Through
EBI1_D[31:0]		XC6VLX		AT91SAM
EBI1_A[20:2]		XC6VLX		AT91SAM
EBI1_NCS0		XC6VLX (H34)		AT91SAM (A10)
EBI1_NRD		XC6VLX (J31)		AT91SAM (F11)
EBI1_NWE		XC6VLX (M25)		AT91SAM (C9)
EBI1_NBS0/A0		XC6VLX (J30)		AT91SAM(F13)
EBI1_NBS1		XC6VLX (P29)		AT91SAM (D9)
EBI1_NBS2/A1		XC6VLX (H30)		AT91SAM (F14)
EBI1_NBS3		XC6VLX (J34)		AT91SAM (A9)
EBI1_NWAIT		XC6VLX (R26)		AT91SAM (C6)

Not tested: EBI1_NBS0/A0, EBI1_NBS1, EBI1_NBS2/A1, EBI1_NBS3

CPU FPGA SPI

Net	Validated	Through	Controlled	Through
SPI1_MISO			SPI1_MISO	AT91SAM (M7)
SPI1_MOSI			SPI1_MOSI	AT91SAM (V5)
SPI1_SPCK			SPI1_SPCK	AT91SAM (T6)
SPI1_NPCS0			SPI1_NPCS0	AT91SAM (U6)

Temperature and diagnostics

SCB Temperature

IC20, IC19, IC18, IC17 TMP100

Net	Validated	Through	Controlled	Through
SCL_TMP		XC6VLX (G13)		
SDA_TMP		XC6VLX (H14)		

FAN

J1 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP

mB: Q2 DMN2020LSN-7, Q4 DMP2066LSN-7

mB: Q1 DMN2020LSN-7, Q3 DMP2066LSN-7

Net	Validated	Through	Controlled	Through
FAN_BOX_EN				XC6VLX (C12)
FAN_PSU_EN				XC6VLX (D12)

miniBackplane Temperature

J2 QSS-048-01-L-D-DP

mB: J2 QTS-048-04-L-D-DP

mB: IC7 TMP101

Net	Validated	Through	Controlled	Through
I2C_IOs_SDA0			FPGA_GPIO36	XC6VLX (AG32)
I2C_IOs_SCL0			FPGA_GPIO37	XC6VLX (AF31)

miniBackplane Status LEDs (Front)

J2 QSS-048-01-L-D-DP

mB: J2 QTS-048-04-L-D-DP

mB: U1 PCA9554PW, LD5 LEDs

Net	Validated	Through	Controlled	Through
I2C_IO_SDA	Observation		ARM_3V3_GPIO_PB6 PB4	AT91SAM (N12) PB24
I2C_IO_SCL	Observation		ARM_3V3_GPIO_PB7 PB0	AT91SAM (P12) PB20
I2C_IO_INT	Observation		ARM_2V5_GPIO_PD13 RF1	AT91SAM (M9) PD15/RF1

miniBackplane Power LEDs (Front)

mB: Q5 DMN2020LSN-7, LD6 LEDs

Net	Validated	Through	Controlled	Through
mB:+3V3	Observation			
mB:+12VCC_IN	Observation			

miniBackplane Flash Button (Rear)

mB: S3 MCDTSA6, P1 Boot_Button

Net	Validated	Through	Controlled	Through
SPI_SO			SPI0_MISO	AT91SAM (T4)

The miniBackplane S3 button is connected via a cable to SPI_SO and can pull SPI_SO to GND. After a reset and during the push of the button the AT91SAM will read only zeros from the boot flash triggering a different boot mode to be able to program the flash.

miniBackplane Generic Button (Rear)

mB: S2 MCDTSA6

Net	Validated	Through	Controlled	Through
ARM_2V5_GPIO_PD14			PE9	AT91SAM (H7)

WR Links

WR Link 0

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J8-1 SFP Module socket, U3-1 PCA9554PW, LD1-1 LEDs, LD2-1 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK0_LOS_TX_FAULT	FPGA_GPIO35	XC6VLX (AB26)		
WR_LINK0_TD_IN_P			MGTTX112_0	XC6VLX
WR_LINK0_TD_IN_N				
WR_LINK0_RD_OUT_P				
WR_LINK0_RD_OUT_N				
WR_LINK0_DETECT	PE2	AT91SAM (G5)		
WR_LINK0_SCL	WR_DL_SCL1	mB:IC5 (SD7)	PB5	AT91SAM (M12)
WR_LINK0_SDA	WR_DL_SDA1	mB:IC5 (SC7)	PB7	AT91SAM (M13)
WR_LINK0_LED_ACTIVITY	Observation		FPGA_GPIO34	XC6VLX (AG33)
WR_LINK0_LED_LINK	Observation	mB: U3-1 (I/O6)	I2C_IOs_SCL1	XC6VLX (AC25)
WR_LINK0_LED_SYNED	Observation	mB: U3-1 (I/O5)	I2C_IOs_SDA1	XC6VLX (AG31)
WR_LINK0_LED_WRMODE	Observation	mB: U3-1 (I/O4)		
SFP1_TX_DISABLE		mB: U3-1 (I/O7)		

WR Link 1

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J10-1 SFP Module socket, U3-1 PCA9554PW, LD3-1 LEDs, LD4-1 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK1_LOS_TX_FAULT	FPGA_GPIO10	XC6VLX (AA33)		
WR_LINK1_TD_IN_P			MGTTX112_1	XC6VLX
WR_LINK1_TD_IN_N				
WR_LINK1_RD_OUT_P				
WR_LINK1_RD_OUT_N				
WR_LINK1_DETECT	PE13	AT91SAM (H4)		
WR_LINK1_SCL	WR_DL_SCL0	mB:IC5 (SD6)	PB5	AT91SAM (M12)
WR_LINK1_SDA	WR_DL_SDA0	mB:IC5 (SC6)	PB7	AT91SAM (M13)
WR_LINK1_LED_ACTIVITY	Observation		FPGA_GPIO33	XC6VLX (AC28)
WR_LINK1_LED_LINK	Observation	mB: U3-1 (I/O0)	I2C_IOs_SCL1	XC6VLX (AC25)
WR_LINK1_LED_SYNED	Observation	mB: U3-1 (I/O3)	I2C_IOs_SDA1	XC6VLX (AG31)
WR_LINK1_LED_WRMODE	Observation	mB: U3-1 (I/O1)		
SFP0_TX_DISABLE		mB: U3-1 (I/O2)		

WR Link 2

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J8-2 SFP Module socket, U3-2 PCA9554PW, LD1-2 LEDs, LD2-2 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK2_LOS_TX_FAULT	FPGA_GPIO32	XC6VLX (AF33)		
WR_LINK2_TD_IN_P			MGTTX112_2	XC6VLX
WR_LINK2_TD_IN_N				
WR_LINK2_RD_OUT_P				
WR_LINK2_RD_OUT_N				
WR_LINK2_DETECT	PE6	AT91SAM (G3)		
WR_LINK2_SCL	WR_DL_SCL3	mB:IC5 (SD5)	PB5	AT91SAM (M12)
WR_LINK2_SDA	WR_DL_SDA3	mB:IC5 (SC5)	PB7	AT91SAM (M13)
WR_LINK2_LED_ACTIVITY	Observation		FPGA_GPIO31	XC6VLX (AE32)
WR_LINK2_LED_LINK	Observation	mB: U3-2 (I/O6)	I2C_IOs_SCL1 I2C_IOs_SDA1	XC6VLX (AC25) XC6VLX (AG31)
WR_LINK2_LED_SYNED	Observation	mB: U3-2 (I/O5)		
WR_LINK2_LED_WRMODE	Observation	mB: U3-2 (I/O4)		
SFP1_TX_DISABLE		mB: U3-2 (I/O7)		

WR Link 3

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J10-2 SFP Module socket, U3-2 PCA9554PW, LD3-2 LEDs, LD4-2 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK3_LOS_TX_FAULT	FPGA_GPIO9	XC6VLX (AA34)		
WR_LINK3_TD_IN_P			MGTTX112_3	XC6VLX
WR_LINK3_TD_IN_N				
WR_LINK3_RD_OUT_P				
WR_LINK3_RD_OUT_N				
WR_LINK3_DETECT	PE14	AT91SAM (J3)		
WR_LINK3_SCL	WR_DL_SCL2	mB:IC5 (SD4)	PB5	AT91SAM (M12)
WR_LINK3_SDA	WR_DL_SDA2	mB:IC5 (SC4)	PB7	AT91SAM (M13)
WR_LINK3_LED_ACTIVITY	Observation		FPGA_GPIO30	XC6VLX (AD31)
WR_LINK3_LED_LINK	Observation	mB: U3-2 (I/O0)	I2C_IOs_SCL1 I2C_IOs_SDA1	XC6VLX (AC25) XC6VLX (AG31)
WR_LINK3_LED_SYNED	Observation	mB: U3-2 (I/O3)		
WR_LINK3_LED_WRMODE	Observation	mB: U3-2 (I/O1)		
SFP0_TX_DISABLE		mB: U3-12(I/O2)		

WR Link 4

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J8-3 SFP Module socket, U3-3 PCA9554PW, LD1-3 LEDs, LD2-3 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK4_LOS_TX_FAULT	FPGA_GPIO29	XC6VLX (AD30)		
WR_LINK4_TD_IN_P			MGTTX113_0	XC6VLX
WR_LINK4_TD_IN_N				
WR_LINK4_RD_OUT_P				
WR_LINK4_RD_OUT_N				
WR_LINK4_DETECT	PE0	AT91SAM (G4)		
WR_LINK4_SCL	WR_DL_SCL5	mB:IC5 (SD3)	PB5	AT91SAM (M12)
WR_LINK4_SDA	WR_DL_SDA5	mB:IC5 (SC3)	PB7	AT91SAM (M13)
WR_LINK4_LED_ACTIVITY	Observation		FPGA_GPIO28	XC6VLX (AC32)
WR_LINK4_LED_LINK	Observation	mB: U3-3 (I/O6)	I2C_IOs_SCL1	XC6VLX (AC25)
WR_LINK4_LED_SYNED	Observation	mB: U3-3 (I/O5)	I2C_IOs_SDA1	XC6VLX (AG31)
WR_LINK4_LED_WRMODE	Observation	mB: U3-3 (I/O4)		
SFP1_TX_DISABLE		mB: U3-3 (I/O7)		

WR Link 5

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J10-3 SFP Module socket, U3-3 PCA9554PW, LD3-3 LEDs, LD4-3 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK5_LOS_TX_FAULT	FPGA_GPIO8	XC6VLX (AB32)		
WR_LINK5_TD_IN_P			MGTTX113_1	XC6VLX
WR_LINK5_TD_IN_N				
WR_LINK5_RD_OUT_P				
WR_LINK5_RD_OUT_N				
WR_LINK5_DETECT	PE12	AT91SAM (J5)		
WR_LINK5_SCL	WR_DL_SCL4	mB:IC5 (SD2)	PB5	AT91SAM (M12)
WR_LINK5_SDA	WR_DL_SDA4	mB:IC5 (SC2)	PB7	AT91SAM (M13)
WR_LINK5_LED_ACTIVITY	Observation		FPGA_GPIO27	XC6VLX (AC29)
WR_LINK5_LED_LINK	Observation	mB: U3-3 (I/O0)	I2C_IOs_SCL1	XC6VLX (AC25)
WR_LINK5_LED_SYNED	Observation	mB: U3-3 (I/O3)	I2C_IOs_SDA1	XC6VLX (AG31)
WR_LINK5_LED_WRMODE	Observation	mB: U3-3 (I/O1)		
SFP0_TX_DISABLE		mB: U3-3 (I/O2)		

WR Link 6

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J8-4 SFP Module socket, U3-4 PCA9554PW, LD1-4 LEDs, LD2-4 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK6_LOS_TX_FAULT	FPGA_GPIO26	XC6VLX (AB31)		

WR_LINK6_TD_IN_P			MGTTX113_2	XC6VLX
WR_LINK6_TD_IN_N				
WR_LINK6_RD_OUT_P				
WR_LINK6_RD_OUT_N				
WR_LINK6_DETECT	PE5	AT91SAM (H5)		
WR_LINK6_SCL	WR_DL_SCL7	mB:IC5 (SD1)	PB5	AT91SAM (M12)
WR_LINK6_SDA	WR_DL_SDA7	mB:IC5 (SC1)	PB7	AT91SAM (M13)
WR_LINK6_LED_ACTIVITY	Observation		FPGA_GPIO25	XC6VLX (AA30)
WR_LINK6_LED_LINK	Observation	mB: U3-4 (I/O6)	I2C_IOs_SCL1 I2C_IOs_SDA1	XC6VLX (AC25) XC6VLX (AG31)
WR_LINK6_LED_SYNED	Observation	mB: U3-4 (I/O5)		
WR_LINK6_LED_WRMODE	Observation	mB: U3-4 (I/O4)		
SFP1_TX_DISABLE		mB: U3-4 (I/O7)		

WR Link 7

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J10-4 SFP Module socket, U3-4 PCA9554PW, LD3-4 LEDs, LD4-4 LEDs

Net	**Validated**	**Through**	**Controlled**	**Through**
WR_LINK7_LOS_TX_FAULT	FPGA_GPIO7	XC6VLX (AB33)		
WR_LINK7_TD_IN_P			MGTTX113_3	XC6VLX
WR_LINK7_TD_IN_N				
WR_LINK7_RD_OUT_P				
WR_LINK7_RD_OUT_N				
WR_LINK7_DETECT	PE10	AT91SAM (H8)		
WR_LINK7_SCL	WR_DL_SCL6	mB:IC5 (SD0)	PB5	AT91SAM (M12)
WR_LINK7_SDA	WR_DL_SDA6	mB:IC5 (SC0)	PB7	AT91SAM (M13)
WR_LINK7_LED_ACTIVITY	Observation		FPGA_GPIO24	XC6VLX (AA29)
WR_LINK7_LED_LINK	Observation	mB: U3-4 (I/O0)	I2C_IOs_SCL1 I2C_IOs_SDA1	XC6VLX (AC25) XC6VLX (AG31)
WR_LINK7_LED_SYNED	Observation	mB: U3-4 (I/O3)		
WR_LINK7_LED_WRMODE	Observation	mB: U3-4 (I/O1)		
SFP0_TX_DISABLE		mB: U3-4 (I/O2)		

WR Link 8

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J8-5 SFP Module socket, U3-5 PCA9554PW, LD1-5 LEDs, LD2-5 LEDs

Net	**Validated**	**Through**	**Controlled**	**Through**
WR_LINK8_LOS_TX_FAULT	FPGA_GPIO23	XC6VLX (Y26)		
WR_LINK8_TD_IN_P			MGTTX114_0	XC6VLX
WR_LINK8_TD_IN_N				
WR_LINK8_RD_OUT_P				
WR_LINK8_RD_OUT_N				

WR_LINK8_DETECT	PE15	AT91SAM (J4)		
WR_LINK8_SCL	WR_DL_SCL9	mB:IC6 (SD7)	PB5	AT91SAM (M12)
WR_LINK8_SDA	WR_DL_SDA9	mB:IC6 (SC7)	PB7	AT91SAM (M13)
WR_LINK8_LED_ACTIVITY	Observation		FPGA_GPIO22	XC6VLX (AE31)
WR_LINK8_LED_LINK	Observation	mB: U3-5 (I/O6)	I2C_IOs_SCL1 I2C_IOs_SDA1	XC6VLX (AC25) XC6VLX (AG31)
WR_LINK8_LED_SYNED	Observation	mB: U3-5 (I/O5)		
WR_LINK8_LED_WRMODE	Observation	mB: U3-5 (I/O4)		
SFP1_TX_DISABLE		mB: U3-5 (I/O7)		

WR Link 9

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J10-5 SFP Module socket, U3-5 PCA9554PW, LD3-5 LEDs, LD4-5 LEDs

Net	**Validated**	**Through**	**Controlled**	**Through**
WR_LINK9_LOS_TX_FAULT	FPGA_GPIO6	XC6VLX (AC34)		
WR_LINK9_TD_IN_P			MGTTX114_1	XC6VLX
WR_LINK9_TD_IN_N				
WR_LINK9_RD_OUT_P				
WR_LINK9_RD_OUT_N				
WR_LINK9_DETECT	PD13/RK1	AT91SAM (L9)		
WR_LINK9_SCL	WR_DL_SCL8	mB:IC6 (SD6)	PB5	AT91SAM (M12)
WR_LINK9_SDA	WR_DL_SDA8	mB:IC6 (SC6)	PB7	AT91SAM (M13)
WR_LINK9_LED_ACTIVITY	Observation		FPGA_GPIO21	XC6VLX (AD29)
WR_LINK9_LED_LINK	Observation	mB: U3-5 (I/O0)	I2C_IOs_SCL1 I2C_IOs_SDA1	XC6VLX (AC25) XC6VLX (AG31)
WR_LINK9_LED_SYNED	Observation	mB: U3-5 (I/O3)		
WR_LINK9_LED_WRMODE	Observation	mB: U3-5 (I/O1)		
SFP0_TX_DISABLE		mB: U3-5 (I/O2)		

WR Link 10

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J8-6 SFP Module socket, U3-6 PCA9554PW, LD1-6 LEDs, LD2-6 LEDs

Net	**Validated**	**Through**	**Controlled**	**Through**
WR_LINK10_LOS_TX_FAULT	FPGA_GPIO20	XC6VLX (AB28)		
WR_LINK10_TD_IN_P			MGTTX114_2	XC6VLX
WR_LINK10_TD_IN_N				
WR_LINK10_RD_OUT_P				
WR_LINK10_RD_OUT_N				
WR_LINK10_DETECT	PE11	AT91SAM (G8)		
WR_LINK10_SCL	WR_DL_SCL11	mB:IC6 (SD5)	PB5	AT91SAM (M12)
WR_LINK10_SDA	WR_DL_SDA11	mB:IC6 (SC5)	PB7	AT91SAM (M13)
WR_LINK10_LED_ACTIVITY	Observation		FPGA_GPIO19	XC6VLX (AC27)

WR_LINK10_LED_LINK	Observation	mB: U3-6 (I/O6)	I2C_IOs_SCL1 I2C_IOs_SDA1	XC6VLX (AC25) XC6VLX (AG31)
WR_LINK10_LED_SYNED	Observation	mB: U3-6 (I/O5)		
WR_LINK10_LED_WRMODE	Observation	mB: U3-6 (I/O4)		
SFP1_TX_DISABLE		mB: U3-6 (I/O7)		

WR Link 11

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J10-6 SFP Module socket, U3-6 PCA9554PW, LD3-6 LEDs, LD4-6 LEDs

Net	**Validated**	**Through**	**Controlled**	**Through**
WR_LINK11_LOS_TX_FAULT	FPGA_GPIO5	XC6VLX (AC33)		
WR_LINK11_TD_IN_P			MGTTX114_3	XC6VLX
WR_LINK11_TD_IN_N				
WR_LINK11_RD_OUT_P				
WR_LINK11_RD_OUT_N				
WR_LINK11_DETECT	PD11/RD1	AT91SAM (T8)		
WR_LINK11_SCL	WR_DL_SCL10	mB:IC6 (SD4)	PB5	AT91SAM (M12)
WR_LINK11_SDA	WR_DL_SDA10	mB:IC6 (SC4)	PB7	AT91SAM (M13)
WR_LINK11_LED_ACTIVITY	Observation		FPGA_GPIO18	XC6VLX (AB27)
WR_LINK11_LED_LINK	Observation	mB: U3-6 (I/O0)	I2C_IOs_SCL1 I2C_IOs_SDA1	XC6VLX (AC25) XC6VLX (AG31)
WR_LINK11_LED_SYNED	Observation	mB: U3-6 (I/O3)		
WR_LINK11_LED_WRMODE	Observation	mB: U3-6 (I/O1)		
SFP0_TX_DISABLE		mB: U3-6 (I/O2)		

WR Link 12

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J8-7 SFP Module socket, U3-7 PCA9554PW, LD1-7 LEDs, LD2-7 LEDs

Net	**Validated**	**Through**	**Controlled**	**Through**
WR_LINK12_LOS_TX_FAULT	FPGA_GPIO17	XC6VLX (AB25)		
WR_LINK12_TD_IN_P			MGTTX115_0	XC6VLX
WR_LINK12_TD_IN_N				
WR_LINK12_RD_OUT_P				
WR_LINK12_RD_OUT_N				
WR_LINK12_DETECT	PE3	AT91SAM (F5)		
WR_LINK12_SCL	WR_DL_SCL13	mB:IC6 (SD2)	PB5	AT91SAM (M12)
WR_LINK12_SDA	WR_DL_SDA13	mB:IC6 (SC2)	PB7	AT91SAM (M13)
WR_LINK12_LED_ACTIVITY	Observation		FPGA_GPIO16	XC6VLX (AA25)
WR_LINK12_LED_LINK	Observation	mB: U3-7 (I/O6)	I2C_IOs_SCL1 I2C_IOs_SDA1	XC6VLX (AC25) XC6VLX (AG31)
WR_LINK12_LED_SYNED	Observation	mB: U3-7 (I/O5)		
WR_LINK12_LED_WRMODE	Observation	mB: U3-7 (I/O4)		
SFP1_TX_DISABLE		mB: U3-7 (I/O7)		

WR Link 13

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J10-7 SFP Module socket, U3-7 PCA9554PW, LD3-7 LEDs, LD4-7 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK13_LOS_TX_FAULT	FPGA_GPIO4	XC6VLX (AD34)		
WR_LINK13_TD_IN_P			MGTTX115_1	XC6VLX
WR_LINK13_TD_IN_N				
WR_LINK13_RD_OUT_P				
WR_LINK13_RD_OUT_N				
WR_LINK13_DETECT	PD10/TD1	AT91SAM (U8)		
WR_LINK13_SCL	WR_DL_SCL12	mB:IC6 (SD3)	PB5	AT91SAM (M12)
WR_LINK13_SDA	WR_DL_SDA12	mB:IC6 (SC3)	PB7	AT91SAM (M13)
WR_LINK13_LED_ACTIVITY	Observation		FPGA_GPIO15	XC6VLX (AA26)
WR_LINK13_LED_LINK	Observation	mB: U3-7 (I/O0)	I2C_IOs_SCL1 I2C_IOs_SDA1	XC6VLX (AC25) XC6VLX (AG31)
WR_LINK13_LED_SYNED	Observation	mB: U3-7 (I/O3)		
WR_LINK13_LED_WRMODE	Observation	mB: U3-7 (I/O1)		
SFP0_TX_DISABLE		mB: U3-7 (I/O2)		

WR Link 14

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J8-8 SFP Module socket, U3-8 PCA9554PW, LD1-8 LEDs, LD2-8 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK14_LOS_TX_FAULT	FPGA_GPIO14	XC6VLX (AA28)		
WR_LINK14_TD_IN_P			MGTTX115_2	XC6VLX
WR_LINK14_TD_IN_N				
WR_LINK14_RD_OUT_P				
WR_LINK14_RD_OUT_N				
WR_LINK14_DETECT	PE4	AT91SAM (G7)		
WR_LINK14_SCL	WR_DL_SCL15	mB:IC6 (SD0)	PB5	AT91SAM (M12)
WR_LINK14_SDA	WR_DL_SDA15	mB:IC6 (SC0)	PB7	AT91SAM (M13)
WR_LINK14_LED_ACTIVITY	Observation		FPGA_GPIO13	XC6VLX (AC30)
WR_LINK14_LED_LINK	Observation	mB: U3-8 (I/O6)	I2C_IOs_SCL1 I2C_IOs_SDA1	XC6VLX (AC25) XC6VLX (AG31)
WR_LINK14_LED_SYNED	Observation	mB: U3-8 (I/O5)		
WR_LINK14_LED_WRMODE	Observation	mB: U3-8 (I/O4)		
SFP1_TX_DISABLE		mB: U3-8 (I/O7)		

WR Link 15

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J10-8 SFP Module socket, U3-8 PCA9554PW, LD3-8 LEDs, LD4-8 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK15_LOS_TX_FAULT	FPGA_GPIO3	XC6VLX (AD32)		
WR_LINK15_TD_IN_P			MGTTX115_3	XC6VLX
WR_LINK15_TD_IN_N				
WR_LINK15_RD_OUT_P				
WR_LINK15_RD_OUT_N				
WR_LINK15_DETECT	PD14/TF1	AT91SAM (U9)		
WR_LINK15_SCL	WR_DL_SCL14	mB:IC6 (SD1)	PB5	AT91SAM (M12)
WR_LINK15_SDA	WR_DL_SDA14	mB:IC6 (SC1)	PB7	AT91SAM (M13)
WR_LINK15_LED_ACTIVITY	Observation		FPGA_GPIO12	XC6VLX (AB30)
WR_LINK15_LED_LINK	Observation	mB: U3-8 (I/O0)	I2C_IOs_SCL1	XC6VLX (AC25)
WR_LINK15_LED_SYNED	Observation	mB: U3-8 (I/O3)	I2C_IOs_SDA1	XC6VLX (AG31)
WR_LINK15_LED_WRMODE	Observation	mB: U3-8 (I/O1)		
SFP0_TX_DISABLE		mB: U3-8 (I/O2)		

WR Link 16

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J8-9 SFP Module socket, U3-9 PCA9554PW, LD1-9 LEDs, LD2-9 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK16_LOS_TX_FAULT	FPGA_GPIO11	XC6VLX (AA31)		
WR_LINK16_TD_IN_P			MGTTX116_0	XC6VLX
WR_LINK16_TD_IN_N				
WR_LINK16_RD_OUT_P				
WR_LINK16_RD_OUT_N				
WR_LINK16_DETECT	PE8	AT91SAM (G6)		
WR_LINK16_SCL			PB1	AT91SAM (T15)
WR_LINK16_SDA			PB2	AT91SAM (R12)
WR_LINK16_LED_ACTIVITY		Observation	FPGA_GPIO2	XC6VLX (AE34)
WR_LINK16_LED_LINK	Observation	mB: U3-9 (I/O6)	I2C_IOs_SCL0	XC6VLX (AF31)
WR_LINK16_LED_SYNED	Observation	mB: U3-9 (I/O5)	I2C_IOs_SDA0	XC6VLX (AG32)
WR_LINK16_LED_WRMODE	Observation	mB: U3-9 (I/O4)		
SFP1_TX_DISABLE		mB: U3-9 (I/O7)		

WR Link 17

J1 QSS-048-01-L-D-DP, J2 QSS-048-01-L-D-DP

mB: J1 QTS-048-04-L-D-DP, J2 QTS-048-04-L-D-DP

mB: J10-9 SFP Module socket, U3-9 PCA9554PW, LD3-9 LEDs, LD4-9 LEDs

Net	Validated	Through	Controlled	Through
WR_LINK17_LOS_TX_FAULT	FPGA_GPIO0	XC6VLX (AF34)		

WR_LINK17_TD_IN_P			MGTTX116_1	XC6VLX
WR_LINK17_TD_IN_N				
WR_LINK17_RD_OUT_P				
WR_LINK17_RD_OUT_N				
WR_LINK17_DETECT	PD12/TK1	AT91SAM (V8)		
WR_LINK17_SCL			PB6	AT91SAM (U14)
WR_LINK17_SDA			PB3	AT91SAM (T16)
WR_LINK17_LED_ACTIVITY		Observation	FPGA_GPIO1	XC6VLX (AE33)
WR_LINK17_LED_LINK	Observation	mB: U3-9 (I/O0)	I2C_IOs_SCL0 I2C_IOs_SDA0	XC6VLX (AF31) XC6VLX (AG32)
WR_LINK17_LED_SYNED	Observation	mB: U3-9 (I/O3)		
WR_LINK17_LED_WRMODE	Observation	mB: U3-9 (I/O1)		
SFP0_TX_DISABLE		mB: U3-9 (I/O2)		

Not Tested

Schematic: SCB_CLKs (no way to test)

Not tested: TERM_EN is not used.

Schematic: RS232_and_USB_ports (no USB_HDP connected and internal access needed)

Not tested: USB_HDP_P/N

Not tested: FPGA RS232 internal

Schematic: CPU_EBI1_FPGA_Memory (not accessible and not connected)

Not tested: EBI1_NBS0/A0, EBI1_NBS1, EBI1_NBS2/A1, EBI1_NBS3

Not tested: ARM_BOOT_SEL_GPIO, FBOOT_SEL

Schematic: FPGA_GTX (not connected)

Not tested: MGTRX116_2_P/N, MGTTX116_2_P/N, MGTRX116_3_P/N, MGTTX116_3_P/N

Schematic: FPGA_Configuration (not mounted)

Not tested: ARM_IRQ , ARM_FIQ , ARM_NRST, EXT_PROGRAM_B

Schematic: CPU_IO_Ports (internal access needed and not mounted)

Not tested: D11, D12, D13, D14 LEDs

Not tested: TWCK, TWD, ARM _WD_INT,

Schematic: External Watchdogs (not mounted)

Not tested: FPGA_WD_SCL, FPGA_WD_SDA, FPGA_WD_INT, FPGA_WD_PROGRAM

Not tested: ARM_WD_SCL, ARM _WD_SDA, ARM _WD_INT, ARM _WD_RST

Schematic: FPGA_QDRII (not mounted)

Not tested: QDRII2_D[35:0], QDRII2_BWSz[3:0], QDRII2_A[18:0], QDRII2_CQ_P/N, QDRII2_K_P/N, QDRII2_DOFFz, QDRII2_WPSz, QDRII2_RPSz, QDRII2_Q[35:0]

Schematic: CPU_JTAG_Power_PLL (internal access needed and not mounted)

Not tested: JNTRST, JTDI, JTMS, JTCK, JRTCK, JTDO, JNRST

Not tested: CB3 Battery connector

Schematic: uTCA_Tongue3 (no uTCA testcrate)

Not tested: CN4 UTCA_MCH_TONGUE3

Not tested: TxFD1_P/N to TxFD6_P/N, RxFD1_P/N to RxFD6_P/N.

Schematic: Connectors (not mounted, not connected, internal access needed, internal access needed, no uTCA testcrate)

Not tested: MGTRX116_2_P/N, MGTTX116_2_P/N (mB: WR_LINK18_RD_OUT_P/N, WR_LINK18_TD_IN_P/N), MGTRX116_3_P/N, MGTTX116_3_P/N (mB: WR_LINK19_RD_OUT_P/N , WR_LINK19_TD_IN_P/N)

Not tested: FBOOT_SEL, EXT_NRST

Not tested: P6 Header 10X2, JNTRST, JTDI, JTMS, JTCK, JRTCK, JTDO, JNRST

Not tested: P5 Header 7X2, FPGA_TMS, FPGA_TCK, FPGA_TDO, FPGA_TDI

Not tested: CN2 KX15-20K4DE, uTCA_TONGUE2_CLK1_P/N, uTCA_TONGUE2_CLK2_P/N, miniBACKPLANE_CLK_P/N.

Schematic: SCB_PLLs (no uTCA testcrate)

Not tested: uTCA_TONGUE2_CLK1_P/N, uTCA_TONGUE2_CLK2_P/N, miniBACKPLANE_CLK_P/N.

Schematic: SMI_Link_7-12 (no SMI socket mounted)

Not tested: TxFD7_P/N to TxFD12_P/N, RxFD7_P/N to RxFD12_P/N.

Schematic: QDRII_mem (no QDR mounted)

Not tested: IC43, IC45, RP2, RP4, RP6, RP7, RP10, RP12, RP14.