

## WRS-4 Workshop, 26 June 2020:

(<https://www.ohwr.org/project/white-rabbit/wikis/New-WRS-4-Workshop>)

### Presentation #3

1. Did you have a look at the level of noise from different power supplies?

A: no

Be careful about the noise from the power supplies

2. Power consumption of SFP+ can be 2 W. Be careful about noise from power supplies to FPGAs/clocking

3. Chosen fans - do they have variable speed.

A: YES

4. Do we want to have fan-control chip on the FAN-module or in control from FPGA

- if we want to replace the fans when switch is running, we need to have a chip on the PCB

5- Life time of Fan connector - do we know how many times they can be reconnected

\* no study, we expect that they will be used few times

6. KM3NET

- will use modified main board of the WRS-4, so adding more ports to the PCB is not that important, what is important to have support in HDL, and use the same binary/bitstream for the release WRS-4 and the KM3NET version of hardware.

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### Presentation #5

6.1. For some people (metrology labs), alignment of internal time base to PPS rising edge, not 10MHz is important

- Doable with the proposed clocking schema

- TDC in FPGA, precision requirement between rising edge of 1PPS and 10MHz: ~100ps

7. What is limiting in the new WRS in terms of timing/noise performance

- limitation is FPGA

- Not true, local oscillators can improve

- 1s - contribution of transceiver and DDMTD, better local oscillator allows to filter the noise

8. Number of ports

- KM3Net: important is the HDL support, they will have different PCB, they want the same bitstream

- we should use cables for the output clock connectors to make more space in the front panel for SFPs

- cSFPs can host the regular SFPs, some of the ports could use cSFPs

- Use dedicated switching chip

- we considered this, we need two times more port in FPGA - in the current FPGA it would be OK as we have many GTHs, we could have max 24 ports with 48 GTHs

- it would be difficult to implement, we need to intercept traffic between SFP and the chip

- NDAs, non-open - the idea was discarded

- Have two FPGAs with fat-pipe between FPGAs
- We need to re-do the estimates of FPGA utilization for more ports
- Note: no need for 10Gb on all ports, only some will be 10Gb - this is interesting for the utilization
- Idea: gather data into 10GB stream in the extension board
- two ideas:
  - 18 x 1Gb, 6 x 10Gb -> it seems OK, except KM3Net
  - 20 x 1Gb, 4 x 10Gb -> it seems OK for all (KM3Net needs 18x1Gb ports to DOMs, 1x1Gb for aggregation)
- Idea: 10Gb -> only for aggregation, no timing -> not really good

#### 9. Clocking circuit

- Peter: as low phase noise as possible, you do not want to spoil the super reference with FPGA noise, WR clock outside FPGA and re-clock the noisy output of FPGA with it
- LMX2594 - is a deterministic PLL, used in SPEC7
- you can use DDMTD clock as bootstrap, this is done in SPEC7
- AUX input could be used for holdover
- Remark to Peter: you look only at GM, but even if we have very clean clock on GM, the Slave will add noise
- Any idea needs to be validated - this will be done with the clocking FMC for the current solution and SPEC7 might be used for evaluation of the solution proposed by Peter
- In Spec7, can you phase-shift the local timebase to align to PPS? Not when directly using 10MHz input
- If we keep synchronization on PPS, not 10MHz edge, 10MHz clock cannot be used directly
- Price to pay if you want direct feed, you need to check everything (all components) for determinism
- The FMC clocking could include some new ideas
- in metrology institutes, they need to anyway calibrate for cable lengths, so alignment with PPS is not that important

#### 10. Interfaces - PS should be 5v TTL

- it is important that all WR equipment have the same standard,
- 5V OK

#### 11. 10MHz out AC coupled - OK

#### 12. CP2105

- bad/breaks even with additional ESD diode
- is FT2232HL compatible with linux - yes

#### 13. Aqueezing Aux/Abscale

- OK
- use cables to place it above the others

#### 14. USB-C

- check robustness
- one can buy very robust USB-C connectors
- USB-B can become obsolete, thus better to use USB-C

#### 15. SSD disc

- using it to store standard distribution of Linux.... If someone wants
- might be useful to store external data
- possibly an overkill
- not mandatory
- leave pads for SATA on PCB and USB
- NVMe PCIe -> good solution

#### 16. Have USB connector inside to connect some additional sensors

#### 17. Dual QSPI -> for recovery, not programming FPGA

#### 18. Substrate

- check what is used in evaluation boards of Xilinx
- the one suggested (N4000-13SI ) as recommended by PCB manufacturer for PCBs with 20Gb lines

#### Posts to the chat:

- Does the move to 10Gb/s require a more specialised PCB material to be used and what PCB material do you currently have in mind for this application?

- the hardware will be prepared to 10Gb/s, the choice will be in HDL

- Hi, could you please point me to the slide repository, if any? Many Thanks

- I see in the feedback slides that somebody suggested to look at N4000-13SI substrate for 10 Gbps links. Maybe it was you? Good subject for discussion later.

- Is this electrical noise, conducted/radiated? or are we talking about vibration?

I.e. is there a risk of vibrations (acoustically) modulating the reference system reference oscillator?

- Mattia's paper:

[https://www.ohwr.org/project/white-rabbit/uploads/253cbfc17d2b43cd445b68348aee0374/Submitted\\_IEEE.pdf](https://www.ohwr.org/project/white-rabbit/uploads/253cbfc17d2b43cd445b68348aee0374/Submitted_IEEE.pdf)

- I think the most of the EMI noise is conducted,

- MDEV is limited at 5E-13/s due to flicker noise. ADEV written in the specs is higher due to white noise floor from 1 to 30 Hz. Better oscillator will reduce this white floor improving ADEV, but MDEV will stay the same MDEV and ADEV values with ENBW=50Hz

- Agreed, UFL is low cost and really quite unsuitable. MCX, or MCX would be much better MMCX rather

- SMAs can work, as long as they are suitably torqued. A naturally retained connection with a detente is better.

- <https://www.fs.com/de-en/products/51419.html>

- Will there be a little more discussion around the topic of "Low Phase Drift Calibration" support in the WRS4 later in the presentations?

- The footprint of cSFP connector I guess is not compatible with regular SFPs?

- you can fit a regular SFP in the same port.

<https://edgeoptic.com/product/cSFP/>

<https://news.thomasnet.com/companystory/compact-sfp-compact-sff-msa-group-forms-813691>

- For the cost/resource issue, one could plan for different stuffing options for the Zync U, i.e a switch variant with more active ports with a larger FPGA?
- Given the comments earlier about bandwidth utilisation, I guess you only need a few 10Gb uplinks, so support many 1Gb ports
- I would think the HW should be planned for 10G all ports, the number of 1G vs 10G ports is a decision for the FW implementation
- just my five cents for the remaining questions on connectors: Moving the management port to the right side is probably fine; clock IO: PPS + 10 MHz in and out is fine; the display is not really important and can be dropped. important thing are the 18 x 1Gb ports
- Regarding ESD protection being ineffective, Littelfuse have some good articles on how parasitic inductance can play a big role in degrading the effectiveness of ESD protection devices. Perhaps there are some improvements that could be made to this next design ([https://www.littelfuse.com/~/media/electronics/application\\_notes/esd/littelfuse\\_tips\\_for\\_enhancing\\_esd\\_protection\\_application\\_note.pdf](https://www.littelfuse.com/~/media/electronics/application_notes/esd/littelfuse_tips_for_enhancing_esd_protection_application_note.pdf))
- (also page 6 of this ONSEMI part: <https://www.onsemi.com/pub/Collateral/NUP4201MR6-D.PDF>)
- USB-C is mechanically weak. I broke some (sorry, no microphone). Problem with soldering. I may be alone here
- I would be more afraid that mini B will disappear over the lifetime of the device.
- we may need a baffle that can be fitted to re-direct some airflow if required - this would be a cheap option
- Innodisk offer some SSD on a chip.
- I don't trust eMMC. With NAND + UBI we know how we use it, with eMMC is black magic. Still, cost and size is important
- [https://www.innodisk.com/en/products/flash-storage/nanosd/nanosd\\_3me3](https://www.innodisk.com/en/products/flash-storage/nanosd/nanosd_3me3)
- Having USB ports for development may be useful regardless or mSATA SSD
- mSATA looks good to me (still, I don't trust it, but it's removable)
- £££...for good reason
- Also USB 3.0? in front
- The issue here I wonder is not so much insertion loss, but i was curious about the effects of changes in delay across the PCB vs Temperature
- a NVMe SSD is another 5W in heat.
- yes this is something to take into account
- Innodisk SLC SSD on a Cip is circa 2.3W max
- ([https://www.innodisk.com/en/products/flash-storage/nanosd/nanosd\\_3ie3#tab2](https://www.innodisk.com/en/products/flash-storage/nanosd/nanosd_3ie3#tab2))
- tempco of the components will likely be dominant