Research Group on Internet Measurement Systems
@ Institute of Electronic Systems
Warsaw University of Technology
Team

• Prof. Ryszard Romaniuk - Optoelectronics
• Prof. Krzysztof Poźniak - FPGA
• Dr. Maciej Linczuk - DSP
• Dr. Grzegorz Kasprowicz - PCB
• Dr. Ryszard Kossowski - Cryptology
• M.Sc. Michał Ramotowski - Analogue electronics
• 10 Ph.D, 20 M.Sc, 15 B.Sc students
Main activities:

• Optoelectronic terabit technologies
  - very fast & synchronous data & clock transmission

• FPGA technologies
  - full hardware & firmware design, multi-FPGA systems

• DSP technologies
  - DSP proc. & DSP in FPGA designs, R-T algorithms

• PCB design (multi GHz)
  - multilayer (up to 24) PCB, EMC/SI verified and tested

• Analogue electronics
  - low noise high speed, multichannel front-ends

• Hardware assembling
  - own assembly workshop, professional HW production

• Hardware testing
  - EMC/SI simulation and measurements
Technical equipment:

• 2008-2012 hardware investment: 3 mln plz + new lab. space
• Computer cluster - 32 multi-core PCs
• FPGA developing hardware
  - Evaluation Boards with FPGAs & DSP processors
  - NanoBoard module system for FPGA test designs
• Precision Time distribution systems - PTP (NI), WR (CERN)
• Scopes - several 60, 20, 5, 1GHz, Analogue and Mixed Signal
• SI laboratory - CS8200 analyser (70GHz Main-Frame) + modules
• Generators - arbitrary Analogue and Mixed Signal, RF up to 3GHz
• Solder & assemble - Pick and Place, 4-zone reflow owen
• Software
  - CAD software (Code Composer, Matlab, ISE, Quartus II)
  - PCB design software (Altium Designer, PADS, Hyper Lynx)
International HEP cooperations:

• DESY (from 1990)
  - Experiment ZEUS at HERA accelerator – BAC detector
  - VUV-FEL, X-FEL – LLRF for TESLA cavities & RF-GUN

• CERN (from 1995)
  - Experiment CMS at LHC accelerator – RPC Muon Trigger
  - PS beam intensity and position monitoring
  - WR development

• ITER, JET, Euroatom (from 2010)
  - R-T plasma diagnostics
White Rabbit development at WUT

- WR gateware, standardization, tests
  - M. Lipiński - PhD student at CERN

- WR hardware
  - SPEC (Simple PCI Express FMC Carrier)
  - SVEC (Simple VME FMC Carrier)
  - POWEC (Power PC FMC Carrier)
  - WR-enabled MCH for uTCA
  - FMC DEL 1ns 4cha
  - FMC ADC 125M 14b 1ch DAC 600M 14b 1ch
  - Stand-alone 18-slot FMC carrier
  - AMC-FMC carrier
SPEC

- Simple PCI Express FMC carrier
  - basic WR node used around the world.
    - commercially available
    - used with FMC DIO and WRS for simple time and event distribution network
SVEC

• Simple VME FMC carrier
  - used with FMC DIO and WRS for simple time and event distribution network
  - second FMC slot enables ADC, DAC or TDC installation
POWEC

• Power PC based FMC carrier
  - used with FMC DIO and WRS for simple time and event distribution network
  - Embedded powerful CPU enables data processing and storage
WR-enabled MCH for uTCA

- MCH for uTCA systems
  - powerful HQ clock distribution
  - versatile FPGA+MGT switch design - great flexibility
  - available in many options: clock, DDS, MGT switch for FP2
FMC DEL 1ns 4cha

• Versatile TDC/DTC/delay
  - provides sub-ns event capture and generation
  - programmable pulse delay: 50 ns - 1 s (10 ps resolution)
FMC ADC 125M 14b DAC 600M 14b

- Versatile ADC/DAC
  - RF analysys and generation (DDS)
  - RF transfer over WR
  - General purpose data acquisition and generation
Stand-alone 18-slot FMC carrier

• 18 FMC slots, 5 large FPGAs + Intel CPU
  – WR enabled
  – high speed, PCIe + MGT links, low latency FMC-to-FMC communication backplane
AMC FMC

- Simple AMC FMC carrier (ATCA and uTCA)
  - used with FMC DIO and WRS forms simple time and event distribution network
  - second FMC slot enables ADC, DAC or TDC installation
Summary

- WUT has competences to build any custom WR-based measurement system.
- We are interested in WR standardization and development.
- WR can solve some problems of future Ethernet networks by adding controlled latency and synchronous operation.