DAC additive phase noise in the WR DDMTD-based clocking scheme

Author: Mattia Rizzi (mattia.rizzi@cern.ch) **30/08/2016**

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1 Abstract

This document explains the additive phase noise due to quantization noise in a theoretical way. Moreover, it provides phase noise values using the default mounted DAC (AD5662, 16 bits), taking into account also the voltage noise due to the DAC output stage. The result of the calculation is that AD5662 is still fine for cheap, AT-cut, voltage controlled crystal oscillators (VCXOs). In order to optimally control an OCXO with SC-cut crystal, a DAC resolution of 20+ bits is recommended.

2 Additive phase noise due to quantization noise

This section is dedicated to the calculation of the quantization's effect on the tuning word feed to the DAC. The quantization noise has a direct effect on the phase noise performance of the VCXO. The quantization noise effect is treated as an uncorrelated noise (respect to VCXO internal noise). Thanks to the statistical properties of uncorrelated noise sources, the combined phase noise is the sum of the VCXO internal noise and the phase noise due to quantization (hence the "additive" term).

In order to calculate the additive phase noise some hypothesis are necessary:

- Electronic frequency control (EFC) linearity: the control word in period of 1 second (the phase noise plot starts at 1Hz) typically doesn't change above a couple of percentage points respect to the EFC full-scale. It is safe to linearize around the working point.
- Quantization noise: the quantization noise is uncorrelated respect to the tuning words and it has a white flat spectrum. This is a common assumption in order to deal with quantization noise.

2.1 DAC quantization noise

To calculate the quantization noise of the DAC we model it as an ideal DAC with a zero-order reconstruction filter (ZOH). The modelled DAC has a step size of Δ volt, a sample frequency (dictated by the control loop) of f_s hertz (sampling period T_s).

The quantization noise can be modelled as a random variable with a zero-mean uniform distribution, hence the standard deviation (or RMS value) of the quantization noise power is:

$$\sigma_\Delta = \sqrt{\Delta^2/12} \quad (1)$$

The (two-sided) power noise spectrum density (PSD) of the quantization noise at the output of the DAC with the optimal reconstruction filter is expressed as follows:

$$S_{\Delta,DAC}(f) = \sigma_{\Delta}^2 \cdot T_s \cdot rect\left(\frac{f}{f_s}\right) \quad (2)$$

S_{DAC} is expressed in V^2/Hz and has a flat spectrum from $-f_s/2$ to $+f_s/2$.

Since the DAC is modelled with a ZOH reconstruction filter, the actual noise power is:

$$S_{\Delta,DAC}(f) = \sigma_{\Delta}^2 \cdot T_s \cdot sinc^2\left(\frac{f}{f_s}\right) \quad (3)$$

The phase noise instruments typically uses single-sided spectrums. In order to get the correct value the formula (3) must be expressed as a single-sided PSD as follows:

$$S'_{\Delta,DAC}(f) = 2 \cdot S_{DAC}(f) \ \forall f \geq 0 \quad (4)$$

2.2 From DAC quantization noise to phase noise

The output voltage noise from the DAC is modulating the VCXO through the EFC control line. The VCXO is modelled as an ideal VCO with a tuning sensitivity of K, expressed as ppm/V.

The instantaneous frequency variation of the VCXO due to $S'_{\Delta,DAC}(f)$ can be expressed as the PSD of the normalized frequency as follows:

$$S'_y(f) = S'_{\Delta,DAC}(f) \cdot (K \cdot 10^{-6})^2 \quad (5)$$

In order to get $S'_{\varphi}(f)$, defined as the one-sided PSD of the random phase noise, only a normalized integration is required, as follows:

$$S'_{\varphi}(f) = \frac{v_0^2}{f^2} \cdot S'_y(f) \quad (6)$$

where v_0 can be the VCO frequency, or an equivalent frequency which the phase noise is calculated.

The IEEE standard 1139 recommends to report the phase noise spectrum as $\mathcal{L}(f)$, defined as

$$\mathcal{L}(f) = \frac{1}{2} S'_{\varphi}(f)$$

$$\mathcal{L}_{dB}(f) = 10\, log_{10}\left(\frac{1}{2} S'_{\varphi}(f)\right)$$

The final formula of additive phase noise due to DAC quantization noise can be expressed as follows

$$\mathcal{L}_{DAC}(f) = \frac{v_0^2}{f^2} (K \cdot 10^{-6})^2 \cdot \sigma_{\Delta}^2 \cdot T_s \cdot sinc^2\left(\frac{f}{f_s}\right) \quad (7)$$

2.3 Additive DAC phase noise in WR (quantization noise)

WR devices typically use a 16 bit DAC converter (AD5662) with a VCTCXO (typically VM53S3) which has a tuning sensitivity of 10 ppm/V and a DAC reference voltage of 2.5V. The control loop sampling rate is determined by the beat frequency of the DDMTD (3814 Hz).

$$\Delta = \frac{2.5\ V}{2^{16}}$$

Since the RC low-pass filter between the DAC output and the EFC line has a bandwidth of 10kHz, it can be omitted if the phase noise plot is limited to 10kHz. This makes sense since above 10kHz the additive phase noise is filtered out and it doesn't make any contribution to the total phase noise of the oscillator.

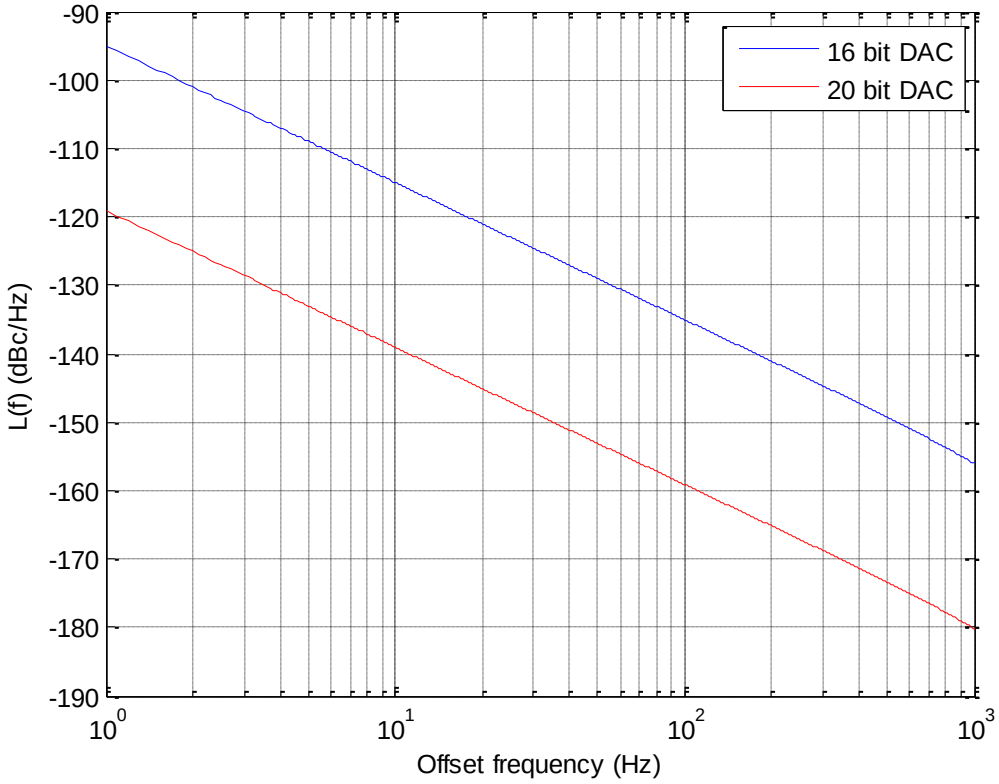

Figure 1 Phase noise due to quantization noise with 10MHz carrier

Figure 1 shows the additive phase noise due to quantization effects. A 16 bit DAC is enough for an AT-cut crystal oscillator as VM53S3 or for a less noisy cheap oscillator (e.g. Connor Winfield T604). If an high quality OCXO is used (SC-cut), the quantization noise with 16 bit can be relevant (e.g. Morion MV272M performs 20dB better at 10Hz).

2.4 Additive DAC phase noise in WR (quantization noise + output noise)

The calculation done until now does not take into account the noise voltage due to the noisy output stage of the DAC. The noise output of the AD5662 is divided in two frequency regions.

The first region is the low frequency. The datasheet specifies a voltage noise of 10uV p-p from 0.1 Hz to 10 Hz. Actually, the total noise power depends also on the noise of the reference voltage. The 0.1Hz to 10Hz is less critical if a cheap VCTCXO is used, since the noise of the VCTCXO itself is greater (typically -70 dBc at 1Hz and -100 dBc at 10Hz). The control loop bandwidth is typically above 10Hz; hence the 0.1Hz to 10Hz noise is not critical.

The second region is from 10Hz to the cut-off of the DAC filter, 10kHz. Here, the combined PSD of the DAC and of the voltage reference used (default is LM385) could be greater than the quantization PSD.

The PSD graph in a datasheet is expressed in $V/\sqrt{Hz}$, in order to have an idea of the noise due to quantization, it can be expressed as $\sqrt{S'_{\Delta,DAC}(f)}$.

The output noise due to quantization is flat (from 0 to about 1kHz) with a density of 250 $nV/\sqrt{Hz}$. As it can be seen from Figure 2 and 3, the most powerful noise source is the voltage reference. The combined noise (quantization, reference voltage and DAC noise) can be over-estimated as high as 1000 $nV/\sqrt{Hz}$ from 10Hz to 1kHz.

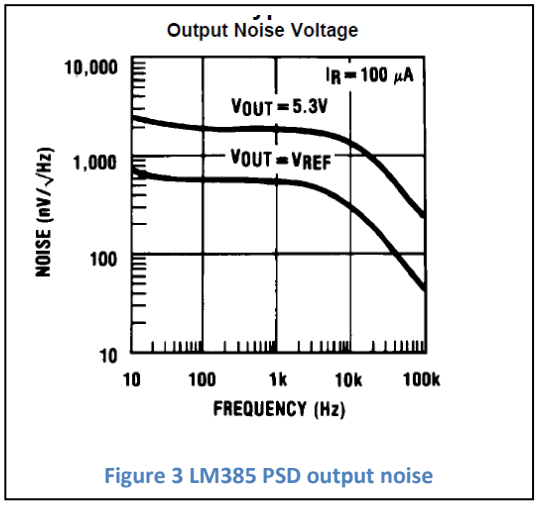

Figure 3 LM385 PSD output noise

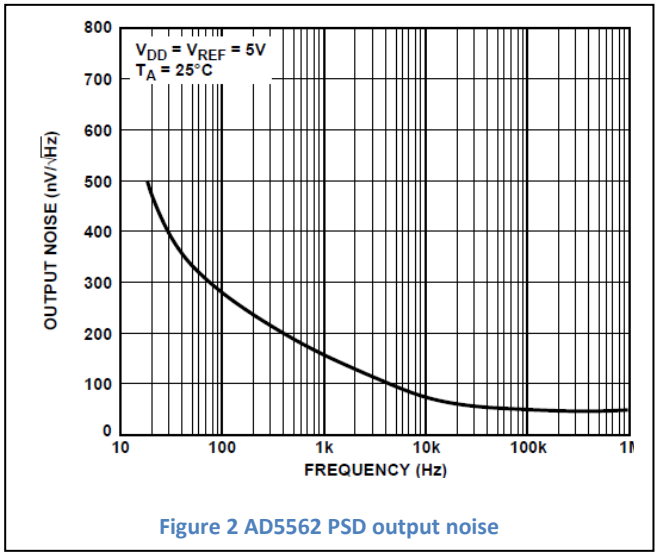

Figure 2 AD5562 PSD output noise

Figure 4 shows the additive phase noise spectrum with the combined noise sources. The result is still good for controlling a cheap VCTCXO.

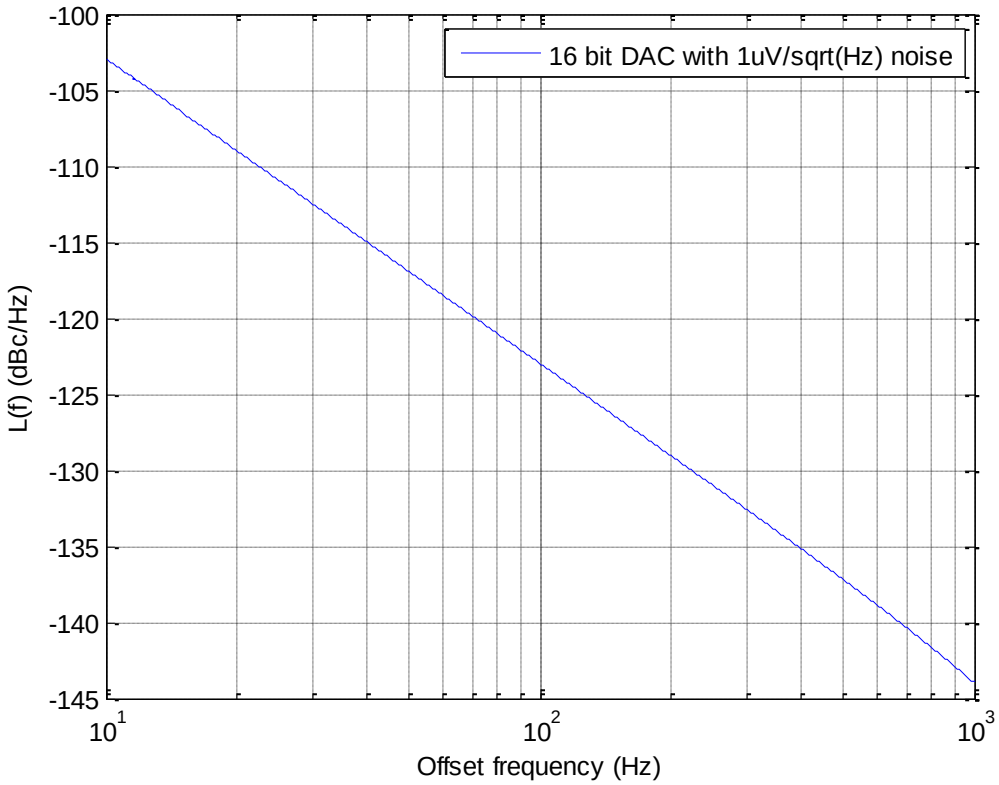

Figure 4 Additive phase noise with 10MHz carrier, 1uV/rtHz noise

3 Conclusions

The default mounted DAC on WR devices, AD5662, is still fine for cheap, AT-cut, voltage controlled crystal oscillators (VCXOs). In order to optimally control an OCXO with SC-cut crystal, additional bits are required if the tuning sensitivity is in the order of ppm/V. The provided formula can be used to calculate the additive phase noise using any VCO or DAC devices.