Clock input for external 10MHz input
Signal type: AC or DC coupled
Allowed power: from -10dBm to 10dBm
Waveform: sine wave or square

Clock output to be connected to the WRS PCB board
Signal type: Buffered LVCMOS DC coupled

Minimum voltage: 9V
Maximum voltage: 14V
Power consumption: 0.3A @ 12V
Connect directly to the WRS power supply

Differential probe points for debug
Signal type: LVPECL AC

Minimum voltage: 8V
Maximum voltage: 14V
Power consumption: 0.3A @ 12V
Connect directly to the WRS power supply

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Top block diagram

Project/Equipment: WR-LOW-JITTER
Document: 30008207.0001.D
Designer: M.R.
Drawn by: M.R.
Last Mod: 25/10/2016
File: Daughterboard.SchDoc
Print Date: 25/10/2016 - 17:52:25
Sheet: 1 of 6

EDA-XXXXX-VX-X
Formula to calculate the output voltage:
\[ V_O = 0.8 \times \frac{R_2}{R_3} \]
PLI Settings:
- Bandwidth: 75MHz
- Margin: 50 degrees
- VCO: 1.5GHz
- VCO DIV: 3
- Reference DIV: 1
- Icp=3.7mA

IC4A
- LPF
- C12
- R4
- GND

PLL_REFSEL
- PLL_RESET
- PLL_LOCK
- PLL_SCLK
- PLL_SDO
- PLL_CS

PLL.SchDoc
- M.R.

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Differential probe points for debug
Place near the J3 connector

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Board detection based on digital I/O loopback

Settings for OSC frequency:

- ID0: ID1, ID2
  - 0 0 0 - 10M
  - 0 0 1 - 20M
  - 1 0 0 - 25M
  - 0 1 1 - 50M
  - 1 0 0 - 100M

Default setting: 20M
Final settings:
FILTA = LOW
FILTB = HIGH

Dont place jumpers for final settings.
Board S