RF distribution over a White Rabbit link

(a proof of concept)

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The idea

- Input any reasonably stable (FM bandwidth: ~ 20 kHz) clock signal,
- Digitize it and broadcast over a synchronous network,
- Reproduce the original signal at any number of receivers,
- Share the network with other applications.
Distributed DDS

Encoder

Monitor out

Input

600 MSPS 14-bit DAC

DD Synthesizer

Timestamp packet encoder

White Rabbit PTP Core

WR reference clock (125 / 500 MHz)

Monitor out

Input

ADF4002 Phase detector

Antialias

1 MSPS 16-bit ADC

Loop filter

WR Network

Receiver

White Rabbit PTP Core

Packet decoder

DD Synthesizer

600 MSPS 14-bit DAC

PLL jitter cleaner

Reproduced clock

WR components

Distributed DDS

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Distributed DDS

- Use a fast DAC driven by a DDS as a tunable oscillator,
- Put it inside a PLL, referenced with the clock that we want to transmit,
- Postprocess, encode and broadcast the oscillator tuning values over the WR network,
- Drive any number of identical DDS cores with the received data stream,
- Since WR ensures phase-compensated 125 MHz reference clock at every node in the network, slave DACs will produce a copy of the master's clock.
Test system

• 2 SPEC cards with 2 DDS FMC mezzanines.
  
  http://www.ohwr.org/projects/fmc-dac-600m-12b-1cha-dds/wiki
  http://www.ohwr.org/projects/spec

• Point-to-point link.

• Test frequency: 10 MHz cesium standard, loop bandwidth: 10 kHz, broadcast rate: 110 kHz.

• Encoder PLL performance: 6 ps rms jitter (10 Hz – 5 MHz), -110 dBc/Hz noise floor (@ 100 Hz)

• Recovered clock: 8.5 ps rms jitter.

• Significant part of the jitter likely comes from buggy PCB design (1st prototype)
Test system

RF Source
40.079 MHz AWG
or 10 MHz cesium

Oscilloscope

Signal source analyzer

SPEC 1
Master

WR Switch

SPEC 2
Slave

Recovered clock

Master PLL
out

IN

DDS
FMC

DDS
FMC
Performance

Master PLL
6.8 ps rms
Performance

Recovered clock 8.5 ps rms
To do…

- Implement point-to-multipoint transmission and simultaneous encoding of multiple clocks,
- Reduce data bandwidth requirements – better encoding (prediction-correction or jitter-bound lossy compression),
- Optimize jitter: fine-tune PLL filters, deal with PCB issues, check performance with an additional cleaner PLL.
Summary

• **Proof-of-concept** system with very promising results,

• Possibility of unifying general and beam-synchronous timing (like TTC) with bidirectional data distribution in a **single network**, 

• **Extensible** to arbitrary analog signals.