Status of the core WR components

WR Switch & WR PTP Core

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Outline

• WR Switch
  • Introduction
  • Features of v6.0
  • Current developments

• WR PTP Core
  • Introduction
  • Upcoming v5.0
White Rabbit network

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Status of the core WR components
Central element of WR network
18-port GbE switch with WR features
WR Switch – hardware overview

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Status of the core WR components
WR Switch – gateware overview

Virtex-6 FPGA

- Optical transceiver 1..18
- Xilinx SerDes 1..18
- GbE Endpoint 1..18
- Switching Core
- Timestamps FIFO
- Watchdog
- Routing Table
- CPU/Wishbone bridge
- Stats Counters
- Timing Subsystem
- Network Interface

1-PPS 10MHz
WR Switch – main features of v6.0

1. Low Phase Drift Calibration (LPDC)
   - Xilinx MGT latency uncertainty +/- 100 ps
   - Caused by Tx/Rx phase aligners and clock dividers
   - Disable both in MGT configuration
   - Additional Phy Tx/Rx calibration at boot time
   - **Phase stability < 5ps**
   - Only WR ports 1-12

![Histogram of phase error](image)
WR Switch – main features of v6.0

2. Low-Jitter Daughterboard support (LJD)
   • Add-on board for WR Switch (7S, Creotech)
   • ...or Integrated in WR Switch (OPNT, SyncTechnology)
   • Replaces internal FPGA PLL and VCXO
   • Reduces jitter (1Hz-100kHz) from 9ps RMS to <2ps RMS
WR Switch – main features of v6.0

3. Networking improvements
   • Port mirroring including CPU traffic (*rtu_stat mirror <...> shell command*)
   • Preamble shrinkage support

4. IEEE1588 compatibility
   • Fields in Announce msg
   • BMCA fixed
   • Leap-second handling
   • Prepared for IEEE1588-2019 HA Profile
5. Automated IEEE1588 compliance testbed
   • Xena network tester + Veryx ATTEST Framework
   • CLI interface with WR Switch
   • IEEE1588 + VLANs tests purchased
   • WR + HA Profile tests developed for CERN
   https://ohwr.org/project/wr-compliance-tests
6. Monitoring & management improvements
   • LDAP+Kerberos authentication
   • LLDP support
   • Syslog local logrotate (/tmp/syslog-*)
Do NOT use v6.0
Issue #239: sync lost every ~50 days

Use v6.0.1 instead
WR Switch – beyond v6.0.1

Done:
1. State reporter to gather all info about a WRS (*wrs_dump.sh*)
2. LLDP working with VLANs
3. More standard MIBs filled in SNMP (BRIDGE-MIB, QBRIDGE-MIB, IP-MIB)
4. Radius-vlan/802.1X MAC authentication
5. Bugfixes
   • SFP DOM access affecting synchronization and SFP EEPROM content

Planned:
6. IEEE1588-2019 HA profile implementation
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Status of the core WR components

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WR Node

Status of the core WR components
WR Node

WR PTP Core is essential part of every WR Node

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Status of the core WR components
WR PTP Core overview

• Gigabit Ethernet MAC HDL module
• ... with WR features
• Provides time to user cores
• Can send and receive user-defined Ethernet frames
WR PTP Core overview

- Implemented in the FPGA
- Using VHDL language
- You don’t need to know WR internals
- You need to know FPGAs to use it
WR PTP Core interfaces

Hardware interfaces:
- Clocks / reset
- DACs output
- PHY I/F
- Flash/EEPROM
- UART / LEDs

User interfaces:
- Fabric I/F
- Control WB
- Timecode I/F
- Aux Clk I/F
LatticeMico32 runs \texttt{wrpc-sw} (PTP, shell, diagnostics...)
Board and Platform Support Package in HDL

- **Board Support Package (BSP)**
  - WR PTP Core
  - VCO DAC controller
  - Reset logic
  - Differential clock buffers
  - Platform Support Package

- **Platform Support Package (PSP)**
  - Deterministic GbE Serdes module
  - PLLs for main and DMTD offset clock

BSP glues WRPC with all required FPGA modules for a given hardware
WR PTP Core – towards v5.0
Reasons for v5.0

• v4.2 was released at the end of 2017
• New hardware platforms
• More complex hardware platforms
• More modern FPGA families
• A lot of work done by the community in various git branches
More supported platforms

- Altera Arria II, Arria V
- Xilinx Spartan-6 GTP
- Xilinx Series-7 GTP / GTX / GTH
- Xilinx Virtex-5 GTP
- Xilinx Kintex UltraScale GTHE3
- Xilinx Zynq UltraScale+ GTHE4
More reference designs

• Kept reference designs for SPEC/SVEC/VFC-HD/FASEC
More reference designs

- Added support for new platforms

SPEC7 (Zynq-7)  SPEXI7U (Zynq US+)  DI/OT System Board (Zynq US+)
HDL modifications

- Replace LM32 with Risc-V
  - Unclear licensing of LM32
  - Modern gcc support
  - Smaller binary size

- Diags RAM area
  - Basic diagnostics to the host
  - Possible to expose board-specific diagnostics

- LPDC for Kintex 7 GTX
wrpc-sw reorganisation

- Introduction of Board Support Packages
  - board.c / board.h
  - Board-specific initialization / peripherals access
  - Custom base addresses
  - I2C EEPROM addresses
  - Custom storage / unique MAC initialization
- Kconfig board selection
- Generic BSP to keep things how they used to be
wrpc-sw reorganisation

• Most drivers rewritten to use context objects
• New tasks subsystem
  • with simple event system
  • allows dynamic task creation
  • ... and BSP-specific tasks
  • `wrc_task_create(name, *init(), *job());`
• More flexible storage support
  • BSP defines and mounts Flash/EEPROM
• Kconfig-configurable debugging levels
• Updated PPSi with IEEE1588 compliance fixes
New Features

• Netconsole
• UART bootloader – for host-less platforms
• New drivers
  • Unique MAC EEPROM
  • GPIO expander
  • SPI ADC
  • PLLs/clk fanouts
  • ...
• SoftPLL can discipline programmable VCXOs
  • Si570 / Si571
• Support for “lock-sweep”
  • To discipline clocks that are not multiples of 62.5MHz
• SNMP SET configuration of SFPs and *init* script
Conclusions

WR Switch firmware:

Please use v6.0.1

WR PTP Core:

Please be patient, v5.0 is coming

Cleanup your branches and let us know your merge requests