IEEE standardisation of WR and future directions

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11th White Rabbit Workshop
6 October 2021
Agenda

• A bit of history
• WR in IEEE1588-2019
• Migration to IEEE1588-2019
• Costs, benefits and lessons learned
• Beyond IEEE1588-2019
• Conclusions
White Rabbit synchronisation

2008: WR Project Start

2011: Publish WR Spec (WR-PTP)

Based on IEEE1588-2008

How to make it a standard?

WR-PTP (WR extension of IEEE1588-2008)

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2013: Start IEEE1588 revision

2016: Finish draft

2017: Start 1st Int. Ballot

2017: Start 2nd Int. Ballot

2018: Start 3rd Int. Ballot

2018: Start Sponsor Ballot

2019: Submit draft to IEEE

2019: Approve text

2020: Publish IEEE1588-2019 (HA Profile)

2020: Open new PAR

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IEEE1588 revision

IEEE standard lifecycle
(enforced to ensure new edition every 10 years)

2008: WR Project Start
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2013: Start IEEE1588 revision

- Initiating the project
- Mobilizing the working group
- Drafting the standard
- Balloting the standard
- Gaining final approval
- Maintaining the standard

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Project Authorisation Request (PAR)

The protocol enhances support for synchronization to better than 1 nanosecond.
IEEE1588 revision

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IEEE1588-2008
IEEE1588 revision

- Performed by **P1588 Working Group** with over 200 members
- Divided into 5 sub-committees
IEEE1588 revision

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• Performed by P1588 Working Group with over 200 members
• Divided into 5 sub-committees
• High Accuracy (HA) sub-committee
  – Focused on White Rabbit
  – Experts from industry and academia
  – Division of WR into self-contained parts, useful separately
  – Definition of Optional Features and High Accuracy Profile that allows WR implementation and performance
• 3 years to have the first draft.
Draft and its ballots

- WR-to-HA translation in the draft:
  3 new annexes, 4 new optional features and a new PTP Profile
- Internal Ballots – within the Working Group:
  - 1\textsuperscript{st}: 3352 comments (666 technical) – 9 months
  - 2\textsuperscript{nd}: 1504 comments (541 technical) – 5 months
  - 3\textsuperscript{rd}: 749 comments (292 technical) – 4 months
- Sponsor Ballot – any IEEE member can join
  - 127 voters, 84% affirmative votes, 358 comments – 12 months
  - 2 re-circulations (mini-ballots) – 4 months
- Final text:
  - 499 pages (instead of 289 pages in IEEE1588-2008)
  - WR/HA-specific sections/annexes: ~55 pages
IEEE SA Standards Board approval

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2018: Start 3rd Int. Ballot
2018: Start Sponsor Ballot

2019: Submit draft to IEEE
2019: Approve technical content

2020: Publish IEEE1588-2019 (with High Accuracy Profile)

• Nov 2019
  – Draft submitted to IEEE RevCom for approval
  – IEEE SA Standards Board (SASB) approved the revised P1588 draft

• Review of IEEE Editor
  – Correct editorial errors and respect technical content
  – Few iterations and 7 months

• June 2020 – IEEE1588-2019 published

IEEE SA Standards Board (SASB) approved the revised P1588 draft.

Review of IEEE Editor:
- Correct editorial errors and respect technical content
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IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems

IEEE Instrumentation and Measurement Society

Developed by the Technical Committee on Sensor Technology (TC-5)

IEEE Std 1588-2019
[Revision of IEEE Std 1588-2008]
IEEE1588-2019

“Synchronisation framework”

“Extensible & parameterised core”
(attributes, delay mechanism)

Optional parts
(optional features)
IEEE1588-2019

"Synchronisation framework"

"Extensible & parameterised core" (attributes, delay mechanism)

Optional parts (optional features)

Transport mappings

Informative Annexes
IEEE1588-2019

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Informative Annexes

Telecom

PTP Applications

Power
IEEE1588-2019

“Synchronisation framework”

“Extensible & parameterised core”
(attributes, delay mechanism)

Profile: delay mechanism, attribute values & options

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Informative Annexes

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PTP Applications

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IEEE1588-2019

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ITU-T Profiles

Telecom

Applications

IEEE/IEC Profiles

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Optional parts
(optional features)

Default Profiles
- Delay Request-Response
- Peer-to-peer

Transport mappings

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WR-PTP

PTP Applications
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Default Profiles
- Delay Request-Response
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- High Accuracy Delay Request-Response

Transport mappings

Informative Annexes

Applications

WR-PTP
White Rabbit split into parts

1. L1 syntonisation and WR Link Setup
2. Delay asymmetry estimation and correction of PTP calculations
3. Calibration procedure
4. Assignment of fixed roles (master/slave) to WR ports
5. WR PTP Profile compatible with Default PTP Profile
1. L1 syntonization in WR

- Syntonisation of Local PTP clock by L1 clock signal and L1 and PTP are congruent
- Frequency loopback between Master & Slave
- Enhancements of timestamps via phase detection
1. L1 syntonization in HA

- In Annex L: Layer-1 based synchronisation performance enhancements
- Flexible and configurable relation between PTP and L1 clocks while all phase offsets known and pseudo-constant
- Enhancements of timestamps via phase detection
- HA PTP Profile forces congruency between L1 and PTP and frequency loopback
1. **WR Link Setup**

- WR State machine in PTP Uncalibrated State
- WR TLV attached to Announce and Signaling messages
- Detection of WR support by a peer
- Handling of WR configuration matching
- Unidirectional status exchange
- Includes obsolete calibration of external PHY
1. **HA L1Sync Link Setup**

- In Annex L: Layer-1 based synchronisation performance enhancements
- L1 state machine semi-independent from PTP’s
- L1Sync TLV attached Signaling messages
- Detection of L1Sync support by a peer port
- Handling of L1 configuration matching
- Continues bidirectional status exchange
2. Correction of PTP calculations

• Hardware delays:
  • In WR: only Slave corrects $\text{offset}_{ms}$ for $\Delta_{TXM}$, $\Delta_{RXM}$, $\Delta_{TXS}$, $\Delta_{RXS}$
  • In HA: Configurable correction of timestamps (16.7)
    Master and Slave correct timestamps for ingress/egress latencies,
    their values can change over time, e.g. accounting for temp. effects
2. Correction of PTP calculations

• Hardware delays:
  • In WR: only Slave corrects $offset_{ms}$ for $\Delta_{TXM}$, $\Delta_{RXM}$, $\Delta_{TXS}$, $\Delta_{RXS}$
  • In HA: Configurable correction of timestamps (16.7) Master and Slave correct timestamps for ingress/egress latencies, their values can change over time, e.g. accounting for temp. effects

• Delay asymmetry estimation:
  • In WR: $delay_{ms} = \frac{1+\alpha}{2+\alpha} \delta_{m_m}$, $\alpha$ in float
  • In HA: Calculation of the delayAsymmetry (16.8)
    $delay_{ms} = < meanDelay > + < delayAsymmetry >$
    $< delayAsymmetry > = constantAsymmetry + \frac{\alpha}{2+\alpha} < meanDelay >$

$constantAsymmetry$ – allows fine tuning asymmetry (e.g. account for active elements)
3. Calibration procedure

- **In WR:** a separate document: “WR Calibration procedure v1.1”
- **In HA:** Annex N in IEEE1588-2019
  - Rewritten into a generic informative annex
  - Rewritten to use IEEE-1588 terminology and data sets
  - Exactly the same step-by-step procedure

- **Does not include**
  - Mathematical proofs
  - Measurement errors estimation
4. Assignment of fixed roles

• **In WR**: BMCA overridden to force Master or Slave

• **In HA**: two options
  • **MasterOnly Mode** (9.2.2.2)
    • Best Master Clock Algorithm running
    • Some PTP Ports can be set to MasterOnly
    • MasterOnly PTP Ports are disallowed from becoming PTP Slaves

• **Mechanism for external role configuration** (17.6)
  • Best Master Clock Algorithm disabled
  • All PTP Ports in a Boundary Clock affected
  • External mechanism to configure PTP Port state
5. **WR PTP Profile**

- “White Rabbit PTP Profile”
- Extends and interoperates with Delay Req-Resp Default PTP Profile
- Mandates support of WR extensions, including BMCA modification
- Defines default and allowed values of attributes, including priority1=64
5. HA PTP Profile

• “High Accuracy Delay Request-Response Default PTP Profile” (I.5)
• Extends and interoperates with Delay Req-Resp Default PTP Profile, allows interoperation with Peer-to-Peer Default PTP Profile
• Mandates support of HA optional features
• Defines default and allowed values of attributes
• Defines High Accuracy Clock Model
  • Local PTP clock is syntonised by L1 and synchronised by PTP
• Does not include
  • BMCA modifications & Priority1=64
High Accuracy Default PTP Profile

IEEE1588 “Core”

Defines attributes and mechanisms

High Accuracy Request-Response Default PTP Profile (Annex I.5)

https://ohwr.org/projects/wr-std/wiki/wrin1588
High Accuracy Default PTP Profile

HA-specific optional features (active by default)
- Calculation of the delayAsymmetry (16.8)
- Configurable correction of timestamps (16.7)

L1 Sync (Annex L)

IEEE1588 “Core”

Requires and specifies default/allowed values
Defines attributes and mechanisms

High Accuracy Request-Response Default PTP Profile (Annex I.5)

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High Accuracy Default PTP Profile

**HA-specific optional features (active by default)**
- Calculation of the delayAsymmetry (16.8)
- Configurable correction of timestamps (16.7)

**Generic optional features (inactive by default)**
- Mechanism for external configuration (17.6)
- master Only Mode (9.2.2.2)

**IEEE1588 “Core”**
- L1 Sync (Annex L)

Enhance

Modify BMCA

Requires and specifies default/allowed values

 Defines attributes and mechanisms

Requires and specifies default/allowed values

High Accuracy Request-Response Default PTP Profile (Annex I.5)

High Accuracy Default PTP Profile

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Modify BMCA

Generic optional features (inactive by default)
- Mechanism for external configuration (17.6)
- master Only Mode (9.2.2.2)

High Accuracy Request-Response Default PTP Profile (Annex I.5)

Informative annex describes Calibration Procedures to be used with the HA Default PTP Profile to allow sub-ns accuracy of synchronisation

Calibration Procedures (Annex N)

https://ohwr.org/projects/wr-std/wiki/wrin1588
### High Accuracy Default PTP Profile

#### HA-specific optional features (active by default)
- Calculation of the delayAsymmetry (16.8)
- Configurable correction of timestamps (16.7)

#### Generic optional features (inactive by default)
- Mechanism for external configuration (17.6)
- master Only Mode (9.2.2.2)

#### IEEE1588 “Core”
- Enhance
- Modify BMCA

#### L1 Sync (Annex L)
- Requires and specifies default/allowed values

#### Calibration Procedures (Annex N)
- Calculation of the delayAsymmetry
- Configurable correction of timestamps

#### High Accuracy Request-Response Default PTP Profile (Annex I.5)
- Requires and specifies default/allowed values

#### Calibration Procedures to be used with the HA Default PTP Profile to allow sub-ns accuracy of synchronization

#### Informative annex describes Calibration Procedures

#### Sub-ns synchronisation using High Accuracy Default Profile (Annex M)
- Requires and specifies default/allowed values

#### Informative annex describes HA Profile implementation that provides sub-ns accuracy of synchronisation

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Migration from WR-PTP to HA PTP Profile

- Hardware implementation (DDMTD, L1) is identical for both WR-PTP and HA PTP Profile
- Software implementation (PTP daemon) differs
Migration from WR-PTP to HA PTP Profile

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- Software implementation (PTP daemon) differs
- **Completed**
  - 2018-2019: Compliance tests developed for WR-PTP and HA PTP Profile (see)
  - 2019: Prototype HA PTP Profile implementation on the WR Switch
  - 2020: WRS-3 v6.0 release - prepared to support WR-PTP together with HA PTP Profile
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- **Planned**
  202x: WRS-3 v6.1 release - support for HA PTP Profile and WR-PTP
  202x: WR Node v5.x (x>0) release with support for HA PTP Profile or WR-PTP
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- Software implementation (PTP daemon) differs
- **Completed**
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- **Planned**
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  - **202x**: WR Node v5.x (x>0) release with support for HA PTP Profile or WR-PTP

- **Migration strategy**
  - **WR Nodes**: will support either HA or WR-PTP (support for WR-PTP to be discontinued in future)
  - **WR Switches**: will support both HA PTP Profile and WR-PTP, providing interoperability between the legacy (WR-PTP) and the new (HA PTP Profile) devices

**Absolute calibration** will be introduced with HA PTP Profile
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Costs, benefits and lessons learned

- **Indicative cost:** 2.25 person-year and 26 kCHF over 7 years
  - Participation in online and F2F meetings, organisation of F2F meeting
  - Preparation and review of documents

- **Benefits:**
  - **For WR technology:** known shortcomings fixed, more generic and flexible, scrutinised by industry experts, future-proof
  - **For users/vendors:** ensured mature and stable solution, more applications/vendors, increased competition
  - **For IEEE 1588:** increased popularity and user base of the standard, PTP ready for ever-growing industry requirements
  - **For CERN:** longevity and lower cost of technology, knowledge transfer, key player in IEEE 1588

- **Lessons learned:**
  - A (very) long process
  - Excellent technology required but also patience and an open-minded attitude ready for compromise to reach consensus
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Beyond IEEE1588-2019

- P1588 WG’s CERN-lead New Features subcommittee: Enhancements for Latency and/or asymmetry calibration
  - In-situ calibration
    - Single bidirectional fiber: work by Peter Jansweijer using tunable SFPs
    - Duplex unidirectional fiber: techniques used in telecom by swapping fibers
    - Calibration capability recognition
  - Absolute calibration (based on work by Peter Jansweijer)
    - Definition of electrical reference plane
    - Definition data sets for storing parameters (physical values, traceability parameters)
Beyond IEEE1588-2019

• **P1588 WG’s CERN-lead New Features subcommittee:**

  **Enhancements for Latency and/or asymmetry calibration**

  – **In-situ calibration**
    - Single bidirectional fiber: work by Peter Jansweijer using tunable SFPs
    - Duplex unidirectional fiber: techniques used in telecom by swapping fibers
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• **SNIA Transceivers: standardisation of Absolute Calibration into SFP’s EEPROM format**

  – **SNIA** - Storage Networking Industry Association
  – **Transceivers subgroup** – responsible for SFF-8472 standard that defines SFP’s EEPROM space
  – Ongoing effort to include parameters required by Absolute Calibration in EEPROM space of SFPs as optional values, see [https://ohwr.org/project/sfp-plus-i2c/wikis/sff_std](https://ohwr.org/project/sfp-plus-i2c/wikis/sff_std)
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Conclusions

• White Rabbit is sub-ns implementation of
  • WR PTP Profile of IEEE1588-2008, and
  • HA PTP Profile of IEEE1588-2019

• Compliance tests developed for
  • WR PTP Profile to ensure backward compatibility and long-term support
  • HA PTP Profile to ease implementation for CERN and industry

• HA PTP Profile to be included in the next major release of WR switch

• Ongoing work to include in-situ and absolute calibration into IEEE1588 and SFF-8472
Backup slides
High Accuracy Default PTP Profile

High Accuracy Delay Request-Response Default PTP Profile
High Accuracy Default PTP Profile

High Accuracy Delay Request-Response Default PTP Profile
High Accuracy Default PTP Profile

Delay Request-Response Default PTP Profile

1. Identification: 00-1B-19-01-01-00
2. PTP Attributes: default values & ranges
3. Optional features /mechanism
   • BMCA: default
   • Mechanism: request-response by default, peer-to-peer allowed
   • Required options: none
   • Prohibited options: none
   • Permitted options: all*
4. Clock physical requirements: frequency accuracy below 0.01%

* Optional feature inactive (disabled) by default
High Accuracy Default PTP Profile

1. **Identification**: 00-1B-19-02-01-00
2. **PTP Attributes**: default values & ranges
3. **Optional features / mechanism**
   - BMCA: default
   - Mechanism: request-response by default, peer-to-peer allowed
   - Required options: Annex O, Q.3, 16.7, 16.8, 17.6*, masterOnly*
   - Prohibited options: 16.5
   - Permitted options: all others*
4. **Clock physical requirements**: frequency accuracy below 4.6ppm
5. **Default values & ranges for attributes of required options**
6. **High Accuracy model of Local PTP Clock**
7. **Information on inter-operation with other Default PTP Profiles**

* Optional feature **inactive (disabled)** by default
Options required/prohibited by HA Profile

Required and active by default:
• L1-based sync. performance enhancements [Annex O]
• Configurable correction of timestamps [16.7]
• Calculation of the <delayAsymmetry> for certain media [16.8]
• Requirements of Q.3 [Annex Q]

Required and inactive by default:
• Mechanism for external config. of a PTP Instance’s PTP Port state [17.6]
• masterOnly mode [9.2.2.2 & 8.2.15.5.2]

Prohibited:
• Isolation of PTP Instances [16.5]
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• masterOnly mode [9.2.2.2 & 8.2.15.5.2]

Prohibited:
• Isolation of PTP Instances [16.5]
L1 synchronization enhancements (L1Sync)

• Supports **cooperation** & defines **relationship** between
  – PTP-based **synchronization** and
  – L1-based **syntonization**, e.g. Synchronous Ethernet

• Provides **configuration** and **status** of the PTP-L1 relationship

• IMPORTANT: Requires **hardware support**
PTP synchronization and L1 syntonization

L1 syntonization
clk\_L1x\_A = clk\_L1x\_B

PTP synchronization
clk\_LocalPTP\_A = clk\_LocalPTP\_B

L1 syntonization
clk\_L1x\_A = clk\_L1x\_B

time
PTP synchronization and L1 syntonization

L1 Syntonization
\( \text{clk}_{L1x_{-}A} = \text{clk}_{L1x_{-}B} \)

PTP synchronization
\( \text{clk}_{\text{LocalPTP}_{-}A} = \text{clk}_{\text{LocalPTP}_{-}B} \)

L1 Syntonization
\( \text{clk}_{L1x_{-}A} = \text{clk}_{L1x_{-}B} \)

Transmit coherent port:

Receive coherent port:

Congruent port:

\( \text{clk}_{L1tx_{-}A} = \text{clk}_{L1tx_{-}B} \)

\( \text{clk}_{L1rx_{-}A} = \text{clk}_{L1rx_{-}B} \)

\( \text{clk}_{\text{LocalPTP}_{-}A} = \text{clk}_{\text{LocalPTP}_{-}B} \)
PTP synchronization and L1 syntonization

L1 Syntonization
\(clk_{L1x_A} = clk_{L1x_B}\)

PTP synchronization
\(clk_{LocalPTP_A} = clk_{LocalPTP_B}\)

L1 Syntonization
\(clk_{L1x_A} = clk_{L1x_B}\)

Transmit coherent port: \(x_{tx} = \text{constant}, \text{so} \ clk_{L1tx} = clk_{LocalPTP}\)

Receive coherent port:

Congruent port:
PTP synchronization and L1 synthonization

L1 Synthonization
\( \text{clk}_{L1x_A} = \text{clk}_{L1x_B} \)

PTP synchronization
\( \text{clk}_{\text{LocalPTP}_A} = \text{clk}_{\text{LocalPTP}_B} \)

L1 Synthonization
\( \text{clk}_{L1x_A} = \text{clk}_{L1x_B} \)

Transmit coherent port: \( x_{tx} = \text{constant} \), so \( \text{clk}_{L1tx} = \text{clk}_{\text{LocalPTP}} \)

Receive coherent port: \( x_{rx} = \text{constant} \), so \( \text{clk}_{L1rx} = \text{clk}_{\text{LocalPTP}} \)

Congruent port: 

\( \text{clk}_{L1tx_A} = \text{clk}_{L1rx_B} \)

\( \text{clk}_{L1rx_A} = \text{clk}_{L1tx_B} \)

\( \text{clk}_{\text{LocalPTP}_A} = \text{clk}_{\text{LocalPTP}_B} \)
PTP synchronization and L1 syntonization

L1 Syntonization
clk_{L1x_A} = clk_{L1x_B}

PTP synchronization
clk_{LocalPTP_A} = clk_{LocalPTP_B}

L1 Syntonization
clk_{L1x_A} = clk_{L1x_B}

Transmit coherent port: \( x_{tx} = \text{constant} \), so \( clk_{L1tx} = clk_{LocalPTP} \)

Receive coherent port: \( x_{rx} = \text{constant} \), so \( clk_{L1rx} = clk_{LocalPTP} \)

Congruent port: flow of L1 syntonization and PTP synchronization are the same.
L1 synchronization enhancements (L1Sync)

- **Data sets:** storing config & status of the L1-PTP relationship (congruent, coherent)
- **L1_SYNC TLVs:**
  - Detection of L1Sync-supporting PTP Ports
  - Exchange of config/status/parameters
- **FSM:** control of establishing of the required PTP-L1 relationship
- **Know PTP-L1 relationship:** allows correction of timestamp with phase measurement
L1Sync in High Accuracy Default PTP Profile

- Requirement for L1Sync PTP Port to be: - transmit and receive coherent
  - congruent

\[ x_{tx_A} = x_{rx_B} = x_{tx_B} = \text{known constant} \]

\[ x_{rx_A} = \text{phase measured to enhance timestamp precision} \]
Options required/prohibited by HA Profile

Required and active by default:

• L1-based sync. performance enhancements [Annex O]

• **Configurable correction of timestamps [16.7]**

• Calculation of the <delayAsymmetry> for certain media [16.8]

• Requirements of Q.3 [Annex Q]

Required and inactive by default:

• Mechanism for external config. of a PTP Instance’s PTP Port state [17.6]

• masterOnly mode [9.2.2.2 & 8.2.15.5.2]

Prohibited:

• Isolation of PTP Instances [16.5]
Configurable correction of timestamps

- IEEE1588-2019 (and 2008) defines timestamping ref. plane and allows correction of timestamps for `<ingressLatency>` and `<egressLatency>`:
  - `<ingressTimestamp>` = `<ingressProvidedTimestamp>` – `<ingressLatency>`
  - `<egressTimestamp>` = `<egressProvidedTimestamp>` + `<egressLatency>`
Configurable correction of timestamps

IEEE1588-2019 (and 2008) defines timestamping ref. plane and allows correction of timestamps for $<\text{ingressLatency}>$ and $<\text{egressLatency}>$:

– $<\text{ingressTimestamp}> = <\text{ingressProvidedTimestamp}> - <\text{ingressLatency}>$
– $<\text{egressTimestamp}> = <\text{egressProvidedTimestamp}> + <\text{egressLatency}>$

This optional feature:

– Defines $\text{timestampCorrectionPortDS}$ dataset to store the values of $<\text{egressLatency}>$ & $<\text{egressLatency}>$
– Mandates correction of timestamps with the provided values
Options required/prohibited by HA Profile

Required and active by default:
- L1-based sync. performance enhancements [Annex O]
- Configurable correction of timestamps [16.7]
- Calculation of the $\text{<delayAsymmetry>}$ for certain media [16.8]
- Requirements of Q.3 [Annex Q]

Required and inactive by default:
- Mechanism for external config. of a PTP Instance’s PTP Port state [17.6]
- masterOnly mode [9.2.2.2 & 8.2.15.5.2]

Prohibited:
- Isolation of PTP Instances [16.5]
Calculation of \(<\text{delayAsymmetry}>\)

- IEEE1588-2019 (and 2008) provides calculation of \(<\text{meanDelay}>\) and allows correction of \(<\text{meanDelay}>\) for \(<\text{delayAsymmetry}>\):

  \[
  <\text{meanDelay}> = \frac{[t_2 - t_1] + (t_4 - t_3)}{2} \\
  t_{ms} = <\text{meanDelay}> + <\text{delayAsymmetry}> \\
  t_{sm} = <\text{meanDelay}> - <\text{delayAsymmetry}>
  \]

- **This optional feature:**
  - Defines \(<\text{delayCoefficient}>\) \((\alpha)\) to characterize asymmetry of applicable bidirectional media (e.g. bidirectional fiber)
  - Specifies \(<\text{delayAsymmetry}>\) calculation using \(<\text{delayCoefficient}>\) \((\alpha)\)

  \[
  <\text{delayAsymmetry}> = \text{constantAsymmetry} + \frac{\alpha}{\alpha+2} \cdot <\text{meanDelay}>
  \]

  - Defines asymmetryCorrectionPortDS dataset for \(<\text{delayCoefficient}>\) & \text{constantAsymmetry}
  - Mandates correction of \(<\text{meanDelay}>\) with the calculated \(<\text{delayAsymmetry}>\)
Options required/prohibited by HA Profile

Required and active by default:

• L1-based sync. performance enhancements [Annex O]
• Configurable correction of timestamps [16.7]
• Calculation of the <delayAsymmetry> for certain media [16.8]
• Requirements of Q.3 [Annex Q]

Required and inactive by default:

• Mechanism for external config. of a PTP Instance’s PTP Port state [17.6]
• masterOnly mode [9.2.2.2 & 8.2.15.5.2]

Prohibited:

• Isolation of PTP Instances [16.5]
Calibration

- Values of `<ingressLatency>`, `<egressLatency>`, `<delayCoefficient>` obtained using Calibration Procedures [Annex Q]
- [Q.3] defines requirements for PTP Instance in calibration procedures:
  1. Output signal, e.g. pulse-per-second (PPS)
  2. Optional features in 16.7 & 16.8 supported and enabled
  3. The value `<meanDelay>` exposed to the user
  4. Timestamps with precision sufficient for the intended accuracy of synchronization
  5. `<egressProvidedTimestamp>` and `<ingressProvidedTimestamp>` corrected for semi-static latency (e.g. bitslide, see Q.2 and P.4.2)
  6. Timestamping Clock is the Local PTP Clock
Options required/prohibited by HA Profile

Required and active by default:
- L1-based sync. performance enhancements [Annex O]
- Configurable correction of timestamps [16.7]
- Calculation of the <delayAsymmetry> for certain media [16.8]
- Requirements of Q.3 [Annex Q]

Required and inactive by default:
- Mechanism for external config. of a PTP Instance’s PTP Port state [17.6]
- masterOnly mode [9.2.2.2 & 8.2.15.5.2]

Prohibited:
- Isolation of PTP Instances [16.5]
External config. of PTP Port state & masterOnly

• Best Master Clock Algorithm (BMCA) defines the state of each PTP Port in BC/OC and synchronization hierarchy in the entire PTP Network

• **Mechanism for external config. of a PTP Instance’s PTP Port state:**
  – Disables BMCA and affects all PTP Ports on a PTP Instance
  – Allows configuring the desired state of each PTP Port
  – Defines externalPortConfigurationPortDS dataset to store the desired state
  – Provides external configuration of synchronization hierarchy in the entire PTP network

• **masterOnly mode on PTP Port:**
  – Maintains operation of BMCA and provides configuration per PTP Port
  – Results in PTP Port ignoring Announce messages and defaulting to Master state
  – Prevents PTP Instance from “slaving” on particular PTP Ports (e.g. access ports)
Options required/prohibited by HA Profile

Required and active by default:
• L1-based sync. performance enhancements [Annex O]
• Configurable correction of timestamps [16.7]
• Calculation of the <delayAsymmetry> for certain media [16.8]
• Requirements of Q.3 [Annex Q]

Required and inactive by default:
• Mechanism for external config. of a PTP Instance’s PTP Port state [17.6]
• masterOnly mode [9.2.2.2 & 8.2.15.5.2]

Prohibited:
• Isolation of PTP Instances [16.5]
Inter-operation with Default PTP Profiles

- **High Accuracy Delay Request-Response Default PTP Profile**
  - Inter-operation with Delay Request-Response Default PTP Profile
  - Inter-operation with Peer-to-Peer Default PTP Profile, if peer-to-peer mechanism supported
  - No inter-operation with Transparent Clocks
  - No enhancements of synchronization performance

PTP Port in Master state:
- High Accuracy Default PTP profile
- Request-Response Default PTP Profile

PTP Port in Slave state:
- Request-Response Default PTP Profile
- High Accuracy Default PTP profile

Operation as if connected to a Request-Response Default PTP Profile
Operation as if it was Request-Response Default PTP Profile
High Accuracy model of Local PTP Clock

High Accuracy Local PTP Clock in J.5.5 – highlights:

- **Syntonization of Local PTP Clock**
  - Physical to the Grandmaster, e.g. L1 clock signal
  - Independent from the PTP timing message exchange
- **Synchronization of Local PTP Clock using PTP timing messages**

![Diagram of Local PTP Clock](image-url)
High Accuracy model of Local PTP Clock

PTP port in the **master** state

- Local PTP clock
- Master time

PTP messages

PTP synchronization

L1 syntonization

Phase detector

\[ x_{tx_A} \]

Medium

PTP Port in the **slave** state

- Local PTP clock
- Master time

Phase shifting PLL

\[ x_{rx_B} \]

Local PTP Clock physically syntonized to the Master Clock and synchronized via PTP

Clock signal physically syntonized to Master Clock’s timescale (e.g. L1 rx clock signal)