SPEC7 & HPSEC
When Low Phase Noise matters

11th WR online workshop, October 6-8, 2021
SPEC7\textsuperscript{[1]}

\textsuperscript{[1]} https://ohwr.org/project/spec7/wikis/home

photograph: Gino Hoft
SPEC7 Features

- Zynq-7000 XC7Z035 FPGA
- Processing System (PS)
  - Dual-Core ARM
  - 2-lane PCIe Gen2 (1GB/s)
  - Ethernet 10/100/1000 Mbps
  - USB2.0 (type-A)
  - mini USB (type B) => Dual UART (PS/PL) interface
  - micro SD slot
  - 512 Mb QSPI (boot and configure PL)
  - 2x 1GB DDR3
  - EUI-48 (PS MAC)

- Programmable Logic (PL)
  - WR Low Phase Noise VCXO’s and DAC
  - 10 MHz 1 ppm TCXO (IEEE1588-2019 I.5.6.1)
  - SFP cage
  - FMC (LPC connected)
  - EUI-48 (WR MAC)
  - 64 Kb EEPROM
  - Bulls-Eye connector
  - 2x Fan interface (FMC & FPGA)
SPEC7 PL configuration\[2\]

1. Tandem PROM (from QSPI)
   - stage 1: spec7_tandem_boot
   - stage 2: spec7_ref_design

2. UBoot => load bitfile to DDR from:
   - USB
   - Ethernet
   - microSD-Card
   - QSPI
   OR
   - PCIe write bitfile

3. UBoot
   - Configure PL from DDR
   - Update QSPI from DDR

...and of course also PL configuration via JTAG.

SPEC7 Tandem Boot\(^3\) from QSPI

**spec7\_tandem\_boot** →

**spec7\_ref\_design** →

<table>
<thead>
<tr>
<th>spec7_tandem_boot (pcie_7x) 1(^{st}) stage</th>
<th>PCIe</th>
<th>Size</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory BAR0</td>
<td></td>
<td>1MB</td>
<td>Reserve the memory space for enumeration &lt; 100 ms</td>
</tr>
<tr>
<td>memory BAR2</td>
<td></td>
<td>64KB</td>
<td></td>
</tr>
<tr>
<td>memory BAR4</td>
<td></td>
<td>16MB</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>spec7_ref_design (XDMA) 2(^{nd}) stage</th>
<th>PCIe</th>
<th>Size</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>XDMA AXI Lite Master</td>
<td>1MB</td>
<td>WR Load DPRAM, WR UART, UART to UBOOT</td>
<td></td>
</tr>
<tr>
<td>XDMA AXI-Stream</td>
<td>64KB</td>
<td>DMA</td>
<td></td>
</tr>
<tr>
<td>XDMA DMA Bypass</td>
<td>16MB</td>
<td>Load bitfile to DDR</td>
<td></td>
</tr>
</tbody>
</table>

\(^3\) [https://www.xilinx.com/support/documentation/ip_documentation/pcie_7x/v3_3/pg054-7series-pcie.pdf](https://www.xilinx.com/support/documentation/ip_documentation/pcie_7x/v3_3/pg054-7series-pcie.pdf)
Low Phase Noise: PCB Layout!

- Implement “island of silence” (GND plane cutouts)

PLL

Low Phase Noise
WR VCXO: 125.000 MHz

124.992 MHz
Low Phase Noise: Use SMPS with integrated MOSFET & Inductors

- Keep high current loops as small as possible to minimize EMI

12V => 3V3@10Amp

1V35, 1V35, 1V8, 2V5@4Amp

12V => 3V3@10Amp
Low Phase Noise: FPGA Core
Supply VCCINT via low noise LDO

VCCINT 1V0@4Amp Via LDO 1V35 PreCore
Low Phase Noise: Use differential Signaling

VCXOs single ended LVCMOS
Abracon:
ABLNO-V125.000MHZ

VCXOs differential LVPECL
Crystek:
CVPD-922-125.000

Mix products 7.6 KHz DMTD @ -90dBm
SPEC7 Phase Noise:

10 MHz Phase Noise (*)

-106 [dBc/Hz] @ 10Hz

Connected to another SPEC7(**)

(*) 10 MHz generated on FPGA; no re-clocking
(**) SPEC7 in mode master running on clean external 125MHz clock
**SPEC7 WR node**

**Default use**

- **On board VCXOs**
  
  **Crystek CVPD-922**

<table>
<thead>
<tr>
<th>Phase Noise @ 100 MHz</th>
<th>(°)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 Hz</td>
<td>-85 dBc/Hz Typical</td>
</tr>
<tr>
<td>100 Hz</td>
<td>-115 dBc/Hz Typical</td>
</tr>
<tr>
<td>1 kHz</td>
<td>-145 dBc/Hz Typical</td>
</tr>
<tr>
<td>10 kHz</td>
<td>-155 dBc/Hz Typical</td>
</tr>
<tr>
<td>100 kHz</td>
<td>-160 dBc/Hz Typical</td>
</tr>
<tr>
<td>1 MHz</td>
<td>-162 dBc/Hz Typical</td>
</tr>
<tr>
<td>10 MHz</td>
<td>-162 dBc/Hz Typical</td>
</tr>
</tbody>
</table>

(°) Phase noise figure is 20 dB higher when comparing 100 MHz oscillator with a 10MHz oscillator.
SPEC7 WR node

Default use

- On board VCXOs
  Crystek CVPD-922

Phase Noise @ 100 MHz: (*)

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>Phase Noise (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 Hz</td>
<td>-85 Typical</td>
</tr>
<tr>
<td>100 Hz</td>
<td>-115 Typical</td>
</tr>
<tr>
<td>1 kHz</td>
<td>-145 Typical</td>
</tr>
<tr>
<td>10 kHz</td>
<td>-155 Typical</td>
</tr>
<tr>
<td>100 kHz</td>
<td>-160 Typical</td>
</tr>
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<td>1 MHz</td>
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</tr>
<tr>
<td>10 MHz</td>
<td>-162 Typical</td>
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</tbody>
</table>

(*) Phase noise figure is 20 dB higher when comparing 100 MHz oscillator with a 10MHz oscillator.
SPEC7 WR node
Using External High Precision Ultra Stable OCXO

- Morion MV336
SPEC7 WR node
Using External High Precision Ultra Stable OCXO

- Don’t waste the excellent Phase Noise figure!
- Let WR control the phase of the 10 MHz OCXO
- Currently the 10 MHz OCXO has **25 arbitrary phase positions** w.r.t. 125 MHz WR Clk
- **Need a hardware handle to PPSI to** shift 10MHz OCXO until phase aligned with *THE* 1 WR RefClk phase position.
HPSEC7[^4]

**High Precision Secondary External Clock**

- High Precision Ultra Stable Oscillator (Morion MV336)
- FMC to DAC LVDS
- SPEC7
- Timing signals

[^4]: [https://ohwr.org/project/hpsec/wikis/home](https://ohwr.org/project/hpsec/wikis/home)
HPSEC Features[4]

- Ultra Stable 10MHz Oven Controlled Crystal Oscillator (OCXO)
  - Morion MV336
  - Separate 24V input for UPS
  - 3x 10 MHz outputs
  - 1x 100 MHz output
  - 1x Arbitrary frequency output
  - 1x input for 1GHz external timescale
  - re-clocking FlipFlops

HPSEC Phase Noise:

-135 [dBc/Hz] @ 10Hz
Connected to WR LowJitter switch

(*) 10 MHz from OCXO (no re-clocking!)
Funding information and Acknowledgements:

- This project 17IND14 WRITE has received funding from the EMPIR programme co-financed by the Participating States and from the European Union's Horizon 2020 research and innovation programme.

- People involved:

  - Guido Visser, Peter Jansweijer: hardware design
  - Charles Ietswaard: PCB layout
  - Pascal Bos: PCIe interface, PS booting and driver software design
  - Nayib Boukadida: Absolute Calibration
  - Ton Damen: Driver software
  - Kenny Lam: Heatsink design
  - Wim Gotink, Gino Hoft: Mechanical design
  - Mamta Ramendra Shukla, Juan David Gonzalez Cobas: PCIe interface, PS booting and driver software design
  - Grzegorz Daniluk, Tomasz Wlostowski: wrpc-v5 support
  - Javier David Garcia Lasheras: PCIe interface, PS booting and driver software design
Soon: SPEC7 v3 with improved heatsink

(*) This picture is still SPEC7 version 2; version 3 with heatsink is being produced.

Low Phase Noise: Use SMPS with integrated MOSFET & Inductors

PRODUCT DISCONTINUANCE NOTIFICATION
PDN 2133

due to Intel decision to exit the Enpirion power business.

Apparently Intel is an unreliable partner!
Summary

• Low phase noise possible with careful design

• We need a PPSI handle to shift external OCXO until it is aligned with the proper 125MHz WR Phase Aligned Reference clock.

• Fundamental discussion on lifecycle of components
Thank you
Backup Slides
**HPSEC MDEV:**

- **Goal:** $1 \times 10^{-13} \@ 100s$
- **Achieved:** $5.6 \times 10^{-15} \@ 100s$

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### Table

<table>
<thead>
<tr>
<th>Tau</th>
<th>Sigma(Tau)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1s</td>
<td>1.73E-12</td>
</tr>
<tr>
<td>2s</td>
<td>4.91E-13</td>
</tr>
<tr>
<td>4s</td>
<td>1.46E-13</td>
</tr>
<tr>
<td>8s</td>
<td>1.86E-14</td>
</tr>
<tr>
<td>16s</td>
<td>4.16E-14</td>
</tr>
<tr>
<td>32s</td>
<td>1.92E-14</td>
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<tr>
<td>64s</td>
<td>1.62E-14</td>
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<tr>
<td>128s</td>
<td>1.46E-14</td>
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<tr>
<td>256s</td>
<td>1.31E-14</td>
</tr>
<tr>
<td>512s</td>
<td>1.15E-14</td>
</tr>
<tr>
<td>1024s</td>
<td>5.53E-15</td>
</tr>
<tr>
<td>2048s</td>
<td>1.79E-15</td>
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<tr>
<td>4096s</td>
<td>1.06E-15</td>
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<td>262144s</td>
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<td>5.20E-17</td>
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<td>1048576s</td>
<td>4.11E-17</td>
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<td>2097152s</td>
<td>2.09E-17</td>
</tr>
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<td>4194304s</td>
<td>1.86E-17</td>
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<td>8388608s</td>
<td>2.51E-17</td>
</tr>
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</table>

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**Trace Notes**
- **Input Freq:** 16 MHz
- **ENBW:** HPSEC
- **MDEV at 100s:** 5.53E-15
- **Duration:** 14 d
- **Elapsed:** 13 d 17 h 57 m
- **Acquired:** 11950303 pts
- **Instrument:** 53100A

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