Next generation WR Switch v4

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Agenda

• Aim of the project
• A bit of history
• Hardware Specification
• Clocking circuit
• Ongoing activities, short and long term plans
• Conclusions
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• **Conclusions**
Goal of the next generation WRSv4 project

Create a new WR Switch that

• Supports 10 Gbps (data and time)
• Serves as drop-in replacement for WRS-v3
• Provides industry-level reliability features
• Meets needs of the WR Community
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A bit of history

- **2014/03**: First idea of next generation 10 Gbps switch
- **2016/07**: First collection of input from WR community via wr-dev mailing list
- **2018/10**: Second collection of input from WR community at the 10th WR Workshop
- **2018/10**: Start design study to prepare *Technical Specification*
- **2020/06**: Design study completed, *Technical Specs* presented at New WRS 4 Workshop
- **2020/10**: Clocking FMC design review completed
- **2020/11**: WR community feedback addressed, *Technical Specification* published
- **2021/02**: Main board schematics design first review and Clocking FMC delivered to CERN
- **2021/04**: Enclosure mechanical design first review starts
- **2021/08**: All components for the main board ordered
- **2021/10**: Enclosure mechanical design review completed
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Hardware specification

• Defined in “Hardware Specifications of the WR Switch version 4” (2021-01-15)
• Based on
  – Preliminary study of input from the WR community, CERN IT (2018-2019)
  – WRS resource utilisation on Xilinx US+ FPGA (2019)
  – Study on the new Hardware features for the WRS-4 (2020-04-01)
  – Study on the WRS-4 main board (2020-06-09)
  – New WRS 4 Workshop (2020-06-26)
  – WR Community feedback resolution (2020-11)
  – WRS-v4 expansion connectors study (2020-11)
• Special attention paid to the final price of WRSv4 (estimated at ~150% of WRS3)
• Defines:
  – Hardware features: enclosure, fans, power supply, front panel and expansion board
  – Main board: architecture, features and specification
Enclosure

- 19” rack-mountable 1U (height: 44.45 mm, wide: 482.6 mm, depth: 310 mm)
- Design review by CERN’s Mechanical Design section
  https://ohwr.org/project/wr-switch-hw-v4/wikis/enclosure
- Extension slot
- Separate airflow for mainboard and PSU (and optionally expansion board)
Fans

- Hot-swappable and self-docking module with a simple bracket
- 4 fans per module
- Configurable airflow direction (mechanical adjustment)
- Adjustable speed controller
- Broken rotor protection
- PWM control
- Tachometer
Power Supply

- Redundant and hot-swappable
- ATX standard compliant connectors
- Size allowed: 215 x 106 x 42 mm (accommodates units from different vendors)
- PMBus included
- The selected power supply unit is the YH5151-1EBR

*For applications without need for redundancy, a simple power supply can be installed*
• Clocking connectors:
  – 5 SMA connectors - inputs: PPS, 10 MHz; outputs: PPS, 10 MHz, AUX (abscal)

• WR SFP ports:
  – v4.0 (HW prototype), the configuration will be 24 stacked SFP+ connectors:
  – v4.1 (1 Gb only) will have 18 ports (or 20 if the old GW ok):
  – v4.2 (1 & 10 Gb) will have 20 ports if we can have 1 & 10 Gb on the same port, otherwise 20x1Gb and 4x10Gb
  * The main board will be prepared for 24 ports, since there is compatibility of SFP cages with different number of slots

• Management:
  – 1 SFP Port
  – 2 USB: 1 x Type C and Type A connector
  – 2 RJ45: 1 x Ethernet port and RS-232
  – 3 buttons: 1 x reset and 2 x next to the OLED display
  – 3 status LEDs: Red and Green status
  – 1 OLED display
Expansion board

• Aimed at providing new functionalities (e.g. holdover capabilities or high-performance oscillators).

• Expansion board characteristics
  – Size: 85 x 235 mm, overhead space: 32 mm
  – Pluggable from the rear panel
  – By default, airflow circulation ensured by the main fans via air guide; optionally, separate airflow circulation can be implemented
  – It can work as an FMC carrier at the same level as the main board

• Expansion connector
  – Single connector with 300 pinout (up to 28+ Gbps support)
  – FMC LPC compatible (68 user-defined pins + other as required by FMC)
  – High speed data I/Fs: 4 GTH and 16 GTY ports (45 diff-pairs to GTH/GTY quads)
  – SAMTEC SEAF-SEAM
Main Board architecture

- **Xilinx Zynq Ultrascale+ XCZU17EG-1FFVC1760E**
  - Quad-core ARM® CortexTM-A53 MPCore up to 1.5GHz
  - Dual-core ARM® Cortex-R5 MPCoreTM up to 600MHz
  - 32 GTH 16.3Gb/s and 16 GTY 32.75Gb/s
  - 28.0 Mb of BRAM and 28.7 Mb of UltraRAM

- **On board memory:**
  - SO-DIMM module with a capacity of 4GB
  - File system memory (single footprint)
    - Prototype: 1x SD memory card (8 GB) for booting and file system
    - Final version: 1x eMMC (4 GB and Industrial range)
  - 2x Dual serial NOR flash Quad-SPI memory (2 x 1Gb) for booting and to implement a recovery system.
  - 1x I2C Serial EEPROM (64K - 8K x 8-bit) for storing serial number, calibration parameters and other critical data.
  - 1x m.2 SATA interface is provided for SATA SSD access
  - Internal UFL connectors: clk-in, clk-out (62.5 MHz)
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Clocking Circuit

- Supports: 125MHz for 1G, 156.25 for 10 G, clock provided from Extension Board
- Includes improvements of Low Jitter WRS – comparable performance
- **Issue**: GM input stage temp-dependence ~6 ps / Celsius degree
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Ongoing activities

• **Hardware**
  – Enclosure design by [7Sols](https://ohwr.org/project/wr-switch-hw-v4/wikis/enclosure)
    • Implementing improvements
  – Validation of the clocking circuit (using FMC) by [7Sols](https://ohwr.org/project/wr-switch-hw-v4/wikis/enclosure) – about to be completed
  – Main board schematics design by [7Sols](https://ohwr.org/project/wr-switch-hw-v4/wikis/enclosure)
    • Preliminary review completed, final review pending validation of the clocking circuit using the FMC
    • Final schematics review in October 2021 – join!
      [https://ohwr.org/project/wr-switch-hw-v4/wikis/wrs-v4-main-board-schematics](https://ohwr.org/project/wr-switch-hw-v4/wikis/wrs-v4-main-board-schematics)

• **HDL**
  – Network Interface IP Core (NIC) with 10Gbps support by [Latgate Limited](https://www.latgate.com) – ongoing conceptual design
  – Forwarding Engine with 10Gbps support (i.e. RTU IP Core) by [M. Zarychta](https://www.mzarychta.com) within MSc Thesis – implemented

• **SW**
  – Linux environment for US+ prepared by [A. Wujek/CTI](https://www.ctl concessions.com) – for another project, foreseen also for WRSv4 ([https://ohwr.org/project/diot-sb-zu/](https://ohwr.org/project/diot-sb-zu/) not yet in the master branch)
Short-term plans

• **Hardware**
  – Layout by **CERN**: end of 2021
  – Prototype production by **7Sols**: Q1 2022 (all components ordered, should arrive before end of 2021*)

• **HDL**
  – Network Interface IP Core (NIC) with 10Gbps support by **Latgate Limited**: ready ~Q1 of 2022
  – CERN Fellow to work on HDL: 2022-2023

• **SW**
  – Work will start when hardware and basic HDL available: Q2/Q3 2022

* One component’s delivery date was moved to March 2022, looking for alternatives (supplier/component)
Long-term plans

2022/Q1 – **First hardware prototype** of the main board and enclosure

2022/Q2 – Board Support Package & basic gateware for the new HW

2022/Q4 – Production Test Suite

2022/Q4 – Port of (as much as possible) SW and HDL to new HW (1Gb)

2023/Q1 – **Second hardware prototype** of the main board and enclosure

2023/Q2 – Release v1 of WRS-4 with 1 Gb for timing/data (might be skipped)

2023/Q3 – **Final hardware** available

2024/Q4 – Release v2 of WRS-4 with 10Gb for timing and data

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**Important note**

- Component lead-times even: >6 months
- Components for the second prototype need to be ordered soon
- If you want to secure the second prototype, pre-order at latest Q1 2022
- Poll to judge interest in buying
  - Second prototype
  - The final product
Strategy for WRS-4 dev. And WRS-3 support

- Incremental GW/SW design of WRS-4
  - First: 1G time and 1G data
  - Second: 10G time and 1G data
  - Third: 10G time and 10G data
- HW published under CERN Open Hardware Licence Version 2 - Weakly Reciprocal
- Long-term support for WRS-3 (large installed base)
  - No foreseen end-date for support but production depends on components availability
  - Lock HW/GW of WRS-v3 – no new features added
  - Very likely, the SW (PTP, RTU, etc daemons) will be common to WRS-3 and WRS-4
    - SW new features for WRS-3 only in common SW, if HW/GW support available
    - Bug-fixes for WRS-v3
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- Hardware Specification
  - based on thorough studies and
  - tuned to WR Community needs
  - expected price of WRSv4 = ~150% of WRSv3
- Clocking circuit using FMC validated
- Design of hardware (main board and enclosure) well advanced, everyone welcome to join main board final review
- Mitigating component long lead-times by advanced orders