WR Nodes using Altera FPGAs

Stefan Rauch
BEL
http://bel.gsi.de
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Essential parts of an WR Receiver

- WR clock circuitry (VCXOs, DACs, PLL)
- SFP slot
- FPGA with gigabit PHYs
WR clock mezzanine

- 25Mhz VCXO
- 20Mhz VCXO
- PLL
- 2x DAC
- Voltage reference
HW Platforms with Altera Arria II

- SCU
- Exploder
- Pexaria with Blackcat mezzanine
SCU

- Scalable Control Unit
- SCU bus
- 32Mbyte Flash
- 128Mbyte DDR3
- 2x SFP
- 2x LEMO IO
- 2x EIA232
- ComExpress Module with Intel Atom
- WR clock circuit
Status: working
Exploder

- 4x SFP
- Mezzanine Slots for IO Board
- Slot for WR Clock Mezzanine

Status: working
Pexaria

- 4 lane PCIe
- 4x SFP
- Extension Board (Blackcat) with WR clock mezzanine
Status: not yet working
Questions?