WR PTP Core block diagram

Memory Mapped
User Application IO
WR PTP Core block diagram

Streaming IO
User Application IO

PHY + PCS (GTP)
Timing System block diagram
(With Phase offset)

\[
f_{\text{out}} = \frac{n}{n+1} f_{\text{in}}
\]

(\(f_{\text{out}}\) = Helper PLL or DMTD Clock)