White Rabbit Switch gateware
status and plans

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Agenda:

1. Current release
   - HDL architecture
   - Timing modules
   - Ethernet switching
   - WR Endpoint

2. Work in progress
   - RMON counters
   - Endpoint modifications
   - Switching Core
   - Routing Table Unit
   - Topology Resolution Unit
   - Resource Utilization
HDL architecture

- first stable release for v3 of the hardware (tag: `wr-switch-sw-v3.0`);
- runs on Xilinx Virtex 6 (XC6VLX130T) but is fully generic, no vendor specific IP-cores required;
- Wishbone bus between all HDL modules;
- internal packets flow using pipelined Wishbone.
Timing modules

- software PLL implementation (LM32 + SoftPLL);
- SoftPLL the same as in WR PTP Core;
- current time stored in PPSgen block;
- SPI, Serial DAC interface for clock tuning;
- TX timestamps, frame IDs, port IDs stored in FIFO.
Endpoint: Ethernet MAC implementation with precise timestamping;
RTU: switching decisions for 18 WR Ports and internal NIC;
SwCore: actual Ethernet frames switching;
NIC: packets from/to main CPU.
RMON counters;
Endpoint modifications;
Switching Core - new functionality;
Routing Table Unit - optimized;
Topology Resolution Unit.
direct counting consumes lots of resources;

algorithms for approximate counting - use very little resources but cannot produce accurate statistics;

Counter Braids seems to be the perfect solution.
Counter Braids

- each event increments more than one counter;
- few levels of small counters (most often 2-3 levels);
- overflowing counter on 1st level increments multiple counters on 2nd level;
- decoding done in software
Endpoint modifications

PHY side

8-bit serdes (GTP)
16-bit serdes (GTX)
MII, GMII

Physical Coding Sublayer

PHY Interface

TX Path
CRC insertion
STP/BRU packet injection
egress VLAN unit
OOB parser

TX FIFO

RX path
802.1 header decoder
packet filter & classifier
status/OOB append
CRC/size checker
ingress VLAN unit
RX elastic buffer

RX FIFO

Timing unit

Flow control
RMON triggers
Control regs

Host side

WB Slave (TX input)
WB Master (RX output)
RTU requests (switch only)
TX timestamps
1-PPS input

Pipelined Wishbone Interface

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Switching Core

- optimization (wire speed)
- separation resources for HP traffic
- improvement output queues scheduling (decoupled)
- implementation of time-triggered output scheduling
- interface with TRU
Routing Table Unit

- fully deterministic and non-dropping for HP traffic
- Fast Match Engine
  - PTP/broadcast/Link-limited/configurable MACs traffic
  - configurable hardware support for HP traffic
  - response in max \((N+5)\) cycles
  - interface with TRU
- port
  - port mirroring
  - drop/broadcast when full match too slow
Topology Resolution Unit

- universal unit for topology resolution protocol
  - port switch-over between redundant ports (eRSTP)
  - traffic distribution between redundant ports (eLACP)
- fully pipelined (3 cycles to answer, each cycle new request)
## Resource Utilization

<table>
<thead>
<tr>
<th>Feature</th>
<th>Resource utilization [%]</th>
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<th>Bigger FPGA</th>
<th>Current FPGA</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>18 ports</td>
<td>18 ports</td>
<td>8 ports</td>
<td>18 ports</td>
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<td></td>
<td>LUTs</td>
<td>Slices</td>
<td>RAM</td>
<td>LUTs</td>
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<td>Master v3</td>
<td>42</td>
<td>57</td>
<td>37/9</td>
<td>79</td>
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<td>RTU optimization</td>
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<td>64</td>
<td>50/11</td>
<td>90</td>
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<td>Master v3</td>
<td>53</td>
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<td>RTU optimization</td>
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<td>Endpoint new features (VLAN, flow control)</td>
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Thank you