Frequency distribution based on White-Rabbit for LLRF applications
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SERVICES

- **Custom electronics design**: PCB (carriers, FMCs, XMCs, ...), Time and RF distribution equipment, dependable and safety critical platforms.

- **Embedded systems programming**: DSPs & SoC software, FPGA gateware, drivers development, dependable firmware for safety-critical and industrial applications.

- **Electronics production externalization**: CE/FCC labeling, production test suites, quality control (IPC-610 rules).

- **Fast control and system integration**: Including HW/SW (VME, VPX/OpenVPX, XMC, CompactPCI, microTCA) and software APIs with EPICS.

- **Custom Timing Solutions**: Accurate calibration, OEM modules, FMC carriers & mezzanines, standalone nodes.
Our Products

- White Rabbit Switch to provide ultra-accurate synchronization.
- Nodes to provide White Rabbit timing.
- Starting kits that will ease the first contact with the White Rabbit technology.
- Embedded nodes designed to be integrated into your product as OEM module.
- PCI-e FMC carriers to bring White Rabbit to the user’s PC.
- IO cards to start playing with White Rabbit technology.
- FMC cards designed to produce precise pulse delays and accurate timestamps.
- Standalone node to achieve sub-nanosecond synchronization in your applications.
- and much more…
Frequency distribution based on White-Rabbit for LLRF applications
1. About Seven Solutions.

2. IFMIF/EVEDA Project
   - Brief review of the project.
   - Seven Solutions involvement: LLRF development and Timing distribution system

3. Time-related project requirements

4. 7S – LLRF

5. Conclusions
The International Fusion Materials Irradiation Facility (IFMIF) has been designed to test the materials to be employed in future deuterium-lithium fusion reactors.

**IFMIF/EVEDA:** A total nominal power of 2.65 MW will be injected in the Radiofrequency Quadrupole (RFQ), the Medium Energy Beam Transport (MEBT), and the Superconducting RF (SRF) cavities by means of 18 RF power chains:

- 8 RFQ of 200kW
- 2 MEBT of 16kW
- 8 SRF of 105kW
CIEMAT is responsible of IFMIF-EVEDA RF System: 18 three-stage amplifiers chain working at 175 MHz. Seven Solutions was recruited to provide:

- The Low-Level Radio Frequency (LLRF): responsible to control/tune the RF cavities in the accelerator. It also supports the synchronization, data logging and fast interlock system related to the RF cavities.

- And the **clock distribution** for BPMs.
1. About Seven Solutions
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3. **Time-related project requirements**
   - Clock distribution
   - Timing distribution
4. 7S – LLRF
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Time-related requirements

Clock distribution:
- Fan-out:
  - ✓ Analog and tested
  - ✓ Ease to install
- ✗ Need to characterize lines
- ✗ Oscillator price
- ✗ Temp. Derivation
- ✗ Not scalable

- White Rabbit 😊

130 mA 9 MeV deuteron beam
i.e. 1.2 MW beam power
16 RF chains 200 kW each (Ciemat)
RFQ 0.1 – 5 MeV (INFN)
SRF linac 5-9 MeV (CEA)
When an emergency stop occurs, data from all the systems, and especially from LLRFs, must be safely studied afterwards. Different speeds of samples are captured:

- **SDL**: Slow Data Logger which provides 1-10 samples/seconds (at to years)
- **FDL**: Fast Data Logger which provides 10K samples/seconds (at to 460sec)
- **RDL**: Raw Data Logger which provides up to 125M samples/seconds (at to 80usec)

This situation and sample speeds require a high precision system which provides the same time to all the systems (**Time distribution**) → **Again White Rabbit 😊**

Extra libraries to analyze LLRF data acquired →
1. About Seven Solutions
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   • Introduction
   • Hardware specifications
   • Functionalities
   • WR compliant (RF in phase)
   • User interface - EPICs.
   • RF distribution for RFQ cavities (under development)
5. Conclusions
The Low-Level Radio Frequency **LLRF** responsibilities:
- Control/tune the RF cavities.
  
  *through the three-stage amplifiers chain* →
- Different power generation depending on Cav. needs.
- Feedback loop to reach stability reqs.
- Fast interlock system

Add in **7S-LLRF**:
- Sub-nano synchronization and clock distribution
- Data logging and time stamping
- RF switch-off in less than 900ns
7S-LLRF HW Specs

Main Features
- Intel® Core™ i7, 2.53 GHz
- Dual-core 64-bit processor
- PICMG CPCI/3.0 CompactPCI Serial
- Up to 4 GB DDR3 SDRAM soldered, ECC
- mSATA and microSD™ card slots
- Standard front I/O: 2 DisplayPorts, 2 Gb Ethernet, 2 USB
- Standard rear I/O: 7 PCI®, 8 USB, 8 SATA, DisplayPorts/PEXI
- Rear I/O via mezzanine board: up to 8 Gigabit Ethernet
- Intel® Turbo Boost 2.0, 3.2 GHz, Hyper-Threading, Active Management Technology
- Open CL 1.1 support

www.sevensols.com Frequency distribution based on White-Rabbit for LLRF applications
Control loops:

- **Feedback loop (FB loop):** Control of the amplitude and phase of each cavity field at 175MHz. (bandwidth req. 10KHz)
- **Conditioning loop:** Manual and Automatic.
- **Beam Pulse (FF loop):** Manual and Automatic Feed-Forward loop.
- **Tuning Loops:** Control of the resonance frequency of the cavity. Two type of tuning:
  - Mechanical tuning: step motor control
  - Frequency tuning: modify the RF output frequency to avoid power reflection through the chain.

- **Emergency stop** (Fast interlocks control): Reception and processing of authorizations to suppress the excitation of the power amplifiers if required. The RF emergency stop when interlock is less than 900nsec.
- **Clock distribution and RF synchronization (White Rabbit)**
- **Signal diagnostic and post mortem analysis:** SDL, FDL, RDL (Extra libraries to process data saved)
- **Temperature compensation**
• RF direct acquisition and generation.
• General features and signal stability:

<table>
<thead>
<tr>
<th>Signal Stability</th>
<th>Features (stand alone mode)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LLRF control loop</td>
<td>Amplitude and phase loop by digital I/Q vector analysis</td>
</tr>
<tr>
<td>Analog Output</td>
<td>Nominal frequency: 175 MHz</td>
</tr>
<tr>
<td></td>
<td>Harmonics: &lt; -60dBc</td>
</tr>
<tr>
<td></td>
<td>Spurious: &lt; -65dBc</td>
</tr>
<tr>
<td>Analog Output (Amp. stability)</td>
<td>Max. Peak Amplitude error: &lt; ± 0.04% of full scale</td>
</tr>
<tr>
<td></td>
<td>Amp. Loop Bandwidth: &gt; 10KHz</td>
</tr>
<tr>
<td>Analog Output (Phase Stability)</td>
<td>Max. RMS Phase error: &lt; 0.08° (from 100Hz-1MHz)</td>
</tr>
<tr>
<td></td>
<td>Phase Loop Bandwidth: &gt; 10KHz</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>RF adjustable power: -54dBm &lt; X &lt; 13.9dBm</td>
</tr>
</tbody>
</table>
Time and clock distribution (WR):

- **WR_PTP_core (v2.1)** introduced as an independent part of the system.
- WR clock is the clock system distributed throughout all controllers, ADCs, and DAC devices.
- Time and PPS is also taken and used for time stamping.
LLRFs are connect through a customized user library to handle PCIe:

- Based on Windriver: support Win/Linux
- Direct FPGA register access
- DMA access to the DDR
- Handling Interrupt
7S-LLRF
User Interface

- CentOS 6
- EPICS 3.14.2
- Asyn, seq, autosave
- CSS/BOY (Jpython)

LLRF main controls →
### 7S-LLRF User Interface

**Synoptic:**
- Amplifiers chain power
- IOC sample rate: 5Hz
- Possibility to choose ADC channel shows
7S-LLRF
AsynWBdriver
library

A C++ library to ease the access to WB register:

>300 PVs per cavities

- Support different memory bridges (i.e, PCIe driver)
- Connect PV to WB field in a FPGA register
- Auto-generate the *.vhdl, *.db and *.h with a fork of wbgen2
- Automatic conversion: fixed point, signedness (2’s complement)

http://www.ohwr.org/projects/epics-wb
RF distribution for RFQ cavity based on WR (under development)

- **Req:** RFQ is controlled by 8 LLRFs that should run as a one.
- **Approach:** Master/Slave configuration
Brainstorm:
- Introduce **WR for automatic loop:**
  - FB loop
  - FF loop
  - Automatic Freq tuning.
- **HW EB Master** to reduce latency.
- Which is WB Master/Remote slave propagation time? → **FeedBack loop bandwidth**?
- **Data rate**? Without compromising synchronization.
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Conclusions

- We have developed a scalable LLRF for a IFMIF/EVEDA facility in collaboration with CIEMAT.
- The LLRF is totally digital: ADC and DAC works with 175MHz directly (No IF).
- We use **White Rabbit** to distribute clock and time through the accelerator:
  - LLRF
  - BPMs
- User Interface to control **remotely** all LLRFs through EPICs.
- Plan to use WR for a **RF distribution** in the RFQ cavity (**under study**).
- **Tests** are on their way. 😊
Thanks for your attention!