1) Motivation and Goals
2) Timeline
3) Test System
4) Test Cases
5) Test Analysis
1) Motivation and Goals

2) Timeline

3) Test System

4) Test Cases

5) Test Analysis
Motivation for a WR test system

- Rather clear: complete WR functionality has to be checked and verified
- Proof of principles, proof of concepts
- Eventual needs for basic changes have to be identified as early as possible
- ...

Goals

- Verify (and understand) complete WR behaviour
- Identify reasonable WR parameters (FEC redundancy factor, subblock size etc.)
- Get accustomed with WR HW/SW/HDL, train further experts
- Test system results shall help for higher layer WR discussion
- Provide test environment for timing receivers and timing master
- Compare test results with simulation results
- ...

Timeline
- Effort and time demand for changes
- Possibility for major changes
1) Motivation and Goals

2) Timeline

3) Test System

4) Test Cases

5) Test Analysis
Stage I - 2009 (diploma thesis 06/09→12/09)

• Set-up complete test environment (analyzing / monitoring tools, eval. boards, switch prototypes)
• Main focus: PTP, HP packets, FEC (fail-safeness), copper/fiber connections, errors
• Definition of valid tests
  → problem e.g. how to proof HP errors $<10^{-15}$ in reasonable test time?

Stage II - starting 2010

• First "normal operation mode" tests (HP content, time pattern)
• Extend test system as much as possible (no scalability proof; simulations necessary)
• Test prototypes
  → timing receivers / FAIR front end controller
  → timing master
• Further / higher layer tests and definitions
  → SNMP, WR parameterization, SW/FW update, ...
  → connects/disconnects, power failures etc. on running timing system

Stage III - from autumn/winter 2010 on

• Integration in new (old) control systems
• Hot standby tests (master)
• Further timing receiver prototypes / form factors
1) Motivation and Goals

2) Timeline

3) Test System

4) Test Cases

5) Test Analysis
Main Ideas

- Run WR code on evaluation boards
- Add monitoring functionalities
- Add basic diagnostic features on board
  → push buttons, LEDs, display
- Write program to generate HP packets
- Define clear test cases in DB
- Run (semi-) automatic tests
- Put test results in DB
  → don't produce GByte of unnecessary data ;-)
- ....

- Extend test system with
  → switch prototypes
  → timing master
  → timing receivers
- Guide test system from childhood to adult
Evaluation Boards for Test System
(Altera Cyclone III EP3C120 dev. kit)

Test Definitions

Test Results

Analysing PCs (ODBC SW)

HP generator
(PC with Intel® PRO/1000 PT
Quad Port Server Adapter)
C++ / Java

PC
MySql DB

Test Results

10/100/1000 Quad-PHY HSMC
Daughter Board (morethanIP)

XPort
serial to ethernet
monitor interface

Push Buttons, LEDs, display to be used for test purposes

• 2nd Eval Board
• WR switch prototype

Test Definitions

Test Results

Push Buttons, LEDs, display to be used for test purposes
1) Motivation and Goals

2) Timeline

3) Test System

4) Test Cases

5) Test Analysis
Test Cases
General Categories

- Tests to verify monitoring functionality and test system interfaces
- Long tests that have to be run only a couple of times
- Tests that have to be run only once
- Short tests that have to be run a lot of times (necessary statistics)
- Tests that have to be run again after WR changes (dependency matrix)
- Tests to compare with simulation results
- Tests to answer open WR design questions
Test Cases
Functional Categories

Bandwidth Load Tests
- granularity window concept
- additional SP traffic
- normal ethernet transparency
- SNMP data
- inside µTCA communication
...

WR Specific Tests (Proof Of Concept)
- HP packets
  → broadcasts / "upward traffic"
  → collisions
  → SP fragmentation
time synchronization / PTP / determinism
redundancy uplink channel
WR messages
...

FEC Algorithm / LT Coding
- algorithm itself / XOR rules / distribution
- subblock size ↔ payload size
- redundancy
- packet encoding / decoding
...

Interface Tests
- timing master
timing receivers
outside world
...

Copper / Fiber Links, "BER" Tests
- 8b10b vs. trelis (→ sync. accuracy)
deliberate error creation
  → realistic statistics
...

Miscellaneous Tests
- connects/ disconnects
global switch parameterization
SW/ FW updates
...

T.Fleck, GSI
## Simple Example of a Test Description

**Test Case "Single HP frame" (Payload 1-bit error)**  

<table>
<thead>
<tr>
<th>Prerequisites</th>
<th>Description</th>
<th>Interface</th>
<th>Workflow</th>
</tr>
</thead>
<tbody>
<tr>
<td>No SP traffic</td>
<td>Simulates a 1-bit error in HP frame payload</td>
<td></td>
<td>1. Generate HP frame</td>
</tr>
<tr>
<td>No other HP traffic (no collisions)</td>
<td></td>
<td>Parameters:</td>
<td>2. Send &quot;Start CRC Test, error at n&quot; command to</td>
</tr>
<tr>
<td>HP flags = 0x00</td>
<td></td>
<td></td>
<td>Switch (XPort)</td>
</tr>
<tr>
<td>No LT encoding</td>
<td></td>
<td></td>
<td>4. Send generated HP frame to switch, save the</td>
</tr>
<tr>
<td>Constant payload ~ 200 Bytes</td>
<td></td>
<td></td>
<td>timestamp in DB</td>
</tr>
<tr>
<td>Test ID: 0x000000001</td>
<td>&quot;dropped&quot; flag</td>
<td></td>
<td>5. Switch sends debug info (XPort)</td>
</tr>
<tr>
<td>Topology: PC &lt;-&gt; Switch</td>
<td>(frame with CRC)</td>
<td></td>
<td>6. Send &quot;Stop Test&quot; command to Switch (XPort)</td>
</tr>
<tr>
<td></td>
<td>Frame ID</td>
<td></td>
<td>7. Wait until the Switch answers with &quot;OK&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>8. n + 1; repeat 2-8</td>
</tr>
</tbody>
</table>

---

*GSI*
1) Motivation and Goals

2) Timeline

3) Test System

4) Test Cases

5) Test Analysis
Test Analysis using Origin / ODBC to MySql

Scientific Analyzing Software ORIGIN

- Easy access to test DB
- no programming effort necessary
Test Analysis
using Origin / ODBC to MySql

Semiautomatic Analysis

- scripting window C like
- complete C programming IF
- easy generation of result graphs

Lost packets as a function of bit error rate and transmitted packets
Questions?

Thanks for your attention

Any Questions?