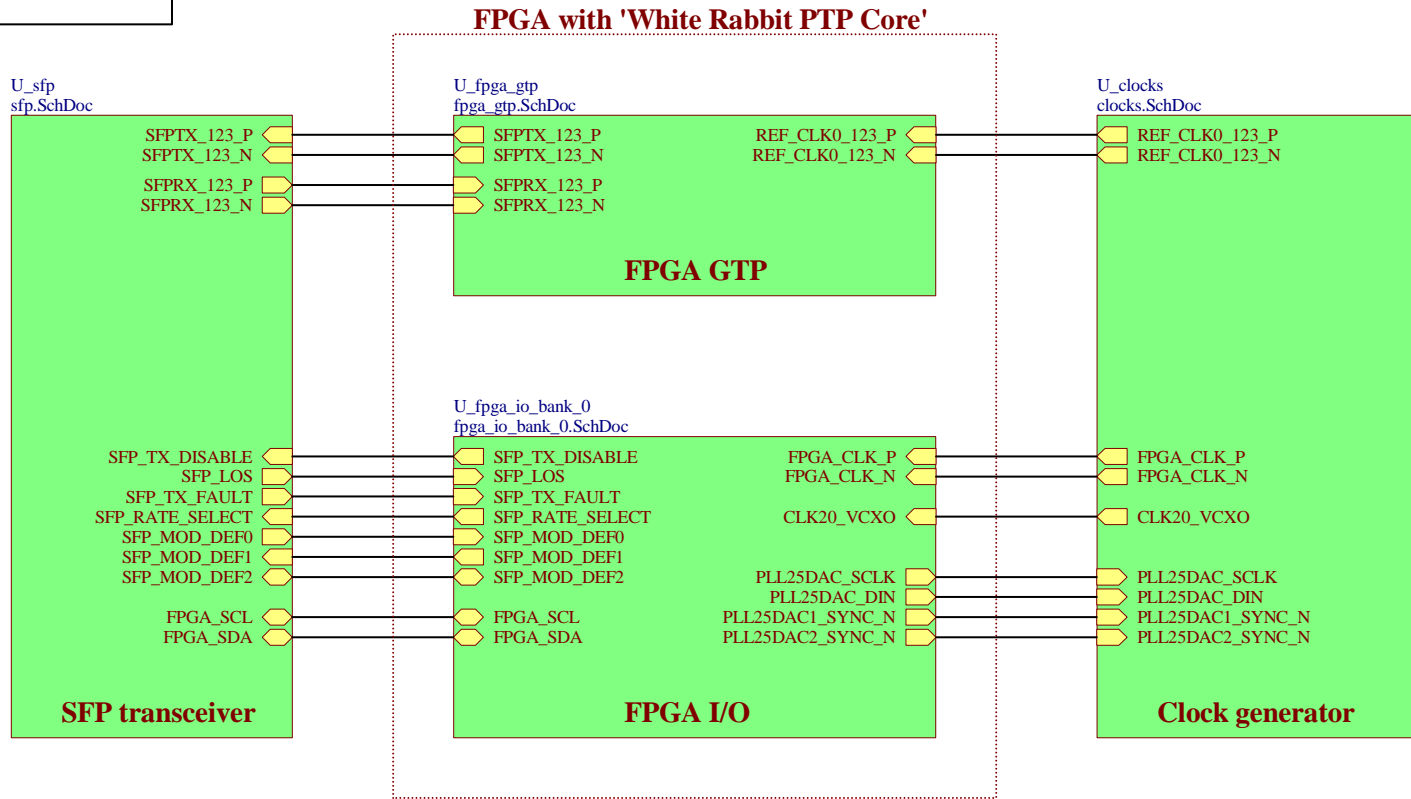


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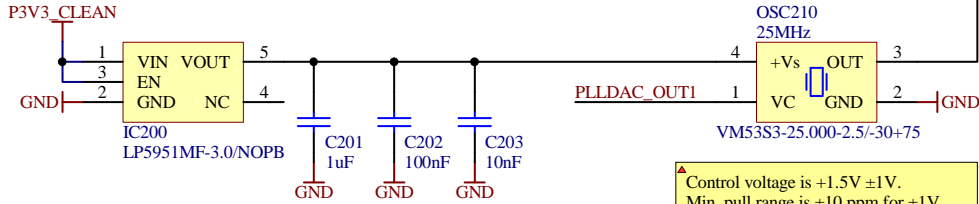


Detailed information see "<http://www.ohwr.org/projects/white-rabbit>"

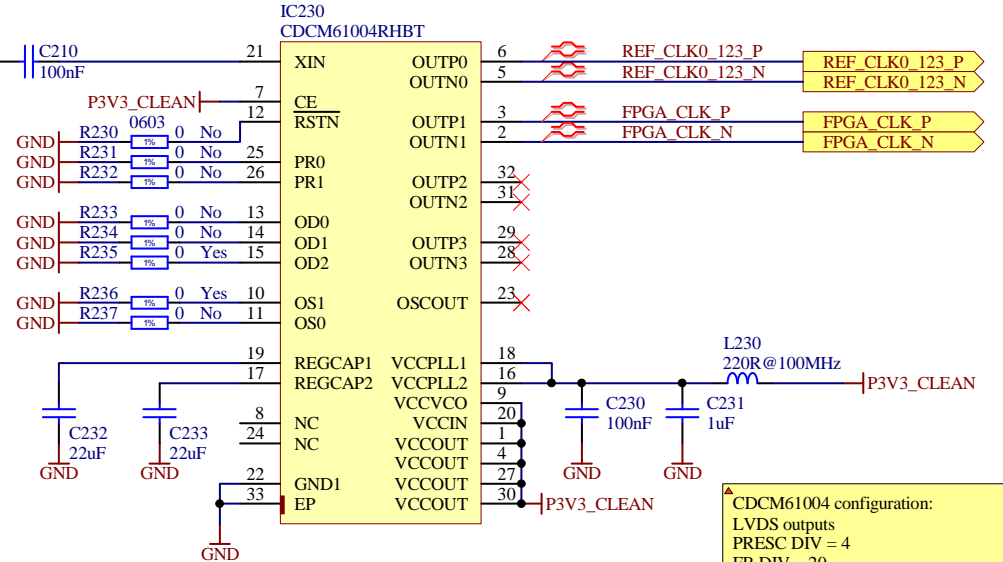
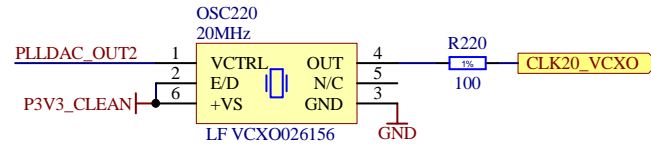
Top	
System: White Rabbit Node Reference Design (upgrade of existing system)	
Board: -	
Created: 07-MAR-2012, Daniel Florin	Revision: -
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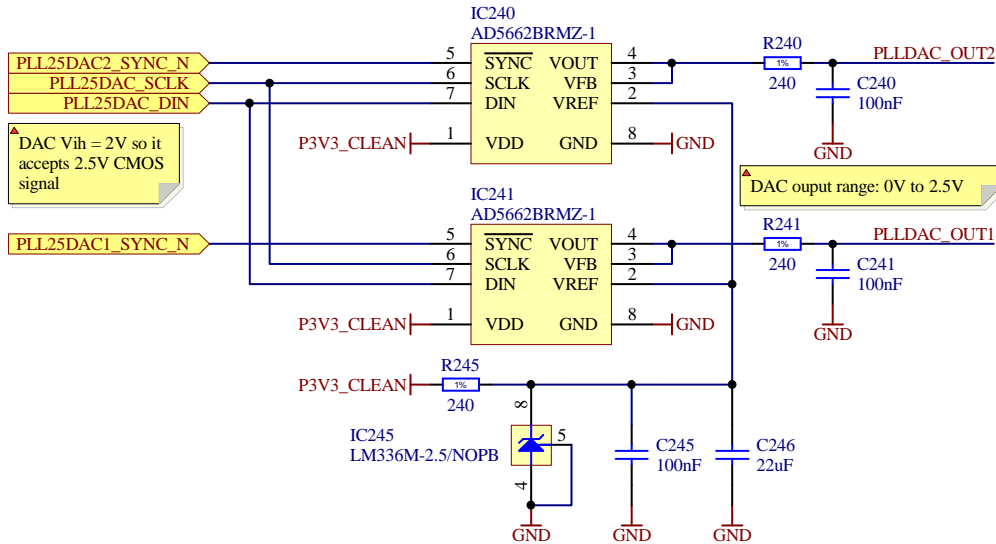


Control voltage is +1.5V ±1V.
Min. pull range is ±10 ppm for ±1V.
Positive slope (Positive voltage for positive frequency shift).

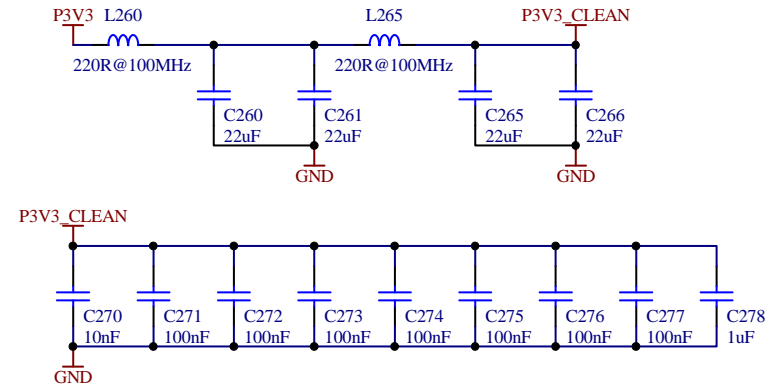


▲ CDCM61004 configuration:
LVDS outputs
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
All config inputs have internal pull-ups.

Input = 25 MHz
Output = 125 MHz



▲ DAC output range: 0V to 2.5V



Clocks

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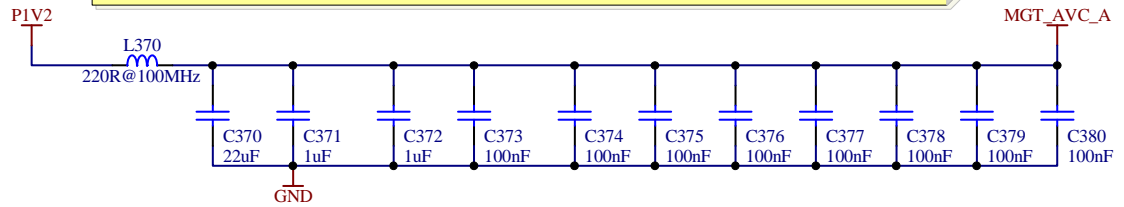
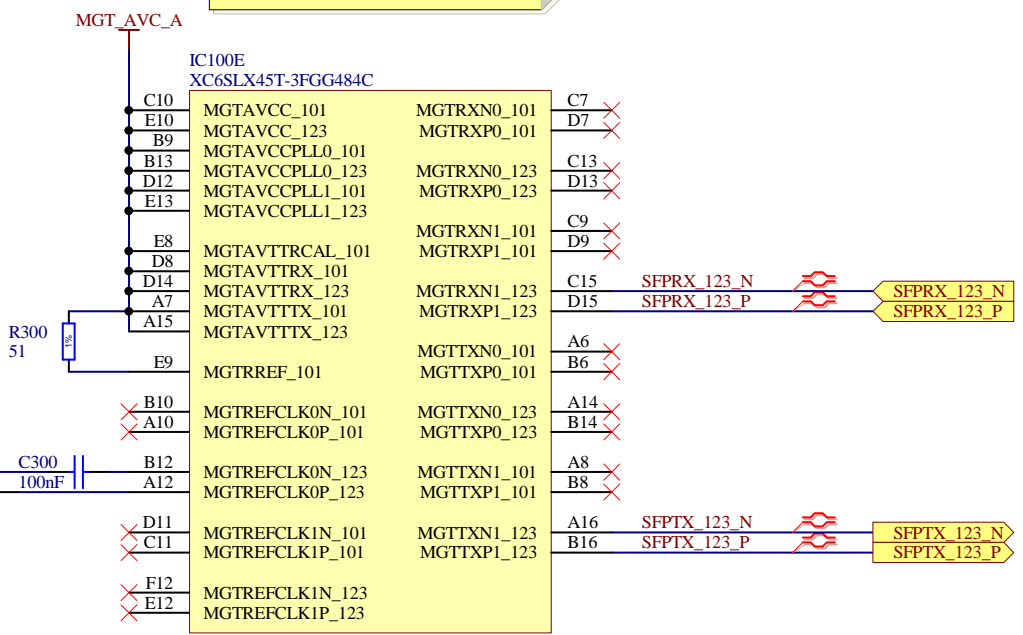
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▲ Only signals relevant for WR PTP shown...

▲ Calibration resistor traces must be equal in length and geometry.
See Spartan-6 FPGA GTP Transceivers; UG386.

▲ Reference clock, 125 MHz

▲ Power: GTPs power plane, and signal plane should be separated by a ground plane from any signal passing close.
The capacitor bank recommended for decoupling is described in: Xilinx user guide Spartan-6 FPGA GTP Transceivers (ug386.pdf). Chapter 5 Board Design Guidelines. Check Table 5-2: Recommended Minimum Decoupling for Spartan-6 FPGA GTPA1_DUAL Tiles and Figure 5-11: Stackup for GTP Power and Signal Layers.



FPGA GTP transceivers	
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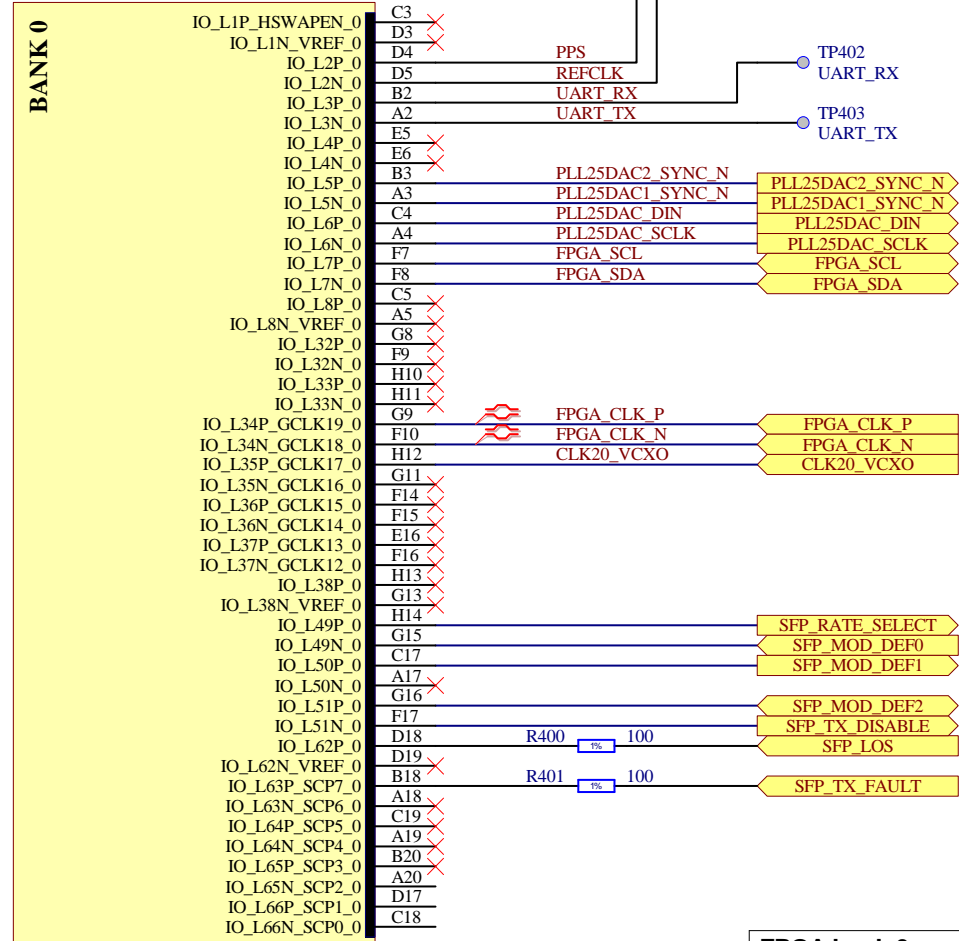
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▲ Only signals relevant for WR PTP shown...

VCCO_0 = 2.5V or 3.3V

IC100A
XC6SLX45T-3FGG484C



FPGA bank 0

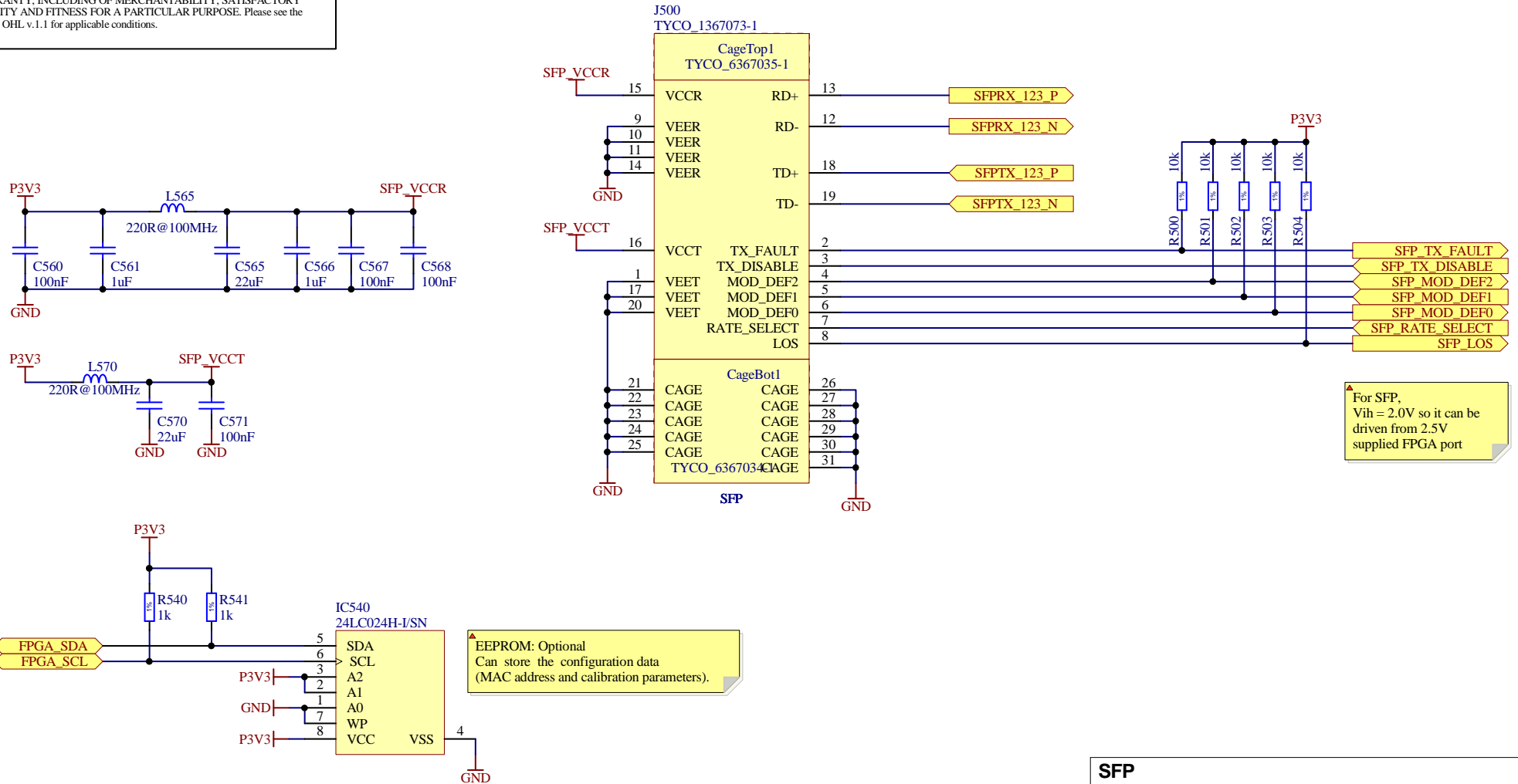
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Compliant SFP devices see "<http://www.ohwr.org/projects/white-rabbit/wiki/SFP>"



SFP	
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