White-Rabbit news from Seven Solutions

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Company overview

Seven Solutions

Seven Solutions (info@sevensols.com)
7S: The team

Direction – R&D
- Eduardo Ros
- Javier Díaz

Market & administration
- Miguel Ángel Reinoso
- Alicia Medina

Engineering & production
- Miguel Méndez
- Benoit Rat
- Gabriel Ramírez
- Rafael Rodríguez
- Santiago Navarro
- Rodrigo Agís
- Richard Carrillo
- Juan M. Lozano
- H. González
- Emilio Marín
- Ángel Tobaruela
- Felipe Torres
Company services & products

Services

- Electronics boards design and production
- Embedded software development (real-time, control...)
- HW/SW dependable systems & certification (DO-254, DO-178B, IEC-615)
- High-tech consulting & training
- Integration & turn-key solutions

Products

- Prototyping FPGA platforms (XircaV4, S400, SB, ViSmart, WR6)
- Custom electronic products: CODE, Sensonic, Ledlocal
- FPGA IP cores: Memory controllers, Ethernet UDP stack, motion detection, video-analytics, etc..
- White Rabbit products (Switch, SPEC, FMC DIO, FMC TDC; FMC ADC.....)
7S role in White Rabbit project

White Rabbit Switch

White Rabbit integrated solutions: production, customization, design, support and more...

BRIDGE (7S)
- Support
- Customization
- Production
...

OPEN HW/SW COMMUNITY

COMMERCIAL TECHNOLOGIES / FINAL CUSTOMERS
7S role on this stage

A) Continue support and product customization

B) Development of fully industrial products based on WR technology

- Improved test and quality procedures
- Board with extended temperature range (industrial range)
- Dependable solutions: redundancy mechanisms (network topologies, power supplies, fans, hardware), etc...
- Easier user interfaces & management
White Rabbit switch

3.4 HW, Firmware/Gateware, Boxes, ...
See HW, GW, FW, SW changes during switch talk

NEW BOXES (ONGOING WORK)
Target goals

- Improvement of WR switch box (similar to SPEC-BOX3N).
  - No extra cost
- Industrial box (probably not needed on many research facilities)
  - Based on in-deep study of current solutions and collaborations with leading companies.
  - Higher cost
Industrial Rackable Switches
INDUSTRIAL 18 Port WR-SWITCH DESIGN
“INDUSTRIAL SWITCH” (BETA)

SPECS:
- 1U Industrial chassis design based on the recommendations of the chassis leading manufacturers.
- Redundant hot swappable power supply modules.
- Up to 5 redundant hot swappable fan modules.
- Power supplies and fans failure monitoring.
- Extreme cooled chassis design.
INDUSTRIAL 18 Port WR-SWITCH DESIGN

- Fan Management Board
- Core Board
- Backplane Board
- Hot swappable Fans
- Hot swappable Power supplies
- Power Distribution Board
INDUSTRIAL 18 Port
WR-SWITCH DESIGN

18 SFP Port

Hot swappable fans

Hot swappable power supplies
Collaboration with KM3Net

Seven Solutions, Emilio Marín, Miguel Mendez (info@sevensols.com)
White Rabbit in KM3NeT

Customization needed to fit WR *(see Peter Jansweijer & Henk Peek talk)*:

- **New WR-PTP packet flow (sw).**
  - Unidirectional links -> Disable the autonegotiation in some ports.
  - Modifications in the routing tables (RTUs) to forwarding **all** packets through the proper ports.

- **Flow Control (gw + sw): Pause Frames.**

**Seven role:** network topology + WR switch firmware/gateware modifications
• Just one downlink is shared by 360 DOMs -> Broadcast or Slow Control Link.
• A unique and dedicated upload link per DOM.
WR in KM3NeT: New WR-PTP Flow

My PLL is locking to Broadcast clk.

I need the deltas (Tx/Rx) of my master.

I update my clock with the timestamps.
WR in KM3NeT: The Demonstrator

KM3NeT demonstrator: proof of concept & development workstation.

The new elements of the network must be calibrated. The KM3NeT consortium is working on this issue right now.

- CH1: WRS Broadcast.
- CH2: SPEC1.
  * GM SW vs SPEC1: Accuracy: 116ps, Precision: 49ps
- CH3: SPEC2.
  * GM SW vs SPEC2: Accuracy: 131ps, Precision: 56ps
The Pause Frame protocol is a flow control mechanism which avoids devices overloading and defined by the IEEE 802.3x standard. It has been adapted and developed for KM3Net.
1- DOM 1 is sending too much traffic.
2- The pause frame is triggered by the Rx port of the WRS1.
3- The pause frame arrives at all the DOMs but just DOM1 will accept the request. The PF uses unicast address.
1- The BC Switch is sending too much traffic through the SC link.
2- A DOM reception buffer exceeds the threshold. A pause frame is transmitted to the on-shore station.
3- The PF arrives at the BC switch which halts the whole BC link for a limited period.
WR in KM3NeT: Pause Frame

Since the Tx Pause Frame is triggered by a specific DOM and sent to all of them; Unicast addresses are used.

There is a control of faulty WR devices: The WRS counts how many times a DOM asks for a Pause. The link doesn’t pause if there are too many requests.

It’s little improvement from the standard: Must be shared with the WR community (official sources)?
New White-Rabbit nodes at Seven...

Towards industrial products

Seven Solutions (info@sevensols.com)
CPIC (Compact PCI serial carrier)

• 6U board, 2 FMC HPC, compatible with Compact PICMG CPCI-S.0 rack. Powered by Virtex-6 FPGA

• **Industrial components.** PCIe: 4-lane interface.

• Windows 8 and Linux OS drivers.
SEVEN MEETS SERIES 7

XILINX

ARTIX®
KINTEX®
VIRTEX®
ZYNQ®
WR-LEN

(White Rabbit Low-Cost Embedded Node)

The WR-LEN (White Rabbit Low-Cost Embedded Node) is a stand-alone board based on Artix devices. Designed for cascade configurations based on two SFP ports.

The WR-LEN board provides synchronization signals (available on an internal connector):

- 1 PPS input/output signal, synchronized to the White Rabbit network.
- 10 MHz and 125 MHz output signal, synchronized to the White Rabbit network.
- 10 MHz input signal, where the WR-LEN configured as GrandMaster could be connected to an external master clock reference.
- TOD (Time of Day) port
Daisy-chain studies
Signals, skew measures and histograms
WR-ZEN (Zynq Embedded Node)

Main characteristic: embedded dual-core ARM9 processor
- A fully programmable solution, software and gateware

Linux OS (3.14 kernel as in the switch)

Possible configurations (requires AXI driver!)
- Embedded node (like SPEC). Possible to reuse FMC cards drivers
- Low cost Switch (up to 4 ports).
WR-ZEN (Zynq Embedded Node)

- Based on Zynq (XC7Z015-1CLG485C) with:
  - Dual ARM® Cortex™-A9 MPCore™ with CoreSight™
  - 74K logic cells, 380 KB of memory (95 Block RAMs).
- **New clocking** scheme (cascada PLLs to reduce jitter)
- Memories: **512 MB DDR3, 256Mb Quad-SPI Flash, 4GB SD Card**
- **2x SFP** Optical Ethernets (2x GTP transceivers for SFP links)
- **2x ETH 10/100/1000** copper Ethernet
- **1x FMC (LPC)** using HPC-FMC footprint (extra GTP channels)
- Internal connector **Samtec** de PN QSS-025-01-L-D with **30 FPGA logic programmable pins**
- **2x mini-USB B** (USB-UART bridge for FPGA and CPU), 5x push-buttons (3 for resets and 2 for user), 2x user LEDs
WR-ZEN: Future Applications

- Network redundancy at MAC level:
  - HSR redundancy in IEC68510 standard for Smart Grid
- Timing holdover:
  - In case of failure of the whole network the synchronization must be kept (LTE: 3usecs/day)
  - Internal 10MHz input for backup oscillator (Microsemi CSAC: ~1usec/day)
- Timing provider with an extended I/O board:
  - NMEA, IRIGB, SNMP, ToD, etc
Other developments ...

Seven Solutions (info@sevensols.com)
FMC ADC/DAC (12ch ADC, 2ch DAC)

- FMC-ADC/DAC board designed for system requiring a feedback loop mechanism with precise timing
  - 12 ADC channels, 2 DAC output for FMC-HPC connector (8 ADC channels on LPC)
  - QSE connector compatible with Samtec EQRF
  - ADC from Linear Technology: LTC2175-14 (4-channels, 14-bits & 125 Msps)
  - DAC from Texas Instruments: DAC3482 (2-channels, 16-bits & 1,25 Gsps)
The XMC-HiPSI is a board in XMC format that can hold several serial interface standards (RS422/RS485/RS232). Main features

- **XMC Interface.** XMC-HiPSI supports a x1 PCIe channel through the primary XMC P15 connector.

- **Xilinx FPGAs:** XC6SLX75T-3FGG484I (-40°C ~ 100°C).

- **On board memory:**
  - 1x 2Gbit (256 MByte) DDR3.
  - 1x SPI 32Mbit flash PROM for multiboot FPGA power-up configuration and storage of the FPGA firmware or critical data.

- **Independent Multi-Protocol Serial Channels** (through connector J16 on the PEX431 carrier):
  - **Multi-protocol transceivers support** (RS422/RS485/RS232)
    - Software Selectable Protocols.
    - Synchronous and Asynchronous operation modes.
    - Up to 20Mbps Differential Transmission Rates.
    - Programmable DCE/DTE and Termination Resistors.
    - 1 5kV ESD Tolerance for Analog I/Os.
    - Parity and CRC detection capability.

- **Cooling options:**
  - Designed with a thermal frame to be used with a conduction cooling.

- **Software:** available drivers and configuration tools for Windows.
The Experimental Physics and Industrial Control System (EPICS) is a software framework used to develop and implement distributed control systems to operate devices such as particle accelerators, telescopes and other large experiments.

- Auto sync from PV to WB registers
- Auto conversion: fixed point, signess, range
- Class to access to I2C, SPI, etc. bus and peripherals
- Generic class to access to WB memory:
  - Genum, X1052, Etherbone*, ...

\* Etherbone is a trademark of National Instruments.
Use wishbone-gen to create “extended” C-headers and EPICS Database records connect to Process Variables (PV)

EPICS db records automatically generated are:

- Asyn Input Analog (ai)
- Asyn Output Analog (ao)
- Asyn Input Binary (bi)
- Asyn Output Binary (bo)
SampleAppDriver::SampleAppDriver(const char* portName, uint32_t idxPCIe):
  asynWBPortDrvr(portName, MAX_NUM_SCOPE_PARAMS)
{
  // Creation of memory connector
  pMemCon = (WBMemCon*)new WBMemX1052Con(idxPCIe);
}

SampleAppDriver::setup()
{
  WBNode* pPrhVer;
  WBReg *lastreg;

  //Declare the root of WB periph
  this->pRoot= new WBNode("SdbFS",WB2_ROOT_PERIPH_OFFSET);

  //Create the peripheral for Version core
  pPrhVer=new WBNode(this->pRoot,"Version",WB2_VER_PERIPH_OFFSET);

  //Adding the registers and the fields
  lastreg = new WBReg(pPrhVer, WB2_REG_ARGS(VER,BOARD));
  createParam(new WBFIELD(lastreg, WB2_FIELD_ARGS(VER, BOARD, ID)));

  lastreg = new WBReg(pPrhVer, WB2_REG_ARGS(VER, GW_VER));
  createParam(new WBFIELD(lastreg, WB2_FIELD_ARGS(VER, GW_VER, BUILD)));

  createParam(new WBFIELD(lastreg, WB2_FIELD_ARGS(VER, GW_VER, MINOR)));
  createParam(new WBFIELD(lastreg, WB2_FIELD_ARGS(VER, GW_VER, MAJOR)));
}
EPICS-WB: Future works

- Reorganize as a standard EPICS library
- Sample files: WR-Starting Kit for EPICS
- Add SDB mechanism

More information:
www.ohwr.org/projects/epics-wb
WHITE-RABBIT FOR RF DISTRIBUTION

LOW LEVEL RF CONTROL
The Low Level Radio Frequency (LLRF) electronics will operate for the IFMIF-EVEDA linear accelerator prototype (LIPAc), and for the future IFMIF accelerator project, which is currently in its final phase.

A total nominal power of 2.65 MW will be injected in the Radiofrequency Quadrupole (RFQ), the Medium Energy Beam Transport (MEBT), and the Superconducting RF Linac (SRF Linac) cavities by means of 18 RF power chains, distributed as follows:

- 8 RFQ of 200kW
- 2 MEBT of 105kW
- 8 SRF of 105kW
The IFMIF-EVEDA RF Power System (RFPS) is composed of 18 three-stage amplifiers working at 175 MHz.
7S LLRF proposal specifications

**7S LLRF system specifications:**

- Linux **EPICs** support
- 19” compact PCI Serial crate.
- Fast control based on FPGA Virtex-6.
- GB Ethernet (SFP): **White Rabbit compatible node**.
- Digital I/O signal: Interlocks, Timing trigger system,...
- 16 Analog-Digital converters, 2 Digital-Analog converters
- PassBand filter center in **175MHz**.
- Pin Switch Diode to switch off the RF signal in less than a 1usec.
- SMA connector with 50Ω impedance.
- **RF signal distribution based on WR under study**
Proposed system

Main Features
- Intel® Core™ i7, 2.53 GHz
- Dual-core 64-bit processor
- PCIExpress® CompactPCI® Serial
- Up to 4 GB DDR3 DRAM soldered, ECC
- mSATA and microSD™ card slots
- Standard I/O: 2 DisplayPorts, 2 Gb Ethernet, 2 USB
- Standard rear I/O: 7 PCIe®, 8 USB, 6 SATA, DisplayPort/SIMD
- Rear I/O via mezzanine board: up to 8 Gigabit Ethernet
- Intel® Turbo Boost 2.53, 3.2 GHz, Hyper-Threading, Active Management Technology
- Open CL 1.1 support
Final remarks

Seven Solutions (info@sevensols.com)
7S is doing an important effort to promote WR for many applications and markets.

Many relevant things are very close to come --> keep posted!

Your opinion is important, any feedback is welcome!

More on http://www.sevensols.com
Thank you for your attention