Distributed DDS in a White Rabbit Network: An IEEE 1588 Application

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***Abstract*—Direct Digital frequency Synthesizers (DDS) require a reference local oscillator (LO) to synthesize waveforms with various frequencies. The output clock inherits to a certain degree the frequency stability of the LO. However, very stable clocks, as those generated from atomic standards, employ a prohibitive price to have as LO. In this paper, a system architecture that distributes a frequency reference to multiple slave receivers using the White Rabbit Network is presented. The system architecture aims to be a competitive solution to distribute frequency references over large distances. In addition, the non-ideality of the different system elements as well as the receiver frequency impairments are studied with the view to assess their influence on the quality of the distributed clock.**

I. Introduction

Distribution of modulated signals over large distances has been a subject of research over the past years. Systems such as Radio-over-Fiber (RoF) [1] employ electrico-optical modulators to transform a modulated passband signal from the electrical to the optical domain to be be transported by an optical fiber. These systems have several advantages such as transmitting high data rates with little computational resources. However, they require dedicated and custom designed hardware, optical modulators and links to perform their functionality.

Other typical systems use Analog-to-Digital converters (ADC) and Digital-to-Analog converters (DAC) to translate from the analog to the digital domain. This technique, known as Digitized RF-over-Fiber (DRoF) [2], instead of performing the traditional direct RF sampling, it employs the bandpass sampling technique to down-convert the bandpass signal to the frequency range of the ADC sampling proces by aliasing. Current ADC technologies allow bandpass sampling of signals at frequencies well beyond their own Nyquist rate. The digitized RF signal is afterwards coded and transmitted to the optical fiber using commercial optical transceivers. It has been suggested that such solution leads to a cost-effective performance to transport radio frequency (RF) signals over optical fiber links [2]. However, it still relies on dedicated links to distribute the data modulated RF signal to the base stations.

In this paper, a system architecture that enables the distribution of a clock reference with a relatively low bandwidth in a cost-effective and flexible implementation is described. The distribution of the signal source is done using Ethernet, the most widely used wired technology for data delivery in local area networks.

The Ethernet transmits the reference input signal together with control/ timing data and non-critical data. The system architecture aims to achieve similar performance in distributing clock references as dedicated radio transmission technologies.

The presented system architecture relies on a tight frequency and phase synchronization between the Ethernet nodes. Typically, the system clock of Ethernet nodes is asynchronous, however, several synchronization standards are available that aim to keep the timing of the Ethernet nodes synchronized to a certain level of accuracy. The White Rabbit (WR) specification, developed at CERN, extends the timing accuracy of Ethernet nodes to the sub-nanosecond accuracy realm.

This paper is organized as follows. The White Rabbit network, a non dedicated timing network that uses Ethernet as physical layer to distribute timing with sub-nanosecond accuracy, is introduced in Section II. In Section III, the distributed DDS system architecture is presented. In addition, the different digital processing blocks in both the transmitter and the receiver nodes are described. Section IV, analysis of the different system parameters that degrade the clock quality of the output signal in the receiver node is given. Section V provides a discussion of the main results and ongoing work.

II. White Rabbit Network

White Rabbit (WR) [3] is a project started and managed by Hardware and Timing section of CERN, Geneva, Switzerland, in cooperation with GSI, a physics laboratory located in Darmstadt, Germany and several industrial partners.

The WR project aims to improve, in terms of operational cost and timing accuracy, the current and still operational CERN's timing network system that distributes time information to the diversified particle accelerators equipment.

With this goal an Ethernet network was designed, with the capability of distributing timing with sub-nanosecond accuracy over an optical Gigabit Ethernet network. The designed Ethernet based network is named White Rabbit network.

The WR network achieves sub-nanosecond timing accuracy by implementing both Synchronous Ethernet (Sync-E) and IEEE 1588 standards [4]. Sync-E is an ITU-T recommendation that specifies the oscillators frequency requirements and the network frequency distribution architecture between the master clock reference to the slave base stations over the Ethernet.

On the other hand, IEEE 1588 is a packet-based-protocol that performs the time synchronization and round-trip link delay measurements between the WR nodes.

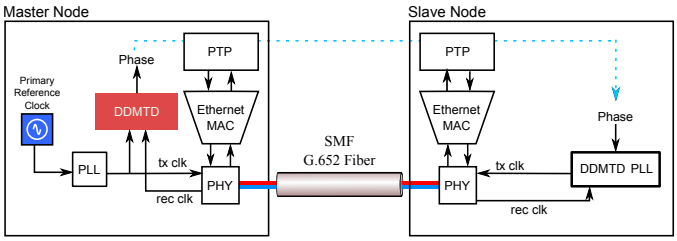

Fig. 1. WR Network System Architecture

In addition, the WR network does frequency loopback to compensate for phase misalignment between the master and the slave nodes, as shown in Fig. 1. The phase difference between the reference clock, at the master node, and the clock recovered from the slave node is measured using the Digital Dual Mixer Time Difference (DDMTD) [5]. The DDMTD circuit is able to measure phase difference between two clocks signals with picosecond resolution. The phase measurement is then transmitted to the slave node to align its clock phase with the reference clock. Thus, achieving the specified sub-nanosecond timing accuracy. The timing performance of the WR network was been extensively described in [6] and [7].

III. Distributed DDS Architecture

The proposed distributed DDS system architecture is illustrated in Fig. 2, for the master node.

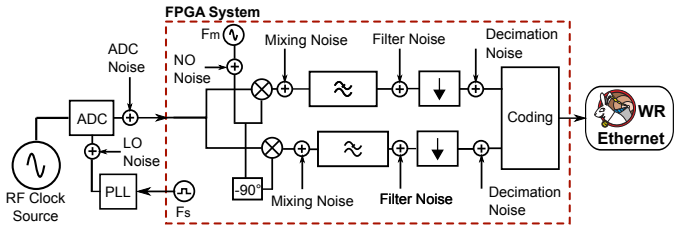

Fig. 2. Master System Architecture

The reference signal is converted to the digital domain by an ADC that performs bandpass sampling and down-converts the input signal to the Nyquist zone of the sampling process. The Nyquist sampling theorem states that the sampling rate must be at least twice the highest component of the low-pass analog signal. To digitize signals with high frequency components, the required sampling rate might be impractical. In the case of bandpass sampling the required sampling rate must be at least twice the maximum signal bandwidth, thus resulting in a reduction of the sampling rate and associated processing requirements.

The bandpass sampling technique has the advantage of down-converting the bandpass signal to a low intermediate frequency (IF) without the need for analog mixers, thus increasing the frequency signal range that the proposed architecture is able to operate.

An added complexity of the bandpass technique is that the input analog signal requires a bandpass filter before the sampling process to minimize the presence of unwanted frequency harmonics that would be aliased to the sampling process frequency range and corrupt the desired analog signal [8].

Prior to the transmission of the digitized signal to the WR receiver nodes, the digital signal is processed using digital signal processing techniques so that only the baseband components are assembled in the Ethernet packet. This aims to reduce the network bandwidth required to transport the reference signal.

The process of translating the digitized IF signal to its baseband frequency is implemented by multiplying the input signal with a synthesized clock signal that has the same center frequency of the input signal. This process generates the in-phase and quadrature (IQ) components of the input signal. The mixing clock is generated in the FPGA by the CORDIC algorithm [9], which is outlined later in this paper.

The mixing process generates high frequency components, which are removed using a low-pass filter. The cut-off frequency of the low-pass filter is selected so that only the bandwidth of the input signal is kept.

The sampling rate can now be further reduced to twice the highest frequency components of the bandpass signal, as stated by the Nyquist sampling theorem. The reduction of the frequency rate is processed by decimation the IQ signal, i.e. by keeping the required number of samples so that the new sampling rate is respected.

The decimated data is then coded in an Ethernet payload frame and broadcasted to the WR slave nodes. A proposed frame format is illustrated in Fig. 3 of how the IQ data might be organized in the Ethernet packet payload. The Ethernet packet contains additional information such as preamble, MAC destination and source address, the Ether-type and the 32-bit CRC which aren't shown for simplicity.

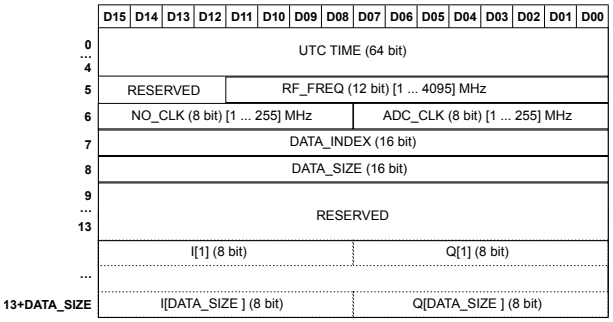

Fig. 3. Ethernet frame

The proposed Ethernet frame contains the UTC timestamp of the first RF sample in the frame being transmitted. In addition, the frame contains a 12-bit field, RF_FREQ, to store the analog RF center frequency in the range between 0 MHz and 4095 MHz. An 8-bit field, NO_CLK, is used to store the CORDIC center frequency ranging from 1 MHz to 255

MHz. The ADC sampling frequency is defined in an 8-bit field, ADC_CLK, that ranges from 1 MHz to 255 MHz. The DATA_INDEX field is a two's complement word that represents the number of total samples already transmitted minus the samples currently being transmitted. The receiver node uses this field to calculate the total number of samples already transmitted. The DATA_SIZE field stores the size of IQ data in the frame. The IQ data is stored between the 14th word and 13+DATA_SIZE. Each word stores first the I data and then the Q data. A frame space of 10 byte is left reserved for future upgrades.

At the receiver node, the received Ethernet frames are decoded and the IQ signal data passes through a modulation process so that the analog signal can be reconstructed. The modulation process is done by executing the same digital processes, performed at the transmitter node, but in reverse order.

Fig. 4 shows the distributed DDS system architecture for the receiver node.

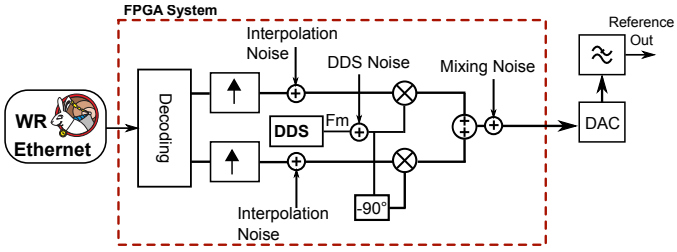

Fig. 4. System Architecture of the Slave Node

To restore the initial sampling rate, the data goes through a digital interpolator. The interpolator has the functionality of adding samples between the decimated samples in the data stream to restore the data stream initial sampling rate.

The digital signal is up-converted to the IF band by multiplying the IQ components with a clock signal with the mixing frequency used in the demodulation process employed at the transmitter. The resulting signals from the mixing process are summed together resulting in the similar reference signal obtained after the ADC sampling process.

A DDS system is designed in the receiver node to synthesized the IF signal back to its original frequency. Implementing the up-conversion process using an DDS system has several advantages such as the ability to generate different frequency sources with high frequency resolution and with virtually no settling time, thus enabling high frequency agility; a requirement highly appreciated in High Energy Physics (HEP) applications, telecommunications or even radar applications. Unfortunately, the frequency spectral quality of the synthesized waveform is corrupted with spurs at different frequencies [10]. In applications where broad-spectral quality is the primary requirement a PLL based synthesizer is preferable to be used.

A. Clock Jitter

The analog to digital process comes with the expense of reducing the signal-to-noise ratio (SNR) of the output signal. Several variables add noise to the signal such as the sampling clock jitter [11] and the ADC finite resolution. In addition, the ADC and DAC employed in the conversion processes add non-linear distortion to the signal due to their non-linearities errors.

Clock jitter is typically described as random variable that changes the transition time from its ideal time position. This intrinsic behavior seen in every clock signal generates an amplitude error in the digitized waveform to be equal to [12]:

$$v_{\text{error}}(t) = \Delta t \frac{dv_{\text{RF}}(t)}{dt} \tag{1}$$

where $v_{\text{error}}(t)$ represents the amplitude sampling error, Δt the ADC's sampling clock jitter and $v_{RF(t)}$ the analog input signal.

The SNR decreases due to the sampling clock jitter variance, σ_i^2. For a sinusoidal clock with frequency f_{RF} the SNR due to jitter is given by:

$$\text{SNR}_{\text{jitter}} = -10\log_{10}\left(\sigma_i^2\,(2\pi f_{\text{RF}})^2\right)[dB] \tag{2}$$

From Eq. 2 it is shown that the clock jitter has a reduce effect in sampling low frequency signals. However, it starts to have a strong effect in the degradation of the SNR for high frequency signals.

However, the total SNR degradation is not just due to the sampling clock jitter. Another term that adds noise to the signal is due to the specific ADC system. The ADC SNR describes the electrical noise of the ADC combined with its static errors. The total ADC SNR is defined as [12]:

$$\text{SNR}_{\text{Total}} = -10\log_{10}\left(10^{-\text{SNR}_{\text{adc}}/10} + 10^{-\text{SNR}_{\text{jitter}}/10}\right) \tag{3}$$

B. Bandpass Sampling

In the described system the ADC employs the bandpass sampling technique instead of direct down-conversion the signal to a IF range.

The bandpass sampling digitizes a bandpass signal by folding the bandpass signal to the frequency range lying between the DC value the Nyquist frequency[1].

To ensure that the spectrum does not overlap and corrupts the desired signal, the bandpass sampling requires that the ADC sampling rate is at least twice the bandwidth of the bandpass signal and twice the highest frequency in the bandpass signal. That is, the sampling rate, F_s, must obey [8]:

$$\frac{2f_U}{k} \leq Fs \leq \frac{2f_L}{(k-1)} \tag{4}$$

where k is an integer given by

$$2 \leq k \leq \left\lfloor \frac{f_U}{(f_U - f_L)} \right\rfloor \tag{5}$$

[1]The Nyquist frequency is half the sampling rate of a discrete signal processing system [13]

The bandpass signal is defined between lower signal frequency component, f_L, and its upper frequency component, f_U. The operation $\lfloor x \rfloor$ represents the largest integer not greater than x.

In addition, bandpass sampling requires that the ADC is able to operate effectively at the highest frequency component of bandpass signal. Typically, high attenuation requirements are specified for the analog bandpass filters to prevent distortion of the bandpass signal due to the presence of nearby frequency components. However, in this application the bandpass filters can be disregarded to a certain extend because the reference signal is obtained from a very pure and well defined (frequency wise) clock signal.

C. ADC/DAC Characterization

The characterization of an ADC or DAC component should be realized by analyzing its static errors in addition to the dynamical errors described above. The static errors are fully described by four terms: The offset error; the gain error; the differential nonlinearity (DNL) and the integral nonlinearity (INL). These errors affect the overall converter transfer characteristic. Both the offset and gain errors can be easily compensated by a calibration process. The DNL is defined as the difference between the ideal quantization width (for an ADC) or quantization height (for a DAC) from one least significant bit (LSB). This error is illustrated in Fig. 5 for an ADC and in Fig. 6 for a DAC.

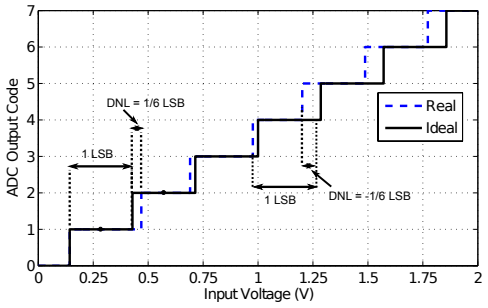

Fig. 5. ADC Differential Nonlinearity Errors

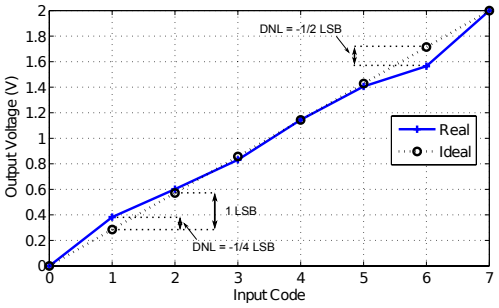

Fig. 6. DAC Differential Nonlinearity Errors

The INL is characterized by the sum of the DNL errors from zero to the highest value and reflects the error variation from the ADC ideal transfer characteristic. The accuracy of the ADC or DAC is maximum difference between the analog value and sum among the quantization errors described.

D. CORDIC Algorithm

A synthesized clock signal is required to down convert the signal from IF to its baseband. An effective way of generating the clock reference in an integrated circuit is by using the Coordinated Rotation Digital Computer (CORDIC) algorithm.

CORDIC algorithm is a recursive computationally efficient arithmetic algorithm, introduced by Volder [14] in the fifties. In its vector rotation mode [15], the $\cos(\theta)$ and $\sin(\theta)$ are calculated as :

$$\begin{aligned} x_{(i+1)} &= x_i + \delta_i 2^{-i} y_i \\ y_{(i+1)} &= \delta_i 2^{-i} x_i + y_i \\ z_{(i+1)} &= \theta_i - \delta_i \tan^{-1}(2^{-i}) \\ \delta_i &= \text{sign}(z_{(i+1)}) \end{aligned} \tag{6}$$

where i is the recursive estimation number, x_n = $\cos(\theta)$, y_n = $\sin(\theta)$, $z_n \approx \theta$ for n recursive operations. The values for $\tan^{-1}(2^{-i})$ are typically stored in read-only lookup table. The CORDIC algorithm accuracy increases with the number of iterations implemented. As shown by Eq. 6, this algorithm relies on basic shift register and add operations which have a very efficient implementation in integrated circuits based designs.

E. Direct Digital Frequency Synthesizer

The DDS is a digital system that generates a waveform by reading from a look-up table storing the amplitude values of a sine wave for a specific phase range. Waveforms of different frequencies may be obtained by choosing the rate of phase increments. A DDS block diagram is shown in Fig. 7. With this simple system, first introduced by Tierney [16], the frequency and phase resolution of the synthesizer can be altered by changing the input control word (FCW).

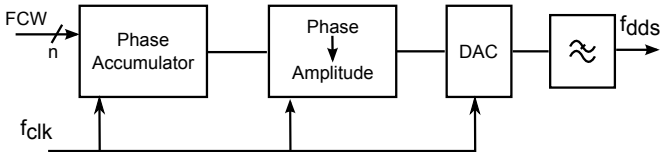

Fig. 7. DDS Block Diagram

The DDS output frequency is given by:

$$f_{\text{dds}} = FCW \cdot \frac{f_{\text{clk}}}{2^n} \tag{7}$$

where f_{clk} is the frequency reference and n is the number of bits used in the representation of the phase accumulator. The phase accumulator output value is then truncated and mapped to an amplitude value with the assistance of the look-up table that maps the phase to the corresponding amplitude. The truncation process is done due to the finite number of

samples in the lookup table. It is known that phase truncation generates spurious frequency at the output of the DDS [10]. The digital output is then converted to the analog domain with a DAC which is followed by a low-pass filter that removes the high frequency components generated by the D/A process.

IV. Numerical Simulations

Numerical simulations were performed using MATLAB to study the performance of the system architecture described in Section III in terms of the SNR and the RMS jitter measured in the output waveform for different system parameters.

The system parameters used for the simulations presented in this section are the following. The number of sampling points is chosen to be 5×10^6 so that the obtained measurements have a good level of confidence. The RF input signal is centered at 40 MHz, selected to be close to the LHC Bunch frequency. The input signal has a defined a bandwidth of 2 MHz, selected for system generalization. The maximum sampling clock frequency of the ADC is 100 MHz. The sampling clock jitter is set constant to 4 ps rms @ 125 MHz, which is higher than the one estimated from a WR slave clock [3]. The maximum resolution for the ADC is 14 bits with $\pm$ 1 INL and $\pm$ 0.3 DNL. The DAC has a maximum resolution is 16 bits with $\pm$ 4 INL and $\pm$ 2 DNL. The low-pass filters are 10^{th} order Butterworth filters with cut-off frequency set to 2 MHz. The digital signal processing calculations are implemented using fixed-point calculations to mirror a real integrated circuit implementation.

We start by showing in Fig. 8 the variation of SNR due to different sampling frequencies. The different sampling rates down-convert the input signal to the ADC nyquist zone by aliasing. The SNR is estimated by measuring the error between the bandpass waveform in the master node and the output waveform obtained in the slave node. Fig. 8 shows that an increase in the ADC's sampling rate reduces the SNR. This is mainly due to the different signal processing blocks. For instance, the low-pass filter has a steep rool-off when operating at lower frequency rates, thus reducing a higher amount of noise.

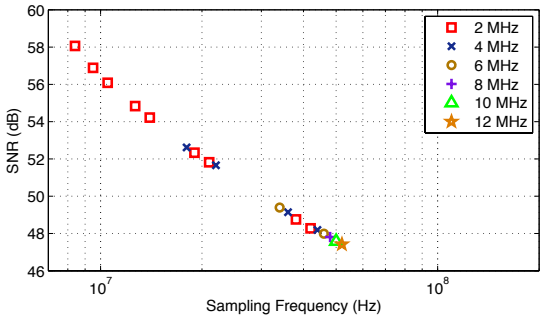

Fig. 8. SNR vs ADC Sampling rates that down-convert for the input signal to several IF

In Fig 9, the variation of SNR due to the number of bits used in the A/D conversion is depicted. It shows that reducing the number of bits used in the process degrades the SNR, a foreseen result.

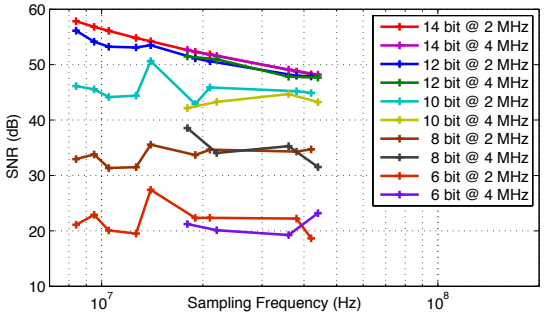

Fig. 9. SNR vs Number bits of the ADC for different IF signals (IF = [2, 4] MHz)

Next, we relate how the precision in generating the cosine and sine signals, using the CORDIC algorithm, reduces the SNR of the output signal. Clearly, from Fig. 10 we can conclude that synthesizing a signal with a 16-bit output precision yields in good SNR.

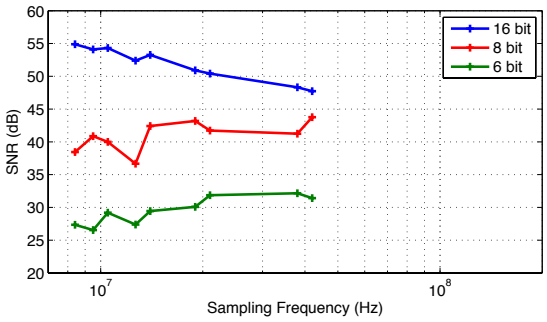

Fig. 10. SNR vs CORDIC Resolution for the (IF = 2 MHz)

Although the SNR is a valuable metric in determining the quality of the distribution system for synchronization applications, the rms jitter and respective phase-noise spectrum, measured at the output waveform are typically required parameters.

Next, we show how phase-noise in the receiver's oscillator increases the rms jitter in the synthesized waveform. In Fig. 11, the phase-noise spectra of the output waveform for different range of phase noise in the frequecy reference of the receiver is shown. In addition, Fig. 11 shows the estimated rms jitter by integrating the phase-noise over the range of offset frequencies simulated, which is between 10 kHz to 2 MHz. The phase-noise spectra presented in Fig. 11 provide the maximum phase-noise permited in receiver's frequence reference. The phase-noise in the receiver's oscillator is modeled as a normally distributed random variable with standard deviation varying between $\pm$ 1 parts-per-bilion (ppb) and $\pm$ 50 parts-per-million (ppm). For a receiver's frequency reference with a rms jitter above $\pm$ 1 ppb the phase-noise spectrum of the output

waveform becomes greater reflecting the increase of phase-noise due to the receiver.

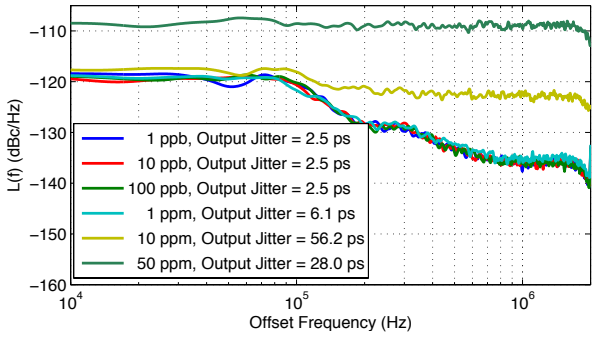

Fig. 11. Phase Noise spectra of the output waveform for different rms jitter in the slave's frequency reference

Nonetheless, as mentioned in Section II, the WR network implements Sync-E to provide a frequency reference between the timing nodes. This means that the slave's system clock is not asynchronous, as in standard Ethernet, but locked and traceable to the master frequency reference resulting in a $\pm$ 100 ppt frequency stabilization between the Sync-E nodes [17] [18].

Fig. 12 shows the output waveform phase-noise spectra for the different sampling rates that down-converts the input signal to an IF centered at 2 MHz. The output phase-noise shows spurs located at different frequency offsets, which are generated by the quantization process. The presence of spurs within the bandwidth of the original signal increases the rms jitter.

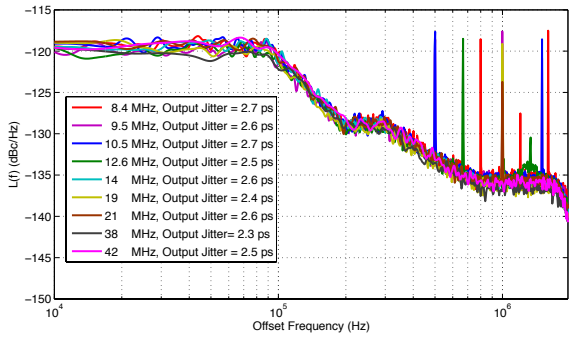

Fig. 12. Phase-Noise Spectrum for different sampling rates (IF = 2 MHz)

In the phase-noise spectra obtained for the sampling rate set to 38 MHz and 42 MHz the frequency spurs are located away from the bandwidth of the input signal. For this reason these two references should be used to sample and distribute the particular frequency reference analyed.

V. Conclusion

This paper described a system architecture, that uses the White Rabbit network to transport specific reference clock signals over large distances. The distributed clock signals are employed as local oscillators for the DDS based frequency synthesizers. The results presented, obtained by simulations, showed that considered different system parameters degrade performance in terms of the SNR and RMS jitter in the reconstructed waveform. We concluded that the Distributed DDS system achieves good performance under propoper selection of system parameters. This work will continue with the implementation of the proposed system in an FPGA design.

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