How to Intergrade

White Rabbit

Into your system

清华大学 工程物理系 龚光华
2018/6/29
Outline

- Making the shopping list.
- Shopping for WR COTS
- Following the manual
- Checking an example
- summary
MAKING SHOPPING LIST
System Spec. list

- Accuracy and precision
- Distance and #n of node
- external T&F reference
- Data transmission over WR
- Reliability and Redundancy
- ....
WR COTS CATALOG (SELECTED).
WRS (standard)

• Central element of WR network
• 18 port gigabit Ethernet switch with WR features
• One management port (separated from WR network)
• Fully open design, commercially available

Image courtesy of Seven Solutions
WRS (fan-less)

- Improved heat dissipation, without FAN
- Improved device temp. range to -20 ~ 70
- Improved low jitter clock circuit
- Improved kernel board placement

- Optical Management port for fiber connection
- 18 WR ports with light guide
- Software/Firmware compatible with standard WRS-18

WRS (compact)

https://redmine.nikhef.nl/et/projects/chromium/wiki/Backplane-20SFP
WR Node: carrier boards

- PCI-Express/VME/PXI/uTCA form carrier boards:
  - Logic/Memory/Process
  - WR circuit/SPF-Port/WRPC
  - FMC mezzanine connectors

- AD/DA/IO with FMC mezzanine cards
Simple PCIe FMC carrier

- 4-lane PCIe (Gennum GN4124)
- 1x Xilinx Spartan6 FPGA (XC6SLX45T-3FGG484C)
- FMC slot with low pin count (LPC) connector
  - FMC connectivity: all 34 differential pairs connected
  - 1 GTP transceiver with clock, 2 clock pairs, JTAG, I2C
  - No dedicated clock signals from Carrier to FMC
Simple PXI express FMC Carrier Board
SVEC

Simple VME FMC Carrier
AFC/AFCK

AMC FMC Carrier
WR Node: mezzanine cards

- FMC form WR mezzanine
  - WR circuit/SFP-Port/WRPC
  - FMC mezzanine connector
WR node – Cute-WR

基于FMC子卡的通用精简WR节点    CUTE-WR

- 以FMC子卡形式与前端电子学集成
- 提供1Gbps光纤以太网接口
- USB配置与调试接口
- LEMO/SMA通用外部接口
Cute-WR block diagram
WR node  Cute-WR-DP

WR双端口节点  CUTEWR-DP
Cute-WR-DP block diagram
1) 并行模式：双端口互为冗余备份，提高系统可靠性
2) 串行模式：两个端口一个上行、一下下行，组成串行/环形网络
WR node - Mini-WR

芯片/模块级的WR节点
Mini-WR block diagram

Signals flyby through FCl connector to gold-finger.
Not all GMII connected to Gold-finger due to limited pos.
WR node - COP-WR

WR node with Co-Process-FPGA
WR node - CRIO-WR
CRIO-WR block diagram
WR node – build your own

Schematic / pcb example

Open source IP core

Manual

Your fancy WR node
Follow the manual
Manuals for WR carrier board

- Follow the FMC standard (ANSI/VITA 57.1-2008) for mezzanine

- Follow the carrier board form standard
  - VME, PCIe, PXI, VXI, MTCA
Cute-WR-DP / COP-WR接口

- 四个LED：一个电源灯和三个通用指示灯

- 两个SMA/LEMO接口：
  1. 专用输入接口，可以外接参考时钟
  2. 通用IO，可以输出PPS信号

- USB：UART协议，115200波特率，8位，无校验。用于本地配置参数和监控同步状态

- FMC接插件：提供32对LVDS通用IO，4对LVDS专用时钟输入
  - 供电：3.3V
  - 定时：PPS、SYNC_CLK
  - 慢控制：SPI，如读取MAC、IP地址等
  - 数据传输：M2C_FIFO Interface，C2M_FIFO Interface
    - 最高支持125M×8bit
Signals on FMC connector

Watch out:
As the LVDS in BANK3 only supports input. The LA31/LA32/LA33 only supports input!
FMC Connector signals

Timing interface

Sync Clock

pps_utc

IDLE PPS_High PPS_Low MSB LSB IDLE

48 Bits UTC

Data Interface

C2M(M2C)_FIFO_clk

C2M(M2C)_FIFO_wrreq

C2M(M2C)_FIFO_active

C2M(M2C)_FIFO_almostfull

C2M(M2C)_FIFO_data<7..0>
Interfacing with user logic

- PPS+TOD
- CLK信号
- PPS
- CLK

Decode logic:
- FSM
- UTC latch
- UTC Counter
- Sub-sec Counter
- Time stamp

User logic:
- USER FPGA

Cute-WR
- PLL/DCM (optional)
1. 完全支持WR协议，单FPGA实现降低系统成本
2. TCP/IP协议栈与WR同步功能集成，数据传输与时钟同步互不干扰；
3. 926Mbps UDP传输带宽，258Mbps TCP传输带宽（过一级交换机）
4. 支持SNMP监控，支持MultiBoot远程更新
5. 支持双端口，可以实现双通道冗余或级联架构，实现灵活的网络拓扑（HSR，PRP）
双端口数据传输/转发功能测试

PC ↔ WR交换机 ↔ CUTEDP1
CUTEDP1用户TCP带宽 258Mbps

PC↔WR交换机↔CUTEDP1↔CUTEDP2
CUTEDP1/2共同用户TCP带宽430Mbps

• 数据传输不影响同步性能
• 数据转发不影响同步性能
• TCP带宽的瓶颈在于TCP/IP协议栈

*测试环境：speedometer
EXAMPLE

This is an example.
Example: PET Insert Ring

Importance of TOF

TOF PET

"Recent advances and future advances in time-of-flight PET" by W. W. Moses et al

27 cm Lesion Phantom

Better quality
Shorter scan
Less dose

Image courtesy of Joel Karp, University of Pennsylvania
Example: PET Insert Ring

Objective: Build a MR-compatible brain PET insert with DOI and TOF capability.
Modulized Digitizer electronics

Detector Module

Digitizer

- ASIC
- LYSO + SiPM
Example: PET Insert Ring

Back-end electronics: a White Rabbit (WR) switch

r.m.s less than 30 ps including clock synchronization and TDC precision.
Clocks of all coincidence units are synchronized based on White Rabbit.

Coincidence logic inside WR switch and data transferred to PC via Gigabit Ethernet.
Q&A

Thank You!