White Rabbit Module for NI CompactRIO

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CompactRIO White Rabbit (CRIO-WR) is a standalone White Rabbit node implementation on a PCB with a form factor for National Instruments CompactRIO modules.
What Is CompactRIO?

- Reconfigurable embedded control and acquisition system made by National Instruments
- Includes a reconfigurable FPGA chassis, an embedded controller and I/O modules
- Programmed with NI LabVIEW
C Series Module Hardware Overview

- The C Series module connects to the CompactRIO chassis through the 15-pin DSUB connector.
- The communication, power, and ground signals in this connection are collectively called the module interface.
- The EEPROM stores identification and calibration information.
• Modules and carriers interact with each other through the C Series interface.
• The C Series interface is implemented through a 15-pin DSUB connector, which includes all required signals in addition to power and ground connections.
• The functions of many of these signals vary depending upon the current operating mode of the module. Different operating modes are defined to enable module identification, module configuration, I/O access, and sleep states.
Basics of Driver Development

- CompactRIO Module Development Kit 2.0
  - Configuration of EEPROM
  - Implementation of the communication over SPI

Main Features

- White Rabbit node in CompactRIO format
- Standalone WR operation (GrandMaster, Master or Slave mode)
- Xilinx Spartan-6 FPGA, SPI FLASH or JTAG configuration
- Programmable I/O (up to 10 x 3.3V / 5 x LVDS), e.g.
  - 10 MHz and PPS inputs (GrandMaster mode)
  - Reference clock and PPS outputs
  - Trigger inputs / pulse outputs
- USB-UART bridge (WRPC user shell)
- Originally derived from and keeps maximum firmware compatibly with SPEC and CUTE-WR
CRIO-WR complies with most CompactRIO specifications. Violations (so far known):

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Specification</th>
<th>CRIO-WR</th>
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<tbody>
<tr>
<td>Current consumption</td>
<td>&lt;= 200 mA</td>
<td>480 mA</td>
</tr>
<tr>
<td>Operating power, 85 °C rated components (100 °C rated components)</td>
<td>&lt;= 0.625 W</td>
<td>2.4 W</td>
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<tr>
<td>Operating temperature range</td>
<td>-40 to 70 °C</td>
<td>TBD</td>
</tr>
<tr>
<td>Total inrush charge during module power-up time (integral of current drawn in excess of 200 mA)</td>
<td>&lt;= 150uC</td>
<td>TBD</td>
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</table>
• Current consumption, operating power / temperature: Hard to achieve specifications with present hardware!
  Operating power of main functional blocks:
  – FPGA: approx. 1 W
  – Clock generators: approx. 700 mW
  – FO Transceiver: approx. 500 mW

• Total inrush charge during module power-up time:
  Specification possibly achievable by reducing the number of on-board bulk capacitors (22 uF) at +1.2V and +3.3V (tests planned)

• Issues:
  First tests at room temperature showed no issues. After 8 hours of constant operation (CRIO-WR master with CRIO-WR slave) the internal module ambient temperature is 45°C.
Considerations for a next hardware version

- Dedicated reference clock output at user I/O connector, i.e. not via FPGA output (jitter) but directly from disciplined reference clock generator
- Reducing operating power (clock generators ...)
- Minor modifications on power supply / filtering / blocking
- ...?
Status:

- HW v1.0, FW WRPC v2.1, FW CRIO v0.1 (demo), LabVIEW VI v0.1 (demo)
- WRPC mode GrandMaster, Master and Slave tested (CRIO-WR / CRIO-WR)
- First tests in cRIO chassis with LabVIEW (SPI EEPROM read / write, SPI FPGA read / write)

More information:

Thank you for your attention!

Questions?

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