White Rabbit Switch V3 board

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Talk overview

Introduction

- White Rabbit switch & Switching core board

Board design

- Schematics
- Layout
- Board development status
- V3 board planning

Conclusions

- Additional design considerations
White Rabbit Switch (WRS)

INTRODUCTION
Introduction

The White Rabbit is intended to be the next-generation deterministic network, based on:
- Synchronous Ethernet
- PTP (IEEE 1588)

Goals:
- ~1000 nodes synchronized up to 10 Km.
- Over copper or fiber.
- Sub-nano second accuracy.

White Rabbit Switch (WRS)

Switch Specifications:


WRS Configurations:

- MCH inside a uTCA rack.
- Standalone switch equipment inside a 19” case (using miniBackplane board).
White Rabbit MCH Switch – uTCA Configuration:

Up to 12 WR AMCs

White Rabbit Switch MCH
- Uplinks ports G.652 fiber
- Backplane connector
- IPMI-A
- Fabric A
- Fabric E
- Fabric F
- CLK1
- CLK2
- Redundant PSU

White Rabbit Switch AMC
- Downlink G.652 fiber or twisted pair port
- Front Panel
- I2C Management[1:12]
- 1.25Gbps Ethernet (LVDS)[1:12]
- SMI_LINK (LVDS)[1:12]
- 1.25Gbps Ethernet (LVDS)[1:4]
- 125 MHz reference clock[1:12]
- Configurable clock[1:12]
- Card mgt.
- WR switch slave module FPGA

Other Slave AMC Card
- Front Panel
- Anything you like here

uTCA crate

Cooling Stuff
SCB in uTCA WRS Configuration:

- Tongue 4: SMI channels 7-12
- Tongue 3: SMI channels 1-6
- Tongue 2: Clocks (CLK1 and CLK2)
- Tongue 1: Power, IPMB, management and Downlinks[1:12]

SCB in Standalone Configuration:

- Tongue 3: not used
- Connectors for communicating boards

SCB
SCB Design Baselines:

- Improve V2 board.
  - Minimizing cost in order to get the lowest WRS price (lower than 1000€/unit).
- Using most of the components and architecture, if is possible, used in WRS V2.
- Improving design flexibility in order to facilitate compatibility between uTCA and miniBackplane configurations.
White Rabbit Switch (WRS)

SWITCHING CORE BOARD ELEMENTS
Switching Core Board (SCB)

The main element of the WRS will be the “Switching Core Board”.

Fundamental functionality of White Rabbit Protocol will be implemented inside this board.

Standalone and uTCA WRS configurations, both will use SCB as their main component.

Designed by Seven Solutions.
Main components: FPGA

- **XC6VLX130T-1FF1156C** Xilinx Virtex-6 FPGA:
  - 1156-ball, 1.0mm pitch, BGA package
  - 20000 slices
  - 1740 Kb Distributed RAM
  - 480 DSP48 Slices
  - 9504 Kb Block RAM capacity
  - 15 Banks and 600 user I/O
  - 10 Mixed-Mode Clock Managers (MMCMs)
  - 20 GTX Transceivers
Main components: Microcontroller ➔ *legacy* ➔ *contingency plans*?

- **AT91SAM9263** Atmel ARM9 CPU
  - 220 MIPS at 200 MHz
  - 16 KB Data and Instruction Caches, Write Buffer
  - MMU (Linux capable)
  - 128 KB Internal ROM and 96 KB Internal RAM
  - Dual External Bus Interface
    - EBI0: SDRAM and NAND Flash
    - EBI1: FPGA Comms.
  - Ethernet MAC 10/100
  - 324-ball, 0.8 mm pitch, TFBGA Package
WRS core board components

Additional components:

- 16MB x 32 SDRAM
- 256 MB Nand Flash
- Ethernet 10/100 PHY
- 8 MB SPI Boot Flash
- Two 512Kx36 QDRII SRAM
- 8MB x 16 NOR Flash (for BPI FPGA Configuration)
- 14-Output Clock Generator with Integrated 1.6 GHz VCO (AD9516-4)
White Rabbit Switch (WRS)

SCB SCHEMATICS
SCB Power Supply Architecture:

- DC/DC
- LDO
- LDO
- LDO
- LDO

Input: +5VIN

Outputs:
- +1V8
- +2V5
- +1V0
- +1V5
- +3V3
- +3V3_PLL
- +2V5_PLL
- +3V0_PLL
- +3V0_OSC
- +3V0_VM53
- +1V2_cpu
- +1V0_GTX
- +1V2_GTX
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**Power Sequency** (FPGA and CPU requirement):

1. +1V0 (FPGA VCCINT)
2. +2V5 (FPGA VCCAUX)
3. +1V2_cpu (CPU VDDCORE), +1V0_GTX, +1V2_GTX
4. +3V3, +1V8 (CPU I/Os)

**LDOs** to feed **GTX** transceivers recommended by Xilinx GTX User Guide (**UG366**).

- +3V3_PLL and +2V5_PLL to feed **AD9516** PLL
- +3V0_VM53 to Enable/Disable **VM53** Oscillator
- +3V0_OSC to feed **DMTD** Phase Detector circuitry.
Based on V2

Bruce Griffith’s flexible clock input circuit for external 10MHz and 125MHz clocks.

Added Signal Transformer to prevent signal integrity problems from GPS.

Oscillators hard to find. IVT3200C footprint added (just in case).
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RS232_and_USB_ports.SchDoc:

- **RS232_MNG_CTS** and **RS232_MNG_RTS** signals removed.
- Added **FPGA_RS232** interface for FPGA debugging purposes *(not used for WRS).*
- Used **USB Device** CPU Port.
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CPU_Memory.SchDoc:

- EBI0 (+3V3) used.
- **16Mx32 SDRAM@133MHz:**
  - IS42S32160B-75EBLI
  - 90-ball BGA 0.8mm pitch package
- **256MB NAND Flash** Memory (normal boot):
  - MT29F4G08ABADAWP
  - TSOP-48 package
- **8MB NAND SPI Data-Flash** Memory (failsafe boot)
  - AT45DB642D-CNU
  - CASON-8 package
- **OR-Gate** in order to select boot process (**V2 bug**):
  - FBOOT_SEL signal HI: boot from Failsafe SPI Flash
  - FBOOT_SEL signal LOW: normal boot from NAND Flash.
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CPU_100M_Ethernet.SchDoc:

- **LAN8720A-CP** PHY Ethernet used:
  - QFN 50 pins 0.5mm pitch package
  - +1V8 I/Os

- CPU Ethernet pins **powered by VDDIOM1** (EBI1 bus) at +1V8:
  - EBI1 Bus connected to FPGA.
  - Virtex-6 is not +3.3V tolerant.

- **Q3 NMOS** for +1V8 ↔ +3V3 level translator (CRS_DV is a +3V3 signal)
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FPGA_GTX.SchDoc:

- XCV6LX130T provides **20 GTX** transceivers:
  - WRS requirement: **16 downlinks + 2 uplinks**
  - 2 free GTX

- Power Supply Decoupling Capacitors: According to Xilinx UG366 (v2.5), page 286, the suggested filtering for the MGTAVCC and MGTAVTT power supplies is:
  - One 0.22uF, size 0402, ceramic capacitor per power supply pin
  - One 4.7uF, size 0402, ceramic capacitor per two Quads
  - One 330uF bulk capacitor for each power supply
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**FPGA_Configuration.SchDoc: (I)**

- **Two FPGA configuration modes** possibilities:
  - Slave Serial Configuration Mode:
    - **Defect mode**
    - $M[2:0] = 111$
    - Used in White Rabbit
    - CPU configures FPGA
  - Master Byte-wide Peripheral Interface (BPI):
    - **Not used in White Rabbit**
    - $M[2:0] = 011$
    - PC28F256P30BFA 256Mbits NOR Flash, BGA-64 balls, 1.0 mm pitch package
    - LX130T Bitstream length: **43,719,776 bits**
  - Mode selected by S3 switch (not mounted in WRS)
Resistors in FPGA_DIN and FPGA_CCLK for level translating

FPGA Global Clocks (LVDS):
- DMTD_CLK (~125MHz)
- FPGA_MAIN_CLK (25MHz)
- QDRII_CLK (250MHz)
- QDRII_200CLK (200MHz)
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CPU_IO_Ports.SchDoc (1):

- **PE[0..7]**: GPIO to external connectors
- **PCK3**: Programmable Clock Output to FPGA MRCC on Bank-15
- **SSC-0** (Synchronous Serial Controller) to Slave Serial FPGA Configuration:
  - **TK0** -> FPGA_CCLK serial configuration clock
  - **TD0** -> FPGA_DIN configuration data.
- **SSC-1** to external connectors for Cortex-M3 comms.
- Two-Wire Interface (I2C): **TWD** and **TWCK** to ARM external Watch-Dog.
- Serial Peripheral Interface **SPI-1** to control the AD9516 through FPGA (this way allows FPGA to control AD9516 too).
- **ARM_WD_INT**: interruption signal from CPU external Watch-Dog.
- **EXT_DMARQ3**: DMA Request-3 from FPGA.
- **ARM_FPGA_RESET**: SW Reset to FPGA firmware.
- **SPI-0** to SPI Flash Failsafe memory.
- **CPU_LED[1..2]**: CPU Led debugg signals.
CPU_IO_Ports.SchDoc (2):

- **FPGA_DONE**: FPGA DONE_0 signal for monitoring configuration.
- **FPGA_INITB**: FPGA INIT_B_0 signal for monitoring configuration.
- **FPGA_PROGRAM_B**: FPGA PROGRAM_B_0 for configuration.
- **EXT_IRQ0**: to external connectors (Cortex-M3 interruption).
- **EXT_IRQ2**: to FPGA
- **PC[0..15]**: GPIO to external connectors.
- **DBG_RXD** and **DBG_TXD**: Debug Unit to external connectors for debugging.
- **IC24 TXB108PWR**: +3.3V (CPU) to +2.5V (FPGA) level translator (100Mbps maximum data rate) to SPI PLL configuration.
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External WatchDogs.SchDoc:

- **Independent** CPU and FPGA external **DS1374** WatchDogs:
  - Not mounted in White Rabbit
  - **Safety** requirement
  - I2C programmable functionality:
    - 32-Bit Binary Counter
    - Second Binary Counter Provides Time-of-Day Alarm, Watchdog Timer, or NV RAM
    - Power-Fail detect
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**FPGA_POWER_GND.SchDoc:**

- **+2AV5** System Monitor Power Supply: Filtering according to Xilinx *UG370*

- **VCCINT** Decoupling Capacitors according to Xilinx *UG373*:
  - Required **330uF** PCB Capacitors:
    - LX130T = 2
    - LX195T = 4
    - LX240T = 4
    - LX365T = 6
  - **WRS provides six 330uF cap.** to improve FPGA possibilities.

- Added decoupling capacitors above recommended by Xilinx.
According to Xilinx XAPP886: Interfacing QDRII SRAM Devices with Virtex-6 FPGAs:

- QDRII SRAM not supported by Virtex-6 MIG.
- Based on the QDRII+ using four-word burst access mode.

Adaptation of the Design:

- **Generate** the most appropriate combination of QDRII+ interfaces using the MIG tool.
- **Modify** the parameter values to adapt to the specifications of the QDR standard.
- **Set up the simulation environment** using the Cypress memory models.
FPGA_QDRII.SchDoc (2):

- Modify the **state machine** to operate properly for two-word burst.
- Modify the **testbench** to verify correct operation for two-word burst.
- **Implement** two modules to connect the testbench to the user interface at the external memory clock frequency.
- **Place and route** the design and close timing.
- **Create a user interface** front end running at the full interface frequency for legacy, purposes, or for designs that need to feed one read and one write command per cycle.
- **Debug and verify** proper functionality through functional simulation.

Final FPGA pinout determined by PCB routing (pin swapping):
- Allowed between signals **inside a group at the same bank**.
Used EBI1 bus interface at 1.8V.
- Power Supply of EBIs: 1.8V or 3.3V nominal
- FPGA doesn’t support 3.3V

32-bit of Data

23-bit of Address

ARM CLK signal included: pull-down resistor R182 on ARM_CLK signal to adapt level:
- CPU Output Current 8mA max.
- FPGA LVCMOS18 VIH min.: 65% VCCO
CPU_JTAG_Power_PLL.SchDoc:

- AT91SAM9263 power supply pins:
  - **VDDCORE** pins: Power core, embedded memories and the peripherals: \(1.2\text{V}\) nominal
  - **VDDIOM0** and **VDDIOM1** pins: Power the EBI0 and EBI1: \(1.8\text{V or 3.3V nominal}\)
  - **VDDIOP0** pins: Power Peripheral I/O and USB transceivers: \(3.3\text{V nominal}\)
  - **VDDIOP1** pins: Power I/O involving the Image Sensor Interface: \(1.8\text{V, 2.5V, 3V or 3.3V nominal}\)
  - **VDDBU** pin: Powers Slow Clock oscillator and part System Controller: \(1.2\text{V nominal}\)
  - **VDDPLL** pin: Powers the PLL cells: \(3.3\text{V nominal}\)
  - **VDDOSC** pin: Powers the Main Oscillator cells: \(3.3\text{V nominal}\)

- **MIC5232** Ultra-Low Quiescent Current LDO instead of series diodes of V2.
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uTCA_Tongue3.SchDoc:

  - Tongue-3 uTCA PCB connector
- FPGA LVDS_25 standard
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Connectors.SchDoc (1):

- **J1 and J2:** QSS-048-01-L-D-DP from Samtec:
  - 0.635mm pitch
  - 17Gbps High speed socket
  - 48 Differential pairs, 1.1A@30ºC per pin

- **P6:** Header, 20-Pin, Dual row, 2.54mm pitch for the SAM-ICE JTAG ARM7 and ARM9 emulator

- **P5:** Header, 14-Pin, Dual row, 2.0 mm pitch for the Xilinx USB Programming Cable

- **CN2:** KX15-20K4DE from JAE:
  - 0.8 mm pitch
  - SMD PCB-to-PCB
  - 20 pins, 0.5A per pin
  - CLKs for uTCA Board-2
White Rabbit Switch (WRS)

Connectors.SchDoc (2):

- P1, P3, P4, P7 and P8 **SMC** clocks connectors.
- P2: 6-Pin, Dual row, 2.54mm pitch Header:
  - RS232_FPGA
  - CPU_DEBUG
- CON1: USB Receptacle **Type B Right Angle** (not mounted in WRS)
- CN1: **Low-profile uTCA Ethernet Jack** from Tyco Electronics
- J4: **Power** Jack 5A @ 12V (not mounted in WRS)
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FPGA_GPIOs.SchDoc:

- General Purpose I/Os on Bank-13:
  - FPGA_GPIO[0..39]
  - To external J2 connector
Main component: 14-Output Clock Generator **AD9516-4**:

- On-chip VCO tunes from **1.45 GHz to 1.80 GHz**
- External VCO/VCXO to 2.4 GHz optional
- One differential or two single-ended reference inputs

**3 pairs** of **1.6GHz LVPECL** outputs:

- **Each pair** shares **1 to 32 dividers** with coarse phase delay
- Additive output **jitter 225 fs rms**
- Channel-to-channel **skew** paired outputs < **10 ps**

**2 pairs** of **800MHz LVDS** clock outputs:

- **Each pair shares** two cascade **1 to 32 dividers** with coarse phase delay
- Additive output **jitter 275 fs rms**
- Fine **delay adjust (ΔT)** on each LVDS output

- **Eight 250 MHz CMOS** outputs (two per LVDS output)
- **SPI Serial control port**
- 64-lead LFCSP
SCB_PLLs.SchDoc (2):

- **AD9516-4 signals:**
  - **REF1** input: CLK25MHZ_GTX_DAC from VM53
  - **REF2** input: CLK10MHZ_EXT
  - Differential CLK: CLK_125MHZ_EXT
  - LVPECL outputs:
    - OUT0 to OUT4: **125MHz** to FPGA GTX Transceivers
    - OUT5: 125MHz Clock to:
      - EXTREF125MHZOUT (LVCMOS_3V3)
      - uTCA_TONGUE2_CLK1 (LVDS)
  - LVDS outputs:
    - OUT6: Free
    - OUT7: 250MHz QDRII_CLK
    - OUT8: configurable uTCA_TONGUE2_CLK2
    - OUT9: QDRII_200CLK
  - **Independent** +3V3_PLL and +2V5_PLL power supplies from LDO
SCB_PLLs.SchDoc (4):

**CDCM61002**: Two Output, Integrated VCO, Low-Jitter Clock Generator:

- Input Frequency Range: **21.875MHz to 28.47MHz**
- On-Chip VCO Operates in Frequency Range of 1.75 GHz to 2.05 GHz
- 2x Output Available: Pin-Selectable between LVPECL, LVDS or 2-LVCMOS
- Output frequency Range: 43.75 MHz to 683.264MHz
- Low Output *Skew of 20 ps* on LVPECL Outputs

**IC13**:

- Input 25MHz
- Output0 125MHz for the **DMTD Phase Detector** in FPGA (LVDS)
- Output1 125MHz to external J1 connector for debugging.

**IC14**:

- Input 25MHz
- Output: 200MHz for QDRII FPGA core
- **Not mounted**, just in case
SMI[7:12] Links on uTCA fabric D to Board-4

- J3 Connector from Samtec: QSS016-01-L-D-DP
  - 0.635mm pitch
  - 17Gbps High speed socket
  - 16 Differential pairs, 1.1A@30°C per pin

- FPGA LVDS_25 standard
- Two free FPGA clock (MRCC, SRCC) Input/outputs
- A free FPGA Global Clock input/output
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FPGA_System_Monitor.SchDoc:

- **10-bit, 200Ksps** Analog-to-Digital Converter **ADC** inside FPGA
- On-chip power supplies (**VCCINT** and **VCCAUX**) and **internal temperature** monitoring
- **17** external analog inputs
- User-programmable **alarm thresholds** for the on-chip sensors.
- Voltage attenuation filter according to Xilinx **UG370**.
- Auxiliary Analog Inputs Voltage Range: **0 - 1V**
- DMTD and GTX **DAC Outputs** monitored:
  - **Safety requirement** (not used in WRS)
- Four I2C Temperature Sensors **TMP100**:  
  - Resolution: **9 to 12 bits** user selectable  
  - Accuracy: ±2°C (-25°C to +8°C)
FPGA_Peripherals_Control.SchDoc:

- Power Good **PG** Inputs from Power Supply
- **SPI1** from CPU
- **PLL_Control** to AD9516-4
- **+3V0_VM53_EN** to Enable/Disable **VM53** Oscillator Power Supply
- **QDR2_VTT_GOOD** from VTT LDO Power Supply
- **FPGA_RS232** for **FPGA debugging** (attenuation voltage resistors on FPGA_RS232_RXD)
- **DAC_CONTROL**: **DMTD** and **GTX DACs** Control Signals.
Two 512K x 36 QDRII SRAM Chips:
- **CY7C1314CV18-250BZCN** from Cypress
- 250 MHz
- BGA-165 balls, 1.0mm pitch package
- Update possibility to 1Mx32 chip

8 x 47R SMD Array Resistor:
- **No On-Die** internal resistor inside SRAM chip.
- To reduce PCB space
- Final pinout determined by PCB routing (pin swapping)
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QDFII_power.SchDoc:

- Termination $V_{TT} = 0.9\text{V}$ generated by LDO
- **TPS51200** Sink/Source DDR Termination Regulator:
  - 2.5V and 3.3V input voltage
  - VLDIN voltage range: **1.1V to 3.5V**
  - PGOOD to **monitoring** regulator output
  - ±10mA RFOUT Buffered Output
  - Source current limit: **3.0 A to 4.5 A**
  - Sink current limit: **3.5 A to 5.5 A**
White Rabbit Switch (WRS)

SCB LAYOUT
White Rabbit Switch (WRS)

PCB features:

- **uTCA Requirements:**
  - MCH uTCA **Board-3** shape
  - **1.6 mm ± 0.16 mm** thickness

- **10-layers** PCB stack-up:
  - 5 layers for GND and Power Supplies
  - 5 routing layers
  - Class 6

- Single ended impedance: **50 Ω**
- Differential impedance: **100 Ω**

Calculations made by www.polarinstruments.com
10-Layer PCB Stack-up:
White Rabbit Switch (WRS)

External TOP and BOTTOM layers:

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<thead>
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<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate 1 Height (H1)</td>
<td>0.1100</td>
</tr>
<tr>
<td>Substrate 1 Dielectric (Er1)</td>
<td>4.6000</td>
</tr>
<tr>
<td>Lower Trace Width (W1)</td>
<td>0.1750</td>
</tr>
<tr>
<td>Upper Trace Width (W2)</td>
<td>0.1750</td>
</tr>
<tr>
<td>Trace Thickness (T1)</td>
<td>0.0420</td>
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<tr>
<td>Impedance (Zo)</td>
<td>49.95</td>
</tr>
</tbody>
</table>

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<td>0.1250</td>
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<tr>
<td>Upper Trace Width (W2)</td>
<td>0.1250</td>
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<tr>
<td>Trace Separation (S1)</td>
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<td>Trace Thickness (T1)</td>
<td>0.0420</td>
</tr>
<tr>
<td>Differential Impedance (Zdiff)</td>
<td>100.01</td>
</tr>
</tbody>
</table>
Internal Mid-Layers:

Offset Stripline 1B1A

- Substrate 1 Height: H1 = 0.1760
- Substrate 1 Dielectric: Er1 = 4.7000
- Substrate 2 Height: H2 = 0.1500
- Substrate 2 Dielectric: Er2 = 4.5000
- Lower Trace Width: W1 = 0.1090
- Upper Trace Width: W2 = 0.1090
- Trace Thickness: T1 = 0.0170
- Impedance: Zo = 50.04

Edge-Coupled Offset Stripline 1B1A

- Substrate 1 Height: H1 = 0.1760
- Substrate 1 Dielectric: Er1 = 4.7000
- Substrate 2 Height: H2 = 0.1500
- Substrate 2 Dielectric: Er2 = 4.5000
- Lower Trace Width: W1 = 0.1000
- Upper Trace Width: W2 = 0.1000
- Trace Separation: S1 = 0.2608
- Trace Thickness: T1 = 0.0170
- Differential Impedance: Zdiff = 99.99
Preliminary PCB Components Placement
Connectors Components Placement:
White Rabbit Switch (WRS)

CPU_100M_Ethernet Components Placement:
CPU_IO_Ports Components Placement:
White Rabbit Switch (WRS)

CPU_JTAG_Power_PLL Components Placement:
White Rabbit Switch (WRS)

CPU_Memory Components Placement:
White Rabbit Switch (WRS)

External WatchDogs Components Placement:
White Rabbit Switch (WRS)

SCB_CLKs Components Placement:
FPGA_Configuration Components Placement:
CPU ARM9 Component Placement:
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SMI_Link_7-12 Components Placement:
White Rabbit Switch (WRS)

FPGA_GTX Components Placement:
FPGA_System_Monitor Components Placement:
White Rabbit Switch (WRS)

Power_Supply Components Placement
White Rabbit Switch (WRS)

QDRII_mem Components Placement:
RS232_USB_ports Components Placement:
White Rabbit Switch (WRS)

SCB_PLLs Components Placement:
QDR Layout
White Rabbit Switch (WRS)

BOARD DEVELOPMENT STATUS & PLANNING
V3 schematics version **finished**.

- With some delay due to last minute modifications and because of the necessity to set-up the CERN-7S working flow as well as the utilization of new tools for 7S engineers (from PADS to Altium).

- Schematics revised and **approved**.
Components for the firsts PCB prototypes purchased by 7S.

PCB Routing started.

- 10-layers stack-up defined
- Component placement done.
  - Modifications due to the routing process still possible
- Aprox. 20% of routing
  - Routed elements: FPGA EBI1, SDRAM, FLASH (EBI 0), one QDR finished
SCB development planning

- Schematics → done
- Layout → running (expected date to deliver to fabrication: May 6)
  - ~One month delay due to schematics delay
  - Contingency plan: 3 engineers doing the routing.
- First prototypes → End of June (according to planning)
  - Components already bought and delivered
  - Contacts with mounting companies done.
- Testing → End of June onwards

ARM modification?
White Rabbit Switch (WRS)

CONCLUSIONS
Conclusions: board comments

- Physical size and shape make very difficult the routing process.
- Noise problems due to placement?
- QDR lines matching
- FPGA package big for the board shape
- ARM package (0.8 mm pitch, pad + clearance requires modify lines width to match impedances)
- FPGA assignment could not be optimal → dummy design as solution
  - We already uses MIG interface for QDRII pinout.
Low cost, fast development ... → robustness analysis of the board would be required.

- **FTA and FMEDA/FMECA** analysis.
  - It allows to detect "tend to failure" elements
  - Simplify the testing and reparation process
  - Many times provides of "easy solutions" to reduce system failures
  - **MTBF** calculation

- Fault tolerant software and FPGA firmware design
  - Run-time monitoring of critical functionalities

- Critical elements Redundancy

- Fabrication for durability
Conclusions: planning

Delay from initial planning: 1 month
- Contingency plan: 3 engineers working on the PCB
- First prototypes delivery on-time as far as no extra delays be required → new processor??

Others WRS elements plans
- Board 1, 2 and 4 design as well as AMC nodes or miniBackplane board?
- FPGA cores (QDRII SRAM)