The White-rabbit NIC (Network Interface Card) reference design

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WR NIC reference design

Development of gateware and software to make the combination of a SPEC and a DIO mezzanine as a **White Rabbit Network interface card** under Linux.

- Based on WR SPEC nodes, one master and one slave.
- FMC-DIO card allows basic operations: input timestamping (8 ns accuracy), programmable output pulse generation (1 ns accuracy, 8 ns aligned).
- Network interface card implementing the White Rabbit technology (PTPv2 compliant).
- Network packages include accurate time-stamping information generated/timestamped at the hardware (currently 8 ns, 1ns driver T.B.D.)
NIC project elements

- Application examples
  - SPEC-GN4124 drivers

- FPGA gateware
  - LM32 WRCORE firmware

Software (Linux PC)

Hardware (SPEC + FMC-DIO boards)
The starting kit contains all you need to play with the NIC reference design.
WR SPEC starting kit

- Board design is stable (fmc-dio latest modification included)
- Production done according IPC-610-2 regulations.
- Board test are available
  - PTS for SPEC
  - PTS for FMC-DIO
- CE certification done
NIC related projects

- OHWR design tools
  - HDLMake, Wishbone slave generator, git/SVN, ..

- NIC gateware
  - NIC project: http://www.ohwr.org/projects/wr-nic/wiki
  - WRPC: http://www.ohwr.org/projects/wr-cores/wiki/Wrpc_core

- SPEC
  - Hardware http://www.ohwr.org/projects/spec/wiki
  - Software (driver, fmc-bus and NIC working examples) http://www.ohwr.org/projects/spec-sw/wiki
  - Golden FPGA gateware (spec-init.bin) http://www.ohwr.org/projects/spec/repository/show/trunk/hdl/golden

- LM32 firmware:
  - Available at: http://www.ohwr.org/projects/wrpc-sw/

- Starting kit tutorial → ready to be released!
  - Where?
WR SPEC Starting Kit (Beta)
6th Nov 2012

White-Rabbit NIC Gateware
21 Jun 2012

SPEC Software Support
October 2012
A driver for the SPEC card and its FMC module

FMC Bus Abstraction for Linux
July 2012
Implementing a bus abstraction for I/O routines

Javier Diaz, UGR-7S

Alessandro Rubini for CERN (BI-CO-HT)
First contact for people interesting on WR technology.

Not necessarily developers

- Quick start guide, even for simple users → first WR contact to newcomers
- Focus on WR concepts, overview of the technology capabilities
- Good for setting up tool chains, hardware configuration, etc..
- Provide links to developers & engineers → go into details
Simple gateware to illustrate the WR NIC functionalities

- Includes de WRPC as key core for implementing WR functionalities.
- LM32 core is used as embedded softprocessor.
- Simple FMC-DIO card core controller is implemented as a Wishbone bus slave.
- Input/output pulses produce interrupts so can be easily captured by the PC.
Basic on-chip architecture

From DIO, TxTSU and NIC

DIO core

DIO, FMC

WB intercon

GN4124 core

GN4124 PCIe bridge

WRPC

NIC

SFP

TxTSU
NIC gateware limitations

- FMC-DIO channel signals are shared between WRPC and DIO core.
  - If grand-master configuration is used, channel 4 and 5 of DIO card are not available for the normal operation.

- I2C signal controlled by WRPC.
  - I2C signals to set threshold of the ADCMP604 comparator and access to EEPROM memory (24AA64) are not available to DIO core.

- Programmable output can be overwrite without output generation
  - There is not any FIFO mechanism for storing multiple programmable outputs of FMC-DIO channels.
NIC software

Alessandro talk!
Conclusions

NIC reference design illustrate the basic functionalities of WR technology
- Starting kits are ready to customers

- Supported/composed by multiple projects (HW, gateware, firmware, drivers and example applications).

- Simple – ready to go tutorial for newcomers
  ➔ starting kit docs
Thank you for your attention

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