Introduction to White Rabbit

Maciej Lipiński
on behalf of
the White Rabbit Team

BE-CO-HT

WR Training
White Rabbit in nutshell

- Accelerator’s control and timing
White Rabbit in nutshell

- Accelerator’s control and timing
- Renovation of General Machine Timing
White Rabbit in nutshell

- Accelerator’s control and timing
- Renovation of General Machine Timing
- Ethernet Local Area Network (LAN)
White Rabbit in nutshell

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- Ethernet Local Area Network (LAN)
- LAN with two additional services:
White Rabbit in nutshell

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- Ethernet Local Area Network (LAN)
- LAN with two additional services:
  1. Sub-ns synchronization
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- LAN with two additional services:
  1. Sub-ns synchronization
  2. Deterministic data delivery
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- LAN with two additional services:
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  2. Deterministic data delivery
- Open hardware & software:
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- LAN with two additional services:
  1. Sub-ns synchronization
  2. Deterministic data delivery
- Open hardware & software:
  - WR Switch
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- Open hardware & software:
  - WR Switch
  - WR Node
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  - WR Switch
  - WR Node
- Commercially available
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- LAN with two additional services:
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  2. Deterministic data delivery
- Open hardware & software:
  - WR Switch
  - WR Node
- Commercially available
- Growing number of applications
Applications
Applications
Applications

[Diagram showing CMS and ALICE experiments with LHC 27 km]

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Applications

- CMS
- ALICE
- LHC - 27 km
Applications

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Applications
Outline

1. Introduction to White Rabbit
2. Sub-ns synchronisation
3. Deterministic Data Distribution
4. Network Elements
5. Applications at CERN
6. Summary
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</tbody>
</table>
White Rabbit synchronisation

- It provides:
  - **Sub-ns** accuracy
  - **Sub-50 ps** precision

**White Rabbit synchronisation**

- **Sub-ns** accuracy
- **Sub-50 ps** precision

**Reference value**

**Accuracy**

**Probability density**

**Value**

**Precision**

**Time & Data Master**

**Control Data**

**GPS**

**Time & Data Master**

**Control Data**

**GPS**

**10km**

**2000 nodes**
White Rabbit synchronisation

- It provides:
  - **Sub-ns** accuracy
  - **Sub-50 ps** precision

- It uses:
  - Precision Time Protocol (IEEE 1588)
  - Layer 1 syntonization
  - Digital Dual Mixer Time Difference
  - Link delay model
Precision Time Protocol (PTP)

- Packet-based synchronization protocol

\[
\delta_{\text{ms}} = \left( t_4 - t_1 \right) - \left( t_3 - t_2 \right)
\]

\[
\text{clock offset}_{\text{ms}} = t_2 - t_1 + \delta_{\text{ms}}
\]

Limitations:
- free-running oscillators
- timestamping precision
- medium asymmetry

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Precision Time Protocol (PTP)

- Packet-based synchronization protocol
- Simple calculations:
  - link delay $\delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$
  - clock offset $\theta_{ms} = t_2 - t_1 + \delta_{ms}$
Precision Time Protocol (PTP)

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- Sub-$\mu$s synchronisation
Introduction

Synchronisation

Determinism

Network Elements

Applications at CERN

Summary

Precision Time Protocol (PTP)

- Packet-based synchronization protocol
- Simple calculations:
  - link delay\(_{ms}\) \(\delta_{ms} = \frac{(t_4-t_1)-(t_3-t_2)}{2}\)
  - clock offset\(_{ms}\) = \(t_2 - t_1 + \delta_{ms}\)

- Sub-\(\mu\)s synchronisation

- Limitations:
  - free-running oscillators
  - timestamping precision
  - medium asymmetry
Layer 1 Synchronization

- All network devices use the same physical layer clock
- Clock is encoded in data by master and recovered by slave
- Clock loopback and phase detection allow precise timestamps
Digital Dual Mixer Time Difference (DDMTD)

**Input:**
- frequency $f_{in}$ [Hz]
- phase $\phi_{in}$ [rad]

**Output:**
- proportionally lower frequency $f_{out}$ [Hz]
- equal phase $\phi_{in}$ [rad]

Zooming effect:
$$x_{in}[\text{ns}] = 1 + 2^N \cdot x_{out}[\text{ns}]$$

** PLL Equation:**
$$f_{DDMTD} = \frac{2^N}{2^N + 1} f_{Ain}$$
Digital Dual Mixer Time Difference (DDMTD)

- **Input:**
  - frequency $f_{in}$ [Hz]
  - phase $\phi_{in}$ [rad]

- **Output:**
  - proportionally lower frequency $f_{out}$ [Hz]
  - equal phase $\phi_{in}$ [rad]

The Digital Dual Mixer Time Difference (DDMTD) is a device that takes an input signal with frequency $f_{in}$ and phase $\phi_{in}$ and outputs a signal with a proportionally lower frequency $f_{out}$ and equal phase $\phi_{in}$. The relationship between the input and output frequency is given by:

$$f_{DDMTD} = \frac{2^N}{2^N + 1} f_{Ain}$$

Where $N$ is a counter that increments by 1 for each output signal. The zooming effect is given by:

$$x_{out} = \frac{1}{1 + 2N} x_{in}$$

This relationship shows how the input signal is scaled down by a factor of $(1 + 2N)$ to produce the output signal.
Digital Dual Mixer Time Difference (DDMTD)

- **Input:**
  - frequency $f_{in}[\text{Hz}]$
  - phase $\phi_{in} [\text{rad}]$

- **Output:**
  - proportionally lower frequency $f_{out}[\text{Hz}]$
  - equal phase $\phi_{in} [\text{rad}]$

- **Zooming effect:**
  \[ x_{in}[\text{ns}] = \frac{1}{1+2^N} \cdot x_{out}[\text{ns}] \]

Diagram:

- PLL
  \[ f_{DDMTD} = \frac{2^N}{2^N + 1} f_{Ain} \]
- Counters
- Clocks
- Timing:
  - $x_{in}[\text{ns}]$
  - $x_{out}[\text{ns}]$

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Link delay model

- **Hardware delays:**
  - Calibrate static delays: $\Delta_{TXM}, \Delta_{RXM}, \Delta_{TXS}, \Delta_{RXS}$
  - Measure semi-static delays: $\epsilon_M, \epsilon_S$

- **Link asymmetry:**
  - Single fibre for two-way communication
  - Fibre asymmetry coefficient: $\alpha = \delta_{MS} - \delta_{SM}$

Diagram:
- **WR Master**
  - WR gear
  - $\Delta_{TXM}$
  - $\Delta_{RXM}, \epsilon_M$
  - $\delta_{SM}$
- **WR Slave**
  - WR gear
  - $\epsilon_S$
  - $\Delta_{RXS}$

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Link delay model

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Link delay model

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- **Link asymmetry:**
  - Single fibre for two-way communication
  - Fibre asymmetry coefficient: \( \alpha = \frac{\delta_{MS} - \delta_{SM}}{\delta_{SM}} \)
Synchronisation performance: basic test setup

Stable oscillator

Cesium beam clock

WR Switch (master)

10 MHz
1 PPS
5 km

Oscilloscope

WR Switch (slave 1)

1 PPS

WR Switch (slave 2)

5 km

WR Switch (slave 3)

5 km

hot-air gun
Synchronisation performance: test results

Histogram of offsets between master and each slave

- Master (CH1)
- Slave 1 (CH2)
  - mean = 161.86 ps
  - sdev = 5.45 ps
- Slave 2 (CH3)
  - mean = 24.67 ps
  - sdev = 5.30 ps
- Slave 3 (CH4)
  - mean = -135.25 ps
  - sdev = 6.14 ps
White Rabbit is ...

... the most accurate implementation of the IEEE 1588 in the world.
WR standardisation in IEEE 1588

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- IEEE 1588 standard is being revised
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- IEEE 1588 standard is being revised
- Dedicated High Accuracy sub-committee
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... the most accurate implementation of the IEEE 1588 in the world.

- IEEE 1588 standard is being revised
- Dedicated High Accuracy sub-committee
- WR extensions will be included in the standard
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Determinism

Deterministic system

A deterministic system is predictable: it provides calculable and consistent characteristics of operation.
Deterministic Data Distribution

White Rabbit switch provides deterministic data forwarding
Deterministic Data Distribution

White Rabbit switch provides deterministic data forwarding

- Openly available design
White Rabbit switch provides deterministic data forwarding

- Openly available design
- Optimized for latency
White Rabbit switch provides deterministic data forwarding

- Openly available design
- Optimized for latency
- Supports prioritization

![Graph showing latency over one and two WR switches](image-url)
White Rabbit switch provides deterministic data forwarding:

- Openly available design
- Optimized for latency
- Supports prioritization
- Provides for critical traffic:
  - upper-bound latency
  - reserved resources
WR Switch

- Central element of WR network
- 18 port Gigabit Ethernet switch with WR features
- Supports VLANs, SNMP, Web-based management
- Optical transceivers: up to 10km, single-mode fiber
- Fully open design commercially available
Open IP Core: WR PTP Core
WR Node

- Open IP Core: WR PTP Core
- Currently runs on:
  - **Xilinx**: Spartan, Kintex-7, Zynq
  - **Altera**: Aria II and V

![WR Node Diagram]

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WR Node

- Open IP Core: WR PTP Core
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- Open HW WR-enabled boards:
  - PCIe
  - VME
  - PXIe
  - CRIO
  - Open HW FMCs: ADC, DAC, TDC, Fine Delay, ...

You can integrate WR into your design!
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- You can integrate WR into your design!
WR PTP Core - reference design

- PLL DACs drive (SPI)
- 5:1 PLL, Fanout
- DAC 16 bit
- VCTCXO 25 MHz 2.5 ppm
- REF clock generator
- DAC 16 bit
- VCXO 20 MHz 100 ppm
- DMTD clock generator
- FPGA WRPC
- IO
- IO
- IO
- IO
- IO
- IO
- GCLK
- MGTREFCLK
- IO
- IO
- IO
- IO
- IO
- IO
- GCLK, 6.25:1 PLL
- MGTX
- MGTRX
- OW
- I2C
- SFPCTRL
- SFPTX
- SFP
- SFP
- SFP
- SFP
- SFP
- PPS
- REFCLK
- UART
- GPIO
- I/O Connector (optional)
- Unique ID (optional)
- EEPROM (optional)
- SFP
- FO TxRx

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White Rabbit PTP Core

- Tunable oscillators
- SFP
- Pipelined WB MAC I/F
- WR PTP Core
- UART
- Periph
- SoftPLL
- 1-PPS
- Lattice Mico32
- RAM
- mini-NIC
- Fabric redirector
- Endpoint
- Wishbone crossbar
- Control Wishbone I/F
- Flash / EEPROM
- PHY (GTP, GTX, ...)
- SFP

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White Rabbit PTP Core

The diagram illustrates the components and interfaces of the White Rabbit PTP Core:

- **Tx** and **Rx** indicate the transmission and reception of data through Ethernet
- **External PHY** connects the Ethernet interface
- **External oscillators** provide reference and DMTD clocks
- **EEPROM** stores configuration data
- **TBI/Serdes** for signal processing
- **WR PTP Core** integrates all components
- **MAC I/F** for communication
- **Pipelined WB Slave I/F** for data transfer
- **Timing I/F** for synchronization
- **Control/status pins** for configuration

Integration of these elements enables precise time synchronization and deterministic network operation.
Example WR PTP Core integration
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**Existing applications at CERN**

- **AD synchronisation**
  - Distribution of 10 MHz and 1 PPS
  - Operational since 2014
Existing applications at CERN

- **AD synchronisation**
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- **LHC Instabilities**
  - Trigger Distribution
  - Operational since 2015
Existing applications at CERN

- AD synchronisation
  - Distribution of 10 MHz and 1 PPS
  - Operational since 2014

- LHC Instabilities
  - Trigger Distribution
  - Operational since 2015

- PS WR-Btrain
  - Distribution of magnetic field
  - Experimental since 2015
Existing applications at CERN

- **AD synchronisation**
  - Distribution of 10 MHz and 1 PPS
  - Operational since 2014

- **LHC Instabilities**
  - Trigger Distribution
  - Operational since 2015

- **PS WR-Btrain**
  - Distribution of magnetic field
  - Experimental since 2015

- **Vibration transfer at LHC’s Point 1**
  - Synchronisation of geophones
  - Used in 2015
Current Developments

- **Diagnostics:**
  - Support SNMP in nodes
Current Developments

- **Diagnostics:**
  - Support SNMP in nodes
  - Integration with CERN tools

![SNMP Interface](image_url)
Current Developments

- **Diagnostics:**
  - Support SNMP in nodes
  - Integration with CERN tools

- **New hardware**
  - WRAP - White RAbbit Pluggable
  - New WR switch with 10GBit ports
Current Developments

- Diagnostics:
  - Support SNMP in nodes
  - Integration with CERN tools
- New hardware
  - WRAP - White RAbbit Pluggable
  - New WR switch with 10GBit ports
- Preparation of new White Rabbit Timing (WRT), successor of GMT
- New applications....
Distributed Direct Digital Synthesis

- Can provide various clocks (RF of many rings and linacs) with a single, standard link.
- Replaces dozens of cables with a single fiber.
- Works over big distances without degrading signal quality.
Common clock in entire network: no skew between ADCs.
Ability to sample with different clocks via Distributed DDS.
External triggers can be time tagged with a TDC and used to reconstruct the original time base in the operator’s PC.
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- A versatile solution for general control and data acquisition
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- Open H/W & S/W with commercial support
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- Active participation in IEEE1588 revision process
Summary

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- More applications than ever expected
Summary

- A versatile solution for general control and data acquisition
- Open H/W & S/W with commercial support
- Standard-compatible and standard-extending
- Active participation in IEEE1588 revision process
- More applications than ever expected
- Supported by BE-CO and recommended CERN fieldbus
A versatile solution for general control and data acquisition
Open H/W & S/W with commercial support
Standard-compatible and standard-extending
Active participation in IEEE1588 revision process
More applications than ever expected
Supported by BE-CO and recommended CERN fieldbus

http://www.ohwr.org/projects/white-rabbit/wiki

Thank you
WR PTP Core - resource utilization

<table>
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<tr>
<th>Slice Logic Utilization</th>
<th>Used</th>
<th>Available</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slice Registers</td>
<td>6,791</td>
<td>54,576</td>
<td>12%</td>
</tr>
<tr>
<td>Number of Slice LUTs</td>
<td>8,956</td>
<td>27,288</td>
<td>32%</td>
</tr>
<tr>
<td>Number of occupied Slices</td>
<td>3,345</td>
<td>6,822</td>
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<tr>
<td>Number of MUXCYs used</td>
<td>1,532</td>
<td>13,644</td>
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<tr>
<td>Number of bonded IOBs</td>
<td>26</td>
<td>296</td>
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<tr>
<td>Number of RAMB16BWERS</td>
<td>56</td>
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<td>Number of RAMB8BWERS</td>
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<tr>
<td>Number of BUFIO2/BUFIO2_2CLKs</td>
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<tr>
<td>Number of BUFG/BUFGMUXs</td>
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<tr>
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<tr>
<td>Number of DSP48A1s</td>
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<td>58</td>
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<tr>
<td>Number of GTPA1_DUALs</td>
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<td>2</td>
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<tr>
<td>Number of PLL_ADVs</td>
<td>2</td>
<td>4</td>
<td>50%</td>
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</table>