ZEN: Zynq based embedded WR node

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Talk outline

1. Introduction to ZEN board and Zynq devices
2. WRPC-2P
3. WR-ZEN Fine Delay reference design (Gateware, Linux kernel & Software, LM32 firmware)
4. Conclusion
5. Future work
6. References
Zynq architecture

Zynq: hard ARM dual core microprocessor + FPGA logic in the same chip.

- The best of both worlds:
  - Linux OS support.
  - Design of custom hardware accelerators.
WRPC-Dual-Port motivation

- One White Rabbit PTP Core to control two SFP ports.

- Two WR Ethernet ports allow:
  1. Redundancy protocols (fault tolerant)
  2. Data forwarding between SFPs.
  3. Daisy-chain configurations (master-slave on a single node)
WRPC-Dual-Port
architecture
WRPC-Dual-Port into ZEN

- Using Zynq architecture:
  1. Provides on-chip processor with Linux
     \[ \text{Zen} = \text{SPEC} + \text{PC} \]
  2. Timing is done at LM32 (node behavior)
  3. FMC support (SPEC-like approach)
ZEN TIE & Phase noise
(preliminary results)
Other WRPC-DP equipment

WR-ZEN Time Provider
Other WRPC-DP equipment

WR-LEN
WR-ZEN FINEDEL
reference design
WR-ZEN FINEDEL reference design

- The reference design includes a compliant WR node with Fine Delay FMC capabilities.
- Done as UGR contribution for SKA (tested by JIVE, see previous talk).
WR-ZEN FINEDEL
Gateware
The Linux OS is generated using the Buildroot tool as in the WR Switch Software OHWR repository.

- The Buildroot has been updated and now we use the buildroot-2015.11 release.

- The Linux kernel is a modified version of the 3.19 release (linux-xlnx-2015.4) with some additional drivers for the Xilinx IP cores.

- The U-boot (custom version based on u-boot-xlnx (zynq based)) is the choosen bootloader instead of the Barebox.
WR-ZEN FINEDEL Linux Software

• Drivers:
  – **WR-ZEN carrier driver**: It is inspired by the SPEC carrier driver but it includes additional capabilities such as the Linux network interfaces for the optical fiber ports.
  – Some minor changes for the Fine Delay FMC driver.
  – Fixed a bug of ZIO kernel module with the ARM architecture.

• Userspace tools:
  – “SPEC-like tools”: zenmem, zen-cl, zen-fwloader, zen-vuart...
The LM32 software has been updated to work properly with the new WRPC dual port IP core.

- The I2C driver has been modified to configure the I2C switch available on the WR-ZEN board.

- Some GPIOs are not directly accessible through FPGA pins. They are placed in the I2C bus and it is necessary to implement a polling mechanism to update their status periodically.
Conclusion

I. WRPC-DP includes new capabilities for fault-tolerant and reliable applications.

II. New clocking circuitry

III. The Zynq technology allows higher flexibility and the application of codesign techniques.

   I. All programmable: software & gateware is inside the same chip!!

   II. Every WR node has a Linux Operating System and can be programmed for any specific or general purpose application.

   III. Easy use for non-hw experts.

IV. ZEN behaves as an standalone node:

   \[ \text{ZEN} = \text{PC+SPEC} + \text{FMC features}. \]
Future work

- High bandwidth over the same data & timing optical fiber link (ongoing work).
- Add additional FMC cards support such as DIO, TDC, ADC, etc.
- Optimize the system parameters (FPGA MMCM + WR PLL + external PLL, etc.. ) to reduce jitter (taking advantage of available new degrees of freedom)
  - Thanks to Henk Peek & Mattia Rizzi for their interesting suggestions.
References

(1) WR-ZEN, Seven Solutions,  

(2) Zynq Technology, Xilinx Inc,  

(3) OHWR, OHWR community, http://www.ohwr.org/  
  • Hardware, http://www.ohwr.org/projects/zen-wr-hw  
- FMC Fine Delay Hardware,  
http://www.ohwr.org/projects/fmc-delay-1ns-8cha/wiki  
Thanks for your attention!

Questions?