White Rabbit
A quick introduction

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Outline

1. Introduction
2. Technology
3. Equipment
4. Performance
5. Current developments
6. Conclusions
What is White Rabbit?

- A solution to problems in distributed real-time controls and data acquisition
- Based on well-known technologies
- Open Hardware and Open Software with commercial support
- International collaboration
- Many users: CERN, GSI, KM3NET, cosmic ray detectors, metrology labs...
## Why we use Open Hardware?

<table>
<thead>
<tr>
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<th>Commercial</th>
<th>Non-commercial</th>
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<td>Open</td>
<td>Winning combination. Best of both worlds.</td>
<td>Whole support burden falls on developers. Not scalable.</td>
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<td>Proprietary</td>
<td>Vendor lock-in.</td>
<td>Dedicated non-reusable projects.</td>
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- Get a design just the way we want it
- Peer review and design re-use
- Healthier relationship with companies
White Rabbit: an *extension* of Ethernet

- Standard Ethernet network
- Ethernet features (VLAN) & protocols (SNMP)
- High accuracy synchronisation
- Reliable and low-latency Control Data
White Rabbit application examples

- CERN and GSI
White Rabbit application examples

- CERN and GSI
- HiSCORE: Gamma&Cosmic-Ray experiment


> Institute for Nuclear Research of the Russian Academy of Sciences
> Moscow State University
> Irkutsk State University
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- The Large High Altitude Air Shower Observatory
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More WR collaborators:
https://www.ohwr.org/projects/white-rabbit/wiki/WRUsers
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White Rabbit technology

Based on

- Gigabit Ethernet over fibre
- IEEE-1588 protocol
White Rabbit technology

Based on
- Gigabit Ethernet over fibre
- IEEE-1588 protocol

Enhanced with
- Layer 1 syntonization
- Digital Dual Mixer Time Difference (DDMTD)
- Link delay model
- WR-PTP (backward-compatible extension of PTP)
Ethernet switches in a nutshell
Ethernet switches in a nutshell

Introduction to White Rabbit
Ethernet switches in a nutshell

PC1 → PC2

Ethernet Switch

D: 00-1B-C5-00-00-02
S: 00-1B-C5-00-00-01

PC 1
MAC: 00-1B-C5-00-00-01

PC 2
MAC: 00-1B-C5-00-00-02

PC 3
MAC: 00-1B-C5-00-00-03
Introduction to White Rabbit

Ethernet switches in a nutshell

Ethernet Switch

PC1 → PC3

PC 1

PC 2

PC 3

MAC: 00-1B-C5-00-00-01
MAC: 00-1B-C5-00-00-02
MAC: 00-1B-C5-00-00-03

D: 00-1B-C5-00-00-03
S: 00-1B-C5-00-00-01

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Ethernet switches in a nutshell

- PC 1: MAC: 00-1B-C5-00-00-01
- PC 2: MAC: 00-1B-C5-00-00-02
- PC 3: MAC: 00-1B-C5-00-00-03

- Ethernet Switch:
  - D: 00-1B-C5-00-00-02
  - S: 00-1B-C5-00-00-01

- PC 2:
  - D: 00-1B-C5-00-00-03
  - S: 00-1B-C5-00-00-01
Precision Time Protocol (IEEE 1588)

- Frame-based synchronisation protocol.
- Simple calculations:
  - link delay \( \delta_{ms} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2} \)
  - clock offset \( t_{ms} = t_2 - t_1 + \delta_{ms} \)
**Precision Time Protocol (IEEE 1588)**

- Frame-based synchronisation protocol.
- Simple calculations:
  - link $delay_{ms} \delta_{ms} = \frac{(t_4-t_1)-(t_3-t_2)}{2}$
  - clock $offset_{ms} = t_2 - t_1 + \delta_{ms}$
- Disadvantages
  - assumes symmetry of medium
  - all nodes have free-running oscillators
  - frequency drift compensation vs. message exchange traffic
Layer 1 Syntonization

- All network devices use the same physical layer clock.
- Clock is encoded in the Ethernet carrier and recovered by the receiver chip.
- Phase detection allows sub-ns delay measurement.

![Diagram of Layer 1 Syntonization](image-url)
Digital Dual Mixer Time Difference

**DDMTD**

- Used for precise phase measurements
- Implemented in FPGA and SoftPLL
- 62.5MHz WR clock and N=14 results in 3.814kHz output signals

\[
\frac{2^n}{2^2+1} f_{\text{Ain}}
\]

- helper PLL
- deglitcher & pulse shaping
- free-running counters

```
clk\_Ain
\[x_{\text{in}}\]

clk\_Bin
\[x_{\text{out}}\]
```
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Typical WR network
White Rabbit Switch

- Central element of WR network
- 18 port gigabit Ethernet switch with WR features
- Optical transceivers: up to 10km, single-mode fibre
- Fully open design, commercially available
Introduction to White Rabbit

Simplified block diagram of the hardware

Xilinx Virtex6 FPGA

18 SFP cages

64MB DDR2

256MB NAND

8MB boot flash

Power supply 12V DC 80W

Cooling FANs

Debug ports

Back panel

Management ports

Front panel

10 MHz in/out

1-PPS in/out

Clocking resources

Power supply 12V DC 80W

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Introduction to White Rabbit
FMC-based Hardware Kit

- All carrier cards are equipped with a White Rabbit port.
- Mezzanines can use the accurate clock signal and “TAI” (synchronous sampling clock, trigger time tag, ...).
White Rabbit Node in more detail

WR Node Device

FPGA

WR PTP core

EtherBone

FMC-base CARD

SPEC

WR Node IP Core

WR PTP Core

MAC I/F

pipelined WB Slave I/F

timing I/F

ccontrol/status pins

SOURCE

sink

Tx Ethernet

Rx

external PHY

external oscillators

CLPWR

CLPWco

I-PPS

Timecode

frequency

source

sink

EEPROM

PC

Network

SFP
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WR time transfer performance: basic test setup

Stable oscillator

Cesium beam clock

10 MHz

1 PPS

5 km

Oscilloscope

WR Switch (master)

WR Switch (slave 1)

WR Switch (slave 2)

WR Switch (slave 3)

CH1

CH2

CH3

CH4

1 PPS

1 PPS

1 PPS

1 PPS

5 km

5 km

5 km

hot-air gun

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Introduction to White Rabbit
WR time transfer performance: test results

Histogram of offsets between master and each slave

- **Master (CH1)**
- **Slave 1 (CH2)**
  - mean = 161.86 ps
  - sdev = 5.45 ps
- **Slave 2 (CH3)**
  - mean = 24.67 ps
  - sdev = 5.30 ps
- **Slave 3 (CH4)**
  - mean = -135.25 ps
  - sdev = 6.14 ps
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Switches and nodes are commercially available

Work now revolves around better diagnostics and remote management of WR networks as well as improving the phase noise and performing extensive network stress tests.
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Standardisation

IEEE 1588 revision process is ongoing and contains a sub-committee (High Accuracy) dedicated to White Rabbit. Revised standard expected in mid-2018.
**Current developments**

**Switches and nodes are commercially available**

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**Standardisation**

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**Robustness**

Based on redundant information and fast switch-over between redundant fibres and switches.
Distributed Direct Digital Synthesis

- Replaces dozens of cables with a single fibre.
- Works over big distances without degrading signal quality.
- Can provide various clocks (RF of many rings and linacs) with a single, standard link.
Distributed oscilloscope

- **Common clock in entire network**: no skew between ADCs.
- **Ability to sample with different clocks** via Distributed DDS.
- **External triggers can be time tagged** with a TDC and used to reconstruct the original time base in the operator’s PC.
Open source (H/W & S/W), with commercial support
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- Open source (H/W & S/W), with commercial support
- More applications than ever expected
- A versatile solution for general controls and data acquisition
- Standard-compatible and standard-extending
- Active participation in IEEE1588 revision process. ISPCS 2018 will be at CERN. Consider submitting papers on applications of WR! See http://www.ispcs.org for details.
Need more information?

https://www.ohwr.org/projects/white-rabbit/wiki