Introducing hdlmake Version 2.0

Javier D. Garcia-Lasheras

Independent Consultant
Pamplona (SPAIN)

javier@garcialasheras.com

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Outline

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- Many others...

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- This is where we are now!

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Goals for the HDLMake v2.0 documentation

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A good quality documentation must be a fundamental piece for this release:

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- Synchronized with the code!!

Documentation: Sphinx

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- Extensive cross-references, code handling, API autodocumentation...

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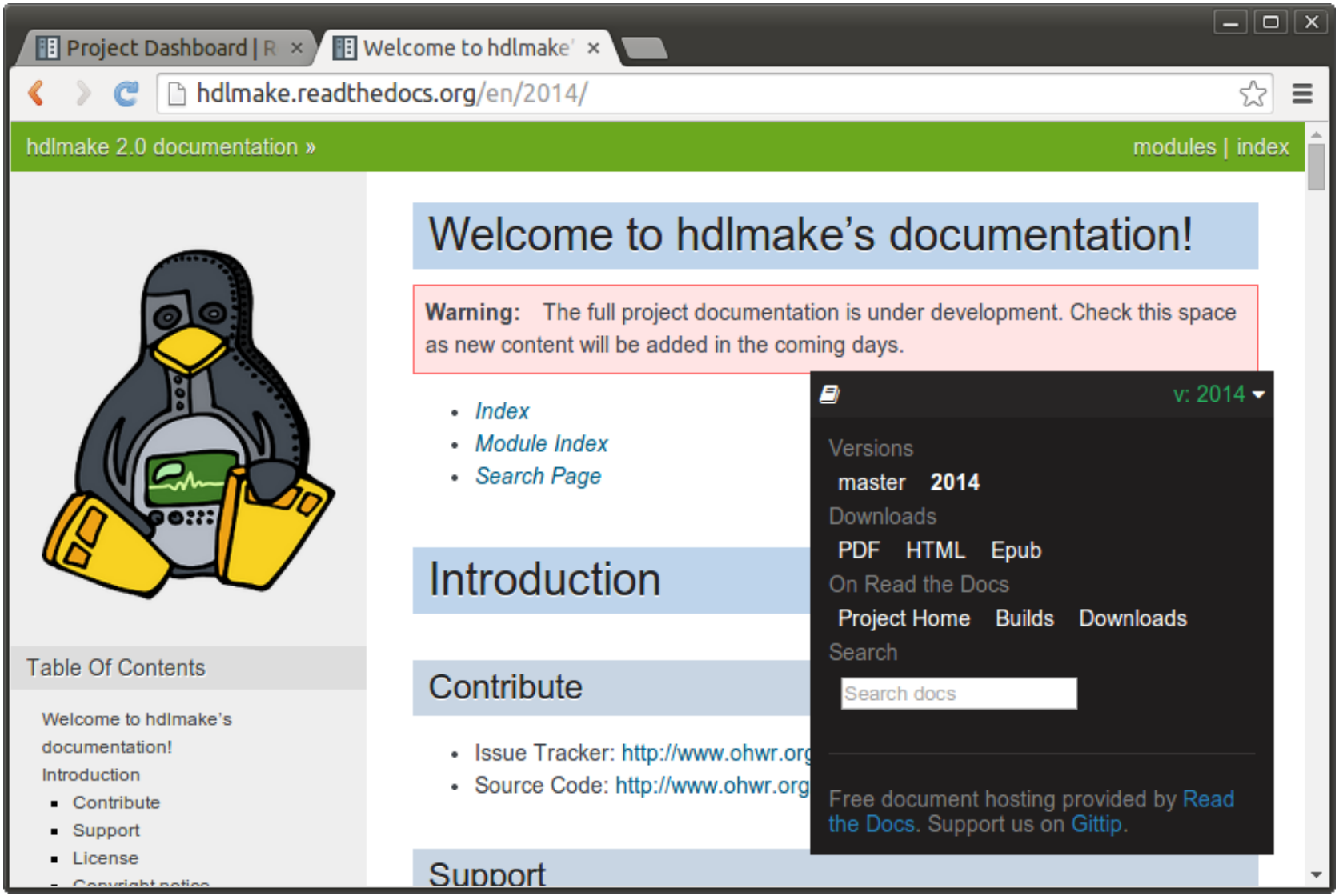
- It is written in Python, hosted in Github and released under MIT license.

Documentation: screenshot



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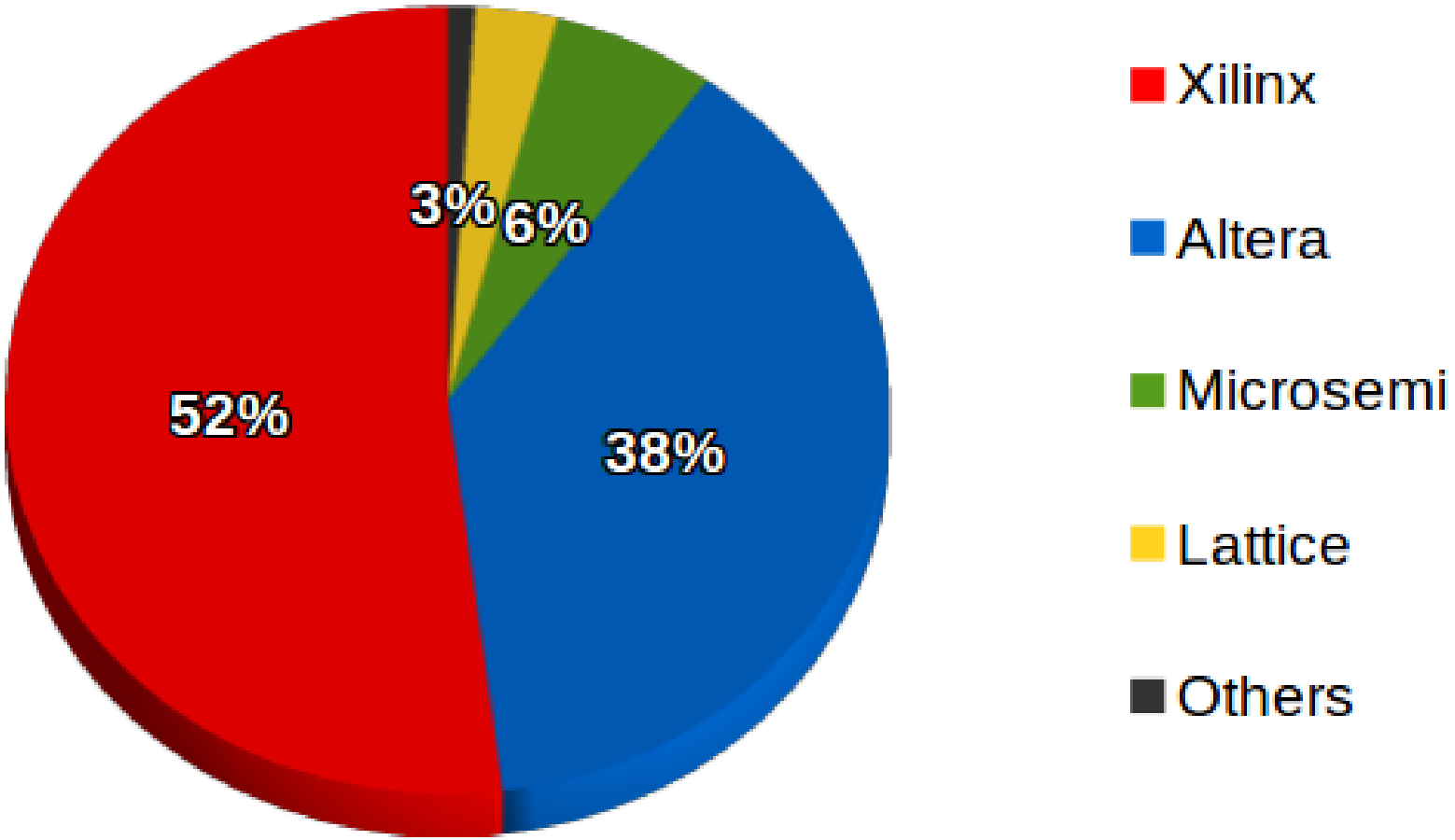
FPGA Market Share by Vendor



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Lattice

- Diamond IDE

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- GHDL (VHDL support only)

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- HDLMake has been modified to allow full compatibility with Cygwin environments.
- HDLMake over Cygwin has been tested on Windows 7 / 8 / 8.1

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The counter test

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The counter test root folder

```
user@host:~\$ tree -d -L 1 counter/
counter/
|-- modules
|-- sim
|-- syn
|-- testbench
`-- top
```

A very simple HDLMake module

A very simple HDLMake module

Overview of the counter modules

```
user@host:~\$ tree counter/modules/
counter/modules/
‘-- counter
    |-- verilog
    | |-- counter.v
    | ‘-- Manifest.py
    ‘-- vhdl
        |-- counter.vhd
        ‘-- Manifest.py
```

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```

The simplest Manifest.py for VHDL

```
files = ["counter.vhd",]
```

A very simple testbench

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The counter testbench folder

```
user@host:~\$ tree counter/testbench/
counter/testbench/
‘-- counter_tb
    |-- verilog
    | |-- counter_tb.v
    | ‘-- Manifest.py
    ‘-- vhdl
        |-- counter_tb.vhd
        ‘-- Manifest.py
```

A very simple testbench

The counter testbench folder

```
user@host:~\$ tree counter/testbench/
counter/testbench/
‘-- counter_tb
    |-- verilog
    | |-- counter_tb.v
    | ‘-- Manifest.py
    ‘-- vhdl
        |-- counter_tb.vhd
        ‘-- Manifest.py
```

The VHDL Manifest.py for counter testbench

```
files = ["counter_tb.vhd",]
modules = {"local":["../../../modules/counter/vhdl"],}
```

Covered simulation tools

Covered simulation tools

The simulation folder

```
user@host:~\$ tree -d -L 1 counter/sim
counter/sim
|-- aldec
|-- ghdl
|-- isim
|-- iverilog
`-- modelsim
```

Inside a simulation folder

Inside a simulation folder

e.g. the modelsim folder

```
user@host:~\$ tree counter/sim/modelsim/
counter/sim/modelsim/
|-- verilog
|  `-- Manifest.py
|-- vhdl
|  `-- Manifest.py
`-- vsim.do
```

Running a simulation

Running a simulation

e.g. Modelsim simulation top Manifest.py for VHDL

```
action = "simulation"
sim_tool = "modelsim"
top_module = "counter_tb"
sim_post_cmd = "vsim -do ../vsim.do -i counter_tb"
modules = {
    "local" : ["../../../testbench/counter_tb/vhdl"],
}
```

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```
action = "simulation"
sim_tool = "modelsim"
top_module = "counter_tb"
sim_post_cmd = "vsim -do ../vsim.do -i counter_tb"
modules = {
    "local" : ["../../../testbench/counter_tb/vhdl"],
}
```

Common simulation command sequence!

```
user@host:~\$ cd counter/sim/modelsim/vhdl
user@host:~\$ hdlmake
user@host:~\$ make sim_post_cmd
```

Real boards under test

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Sample FPGA boards for testing

```
user@host:~\$ tree -d -L 1 counter/top
counter/top
|-- brevia2_dk
|-- cyclone3_sk
|-- proasic3_sk
`-- spec_v4
```

A constrained top design

A constrained top design

e.g. the SPEC top board folder

```
user@host:~\$ tree counter/top/spec_v4/
counter/top/spec_v4/
|-- spec_top.ucf
|-- verilog
| |-- Manifest.py
| `-- spec_top.v
`-- vhdl
    |-- Manifest.py
    `-- spec_top.vhd
```

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```

The VHDL Manifest.py for a top board

```
files = ["spec_top.vhd", "../spec_top.ucf"]
modules = {"local":["../../../modules/counter/vhdl"],}
```

Covered synthesis tools

Covered synthesis tools

The synthesis folder

```
user@host:~\$ tree -d -L 1 counter/syn
counter/syn
|-- brevia2_dk_diamond
|-- cyclone3_sk_quartus
|-- proasic3_sk_libero
|-- spec_v4_ise
`-- spec_v4_planahead
```

Inside a synthesis folder

Inside a synthesis folder

e.g. SPEC v4 ISE folder

```
user@host:~\$ tree -d -L 1 counter/syn/spec_v4_ise
counter/syn/spec_v4_ise/
|-- verilog
| `-- Manifest.py
`-- vhdl
    `-- Manifest.py
```

Running a synthesis

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e.g. SPEC v4 synthesis Manifest.py with ISE

```
target = "xilinx"
action = "synthesis"
syn_device = "xc6slx45t"
syn_grade = "-3"
syn_package = "fgg484"
syn_top = "spec_top"
syn_project = "demo.xise"
syn_tool = "ise"
modules = {"local":["../../../top/spec_v4/vhdl"],}
```

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syn_tool = "ise"
modules = {"local":["../../../top/spec_v4/vhdl"],}
```

Synthesis command sequence!

```
user@host:~\$ cd counter/syn/spec_v4_ise/vhdl
user@host:~\$ hdlmake
user@host:~\$ make
```

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Keep in touch

If you are interested in knowing more about HDLMake, just take a look to its OHR project site:

▸ http://www.ohwr.org/projects/hdl-make

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