WR PTP Core block diagram

See next slide

DPM Time division multiplexed to four ports

User Application
Timing System block diagram

*With Phase offset*

\[ f_{\text{out}} = \frac{n}{n+1} f_{\text{in}} \]

\( f_{\text{out}} = \) Helper PLL or DMTD Clock
Simplified Timing System block diagram
(Without Phase offset)