Switch v3: hardware production test suite

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Compatibility: PTS already defined for SPEC board as guide.

Goal: detect any anomaly introduced during the manufacturing.
- System characterization, performance testbenches, etc. addressed at different test stages.
- Could be convenient to include stressed environmental conditions

The main test can be categorized according to:
- Visual inspections
- Off-line tests
- Functionality testing
Visual Inspections: independently of soldering manufacturer, a basic check must be done. The checkpoints must include:

- Short-cuts in connectors and CI.
- Main CIs orientation.
- Not mounted components.

Off-line test: in order to prevent board elements damage, the follow basic tests must be performed:

- Electric resistance between the main power supplies. It will detect short-cuts (mainly below the BGA) not detected by visual inspections.
- Power supplies voltages: avoid over-voltage that could produce damage. It requires simple multimeter for Vrms value or an oscilloscope to see complex defects (oscillations, noise, spikes...)
Functionality testing

- It must assure that the components and functionality of the equipment work properly.
- Fault detection & element localization & possible cause vs. test complexity trade-off
- NOTE: In order to accomplish with a whole functionality test, an auxiliary test equipment could be necessary (perhaps out of scope of ohwr)

Two possible approaches:
- High level (HL) functional testing (Linux based)
- Low level (LL) functional testing (independent / complete test of each board elements, mainly FPGA related ones)
LL Functionality testing of SCB

FPGA peripherals
- QDR memories
- AD9516 and DMTD PLLs
- VCXOs
- VCO DACs
- 40 GPIOs interface to main connector
- SMC clock inputs and outputs
- GTX transceivers
- I2C temperature sensors
- RS232 interface
LL/HL Functionality testing of SCB II

ARM peripherals:
- DDR memory
- SPI boot Flash
- NAND Flash
- Ethernet, USB and RS232 interfaces
- FPGA bitstream configuration
- FPGA EBI1 interface
LL/HL Functionality testing of Minibackplane

- I2C chips
- LEDs
- SFP connections
- FPGA USB interface
- ARM USB and RSA232 interfaces
- FPGA and Box Fan Controllers
High Level Functionality Testing (HLFT)

The solution already more advanced is based on loading a Linux kernel and executing different applications for testing the different elements.

- Supported by Benoit (7S) and Alessandro (GNUDD)

Test elements

- CPU responds
- JTAG port
- DBSU port
- Internal ROM (Reboot)
- Internal RAM
- DDR memory (EBI0)
- Ethernet port
- Dataflash memory
- NAND memory (EBI1)
- USB port
- CPU-FPGA flashing:
  - TK0, TD0
  - FPGA_INIT_B+FPGA_INIT_A
- CPU-FPGA channel (EBI1)
The different steps for the test should not be performed in bootstrap but in a linear way.

A first step is needed to check: CPU & DDR

The second step must be executed respecting the following properties:

- Load all the following files at once: at91bootstrap.bin, barebox.bin, kernel, filesystem
- Two ways of loading files in case one failed: JTAG and USB
- No use of TFTP for loading (in case Ethernet is failing we want to check the other components)
HLFT: actual workflow

Low level: testing the component that are need to load Linux (basic LLFT for the ARM)
- Loading from CPU
- Testing SRAM (g45memtest is loading?)
- Testing DDR (run g45memtest)

High level: testing all other components once the Linux is loaded
- Ethernet (Loading files from TFTP*)
- FPGA (flashing)
- CPU-FPGA bus
- USB bus*
- DF memory test
- NAND memory test
- PTS (testing FPGA components like SPEC) ...
- Flashing test (Reading back after reboot*)
Test example: G45memtest (DDR)

Still in development

Improve from Alessandro/Tomasz

Try to perform the same stress test as memtestx86 (9 +1 types)

1. Address test, walking ones: DONE
2. Address test, own address: DONE
3. Moving inversions, ones & zeros: DONE
4. Moving inversions, 8 bit pattern: DONE
5. Moving inversions, 32 bit pattern: DONE
6. Moving inversions, random pattern
7. Block move, 80 moves
8. Random number sequence
9. Modulo 20, Random pattern
10. Bit fade test, **90 min**, 2 patterns
HLFT: work done

- Checked flashing & boot procedure
  - from Alessandro & Tomasz
  - Correction of bugs with DDR configuration.
  - Strange behavior of flashing tool.
- Scripts to check ARM peripherals
- Improve g45memtest
PTS open issues

In the HLFT framework:

- Should we prefer USB to JTAG to load the first test environment? And what to do if one stop working?
- What to do if ETH does not work?
- Impossible to test FPGA if EBI0 is badly sold?

HL functional test is very flexible but, impossible to test anything if ARM does not work?

Does the FPGA & ARM need to be tested independently?

DDR test should be extensive from the begin (Maybe 3 hours)?
How to test components like PLL, DAC, VXCO?

- Oscilloscope (more precise but manual)
- Functional testing: group of components that might produce specific result with some parameters. If test fail, each component should be tested using oscilloscope.
- Specific designed equipment test

Fault detection & element localization & possible cause vs. test complexity trade-off

- Probably an affordable solutions with reasonable covertures requires solutions/test done at different levels of complexity.
PTS is a key element in order to get a high quality – dependable systems towards a stable commercial product.

A lot of work already done but we still have many open questions:

- HL vs LL functional tests
- Development of test equipment
- Test of stressed environmental conditions

→ questions to be answer here?
Thank you for your attention