White Rabbit Node

Technical Specification, Slim Version

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Contents

Revision History Table

Version	Date	Authors	Description
0.1	26/10/2010	T.F, C.P	First Draft
0.2	26/10/2010	T.F, C.P	Upgrade of the document after CERN meetings(date)

Acronyms List

WR	:	White Rabbit
WRP	:	White Rabbit Protocol
WRPTP	:	White Rabbit PTP
HP	:	High Priority. Used to indicate special WR Ethernet Frames
SP	:	Standard Priority. Used to indicate special WR Ethernet Frames
WRN	:	White Rabbit Node
WRN	:	White Rabbit Node Board
WRS	:	White Rabbit Switch
WRCM	:	White Rabbit General Clock Master Node
WRMM	:	White Rabbit Management Master Node
WRDM	:	White Rabbit Data Master Node
FESA	:	Front-End Software Architecture
NIC	:	Network Interface Card
SNMP	:	Simple Network Management Protocol
PTP	:	Precision Time Protocol
FMC	:	FPGA Mezzanine Card
FPGA	:	Field Programmable Gate Array
FEC	:	Forward Error Correction
UDP	:	User Datagram Protocol
LCD	:	Liquid Crystal Display
LED	:	Light-Emitting Diode
IRQ	:	Interrupt Request
SFP	:	Small Form-factor Pluggable transceiver

- **"Shall"**, which is equivalent to "is required to", is used to indicate mandatory requirements, strictly to be followed in order to conform to the standard and from which no deviation is permitted.
- **"Recommended"** is used to indicate flexibility of choice with a strong preference alternative.
- **"Must"** indicates an unavoidable situation.
- **"Should"**, which is equivalent to "is recommended that", is used to indicate:
  - Among several possibilities, one is recommended as particularly suitable, without mentioning or excluding others
  - That a certain course of action is preferred but not required.
  - That (in the negative form) a certain course of action is deprecated but not prohibited.
- **"May"**, which is equivalent to "is permitted", is used to indicate a course of action permissible within the limits of the standard.
- **"Can"**, which is equivalent to "is able to", is used to indicate possibility and capability, whether material or physical.

1. Introduction

White Rabbit is intended to be the next generation of deterministic network based on synchronous Ethernet, allowing for low-latency deterministic packet routing/forwarding and transparent, high precision timing transmission.

The receiver within White Rabbit, the so-called White Rabbit Node, is a device capable to accomplish what applies for a node in the "White Rabbit Node Functional Specifications" [WRS] document. Besides and specific only for the nodes, according to the White Rabbit Node Functional Specification [WRFNS], there are special different roles that a node may carry out:

- A White Rabbit General Clock Master Node (WRCM) shall provide time and frequency reference.
- A White Rabbit Management Master Node (WRMM) shall cover all network related function together with functionality to monitor and configure all White Rabbit Nodes.
- A White Rabbit Data Master Node (WRDM) should be used whenever control information has to be created centrally and fanning-out to all other nodes is mandatory like in the use case for particle accelerator control.

The very same hardware shall be configurable in order to perform any of these roles. This document does not cover scenarios where additional hardware is needed. For example the WRDM in the FAIR facility needs additional external hardware for processing the control data or aggregating interlock information.

On the one hand a WRN is a WR Network Device, on the other hand, it's a device that is intimately linked to the requirements of the use case. For that reason the aim of this document is to define a WRN generic and flexible enough to cover a wide range of scenarios.

In the current version of this document, the "Technical Specification, Slim Version", important information regarding detailed technical specification will be left aside, and it is focused on a top-down design.

2. White Rabbit Node Requirements

The White Rabbit Node shall provide hardware/software support to:

- White Rabbit
- Synchronous Ethernet
- PTP, IEEE 1588 v.2
- IEEE 802.1D and IEEE 802.1Q

Besides a WRN has to fulfil the requirements of different users of Time-Critical Control Systems that want to use White Rabbit. Thus, the White Rabbit Node has to be devised and designed according to the following guidelines:

- The White Rabbit Node Board shall provide a flexible and versatile design which may be adapted to a wide rage of applications.
- Interconnectivity. The WRN shall be designed either as standalone receiver, or as carrier within a crate.

3. White Rabbit Node Board

The WRNB shall provide the full functionality specified in [WRNFS]. Besides it shall provide the hardware support for all the functionalities expected from a control system receiver.

3.1 Hardware

- An FPGA contains the main WRN functionalities described in HDL language (Macro, to be defined). The Figure 4.1 shows the different modules of the so-called White Rabbit Core.
- Flash Memory (Size,to be defined)
- DDR SDRAM (Size, to be defined)

3.2 Form Factor

All WRNs shall come in one of the following form factors:

- PCI
- PCIe: This node shall follow the detailed hardware-specification of "PCIe FMC Carrier Functional Specifications".
- VME: This node shall follow the detailed hardware-specification of "VME FMC Carrier Functional Specifications and connectivity Diagram".
- PMC
- μTCA
- Standalone

3.3 Interfaces

The WRNB shall offer the following interfaces:

- SMC Coaxial connectors:
  - 125 MHz reference clock input. Used to provide external 125 MHz clock as a reference for downlink ports instead of clock recovered from uplinks.
  - 10 MHz reference clock input. Allows for using 10 MHz reference clock from rubidium/GPS.
  - PPS input.
  - PPS output.

- LEDs for information/debugging purposes.
- Power Supply
- At least one FMC socket (VITA 57 standard).
- At least one SFP module socket
- Lemo-00 connectors
- Configurable RS232
- JTAG interface

3.4 Power Supply

The powers supply shall follow the standard of the respective form factors for power supplies. In the case of a standalone WRN an external power supply shall be provided.

4. White Rabbit Node Core

The main elements and functionality of WR Node Board seats on an FPGA. The Figure 4.1shows the functional block diagram of the WRN.

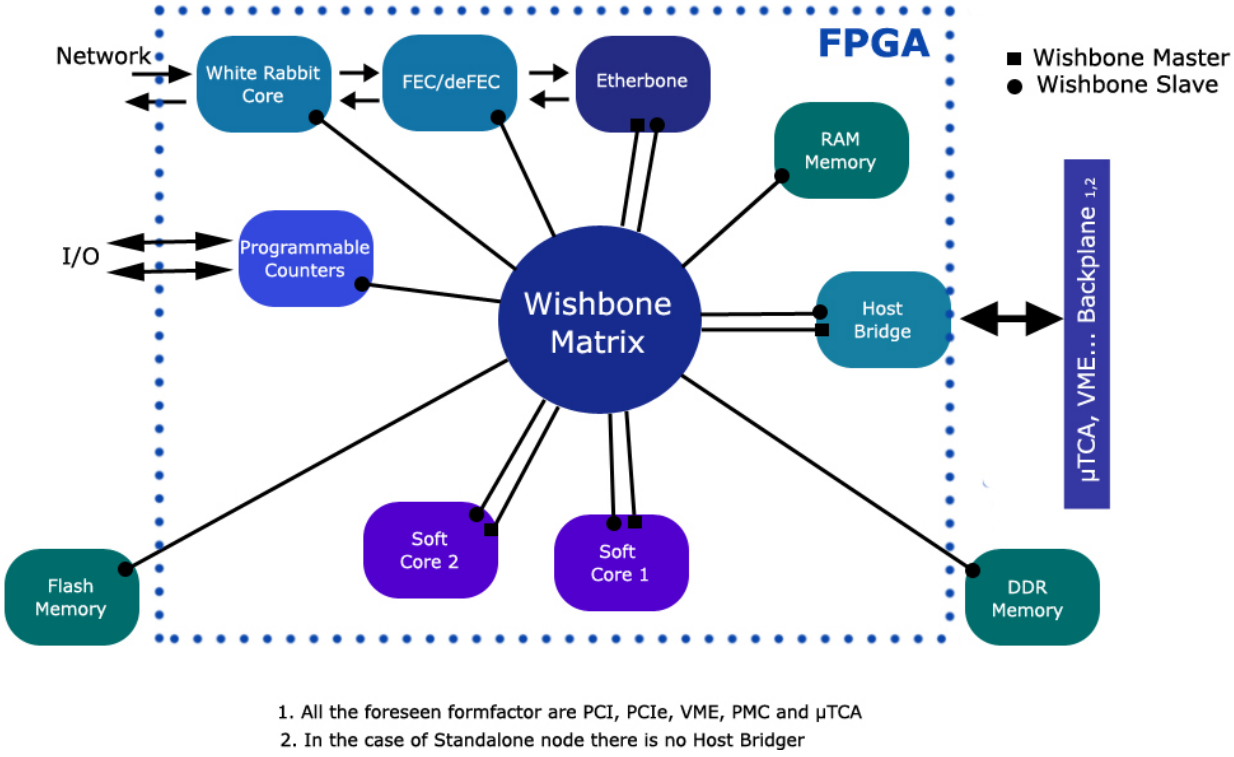

Figure 4.1: White Rabbit Node Block Diagram

We describe the functional blocks of the WRN in following chapters.

4.1 White Rabbit Core

The White Core will provide all the functionalities described in the White Rabbit Specification that applies for a node.

This functional block is made up of:

- Soft Core
  - WRP Protocol daemon and phase sync.
  - Handling of high-layer IEEE802.1x protocols
  - Configuration of WR features
- White Rabbit IP Core
  - MAC
  - miniNIC

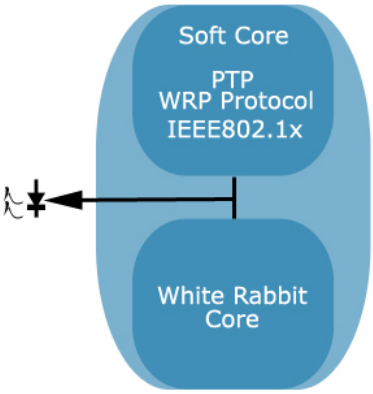

Figure 4.2: White Rabbit Core

4.2 Forward Error Correction

The FEC will encode the Data Control Information according to the FEC scheme propose in [WRR].

The Encoder/Decoder module shall:

- encode/decode codewords in range length of ???
- encode/decode the information with a minimum throughput of ???? / ?????

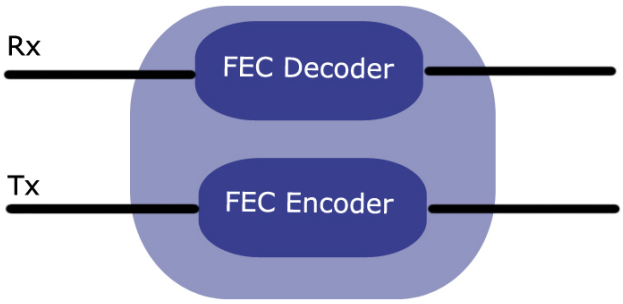

Figure 4.3: Forward Error Correction Block Diagram

4.3 Etherbone

Etherbone [ETHBONE] is an FPGA-core that connects Ethernet to internal on-chip wishbone buses permitting any core to talk to any other across Ethernet. By implementing Etherbone, the WR Node becomes an Etherbone Addressable Device (EAD) and this fact enables the possibility of reading/writing data to/from other WRN over Ethernet.

Etherbone is used by:

- the WRDM to write control data to the WRN Cores.
- the WRMM to write/read configuration information to/from other WRN Cores.
- the WRN to write/read data to other WRN Cores.

4.4 Host Bridge

The Host Bridge shall be designed for interfacing the WRN with other carriers in a crate. This module shall contain options to support the next buses:

- PCI
- PCIe
- VME
- μTCA [1]

4.5 Soft Cores

With the aim of providing flexibility to the WRN, Soft Cores shall be implemented in the FPGA. The purpose of such a Soft Cores is generic and it will depend on the use case. Also it depends on the role that the node performs, according to the [WRNFS]:

- **WR Data Master Node**
  The Soft Core 1 shall orchestrate the flow of control data. The Soft Core 2 shall gather statistics.
- **WR Management Node**
  It could be even only one Soft Core available for network management purposes.
- **WR Node** The Soft Core 1 shall orchestrate the flow of control data. The Soft Core 2 shall configure and supervise the Programmable Counter module.

The choice of a special Soft Core will depend on requirements of the Control System and the available area of the chosen FPGA. The alternative more attractive to the date are:

- LION 3
- xxx

Currently GSI is evaluating different open Soft Cores taking into account the FAIR facility and CERN requirements. Soon a document will be published with the result of this evaluation.

4.6 Programmable Counter

The module shall offer a number (to be defined) of programmable counters. They shall be clocked either by an internal clock ??? MHz (To be defined) or an external clock ??? MHz.

The configuration of the counters shall be provided either from the WRDM or the Host Bridge.The counter's output will be mapped to the physical interfaces described in previous chapters. These counters shall perform a set of possible actions upon receiving control event, like:

- Loading counters

[1] The electrical interfaces may include: PCI Express, Advanced Switching, Serial RapidIO, and Gigabit Ethernet.

- Trigger pulse productions
- Burst Interrupt
- Host Bridge IRQs

4.7 RAM Memory

? MB (to be defined) of embedded memory shall be used within the FPGA.

4.8 WishBone Matrix

As the figure 4.1 shows the modules of the WRN Core are interconnected by a matrix of Wishbone buses. Such a matrix shall provide parallel communication between wishbone master and slaves. All the modules shall be slaves, and only the next devices master as well:

- Etherbone
- Host Bridge
- Soft Cores

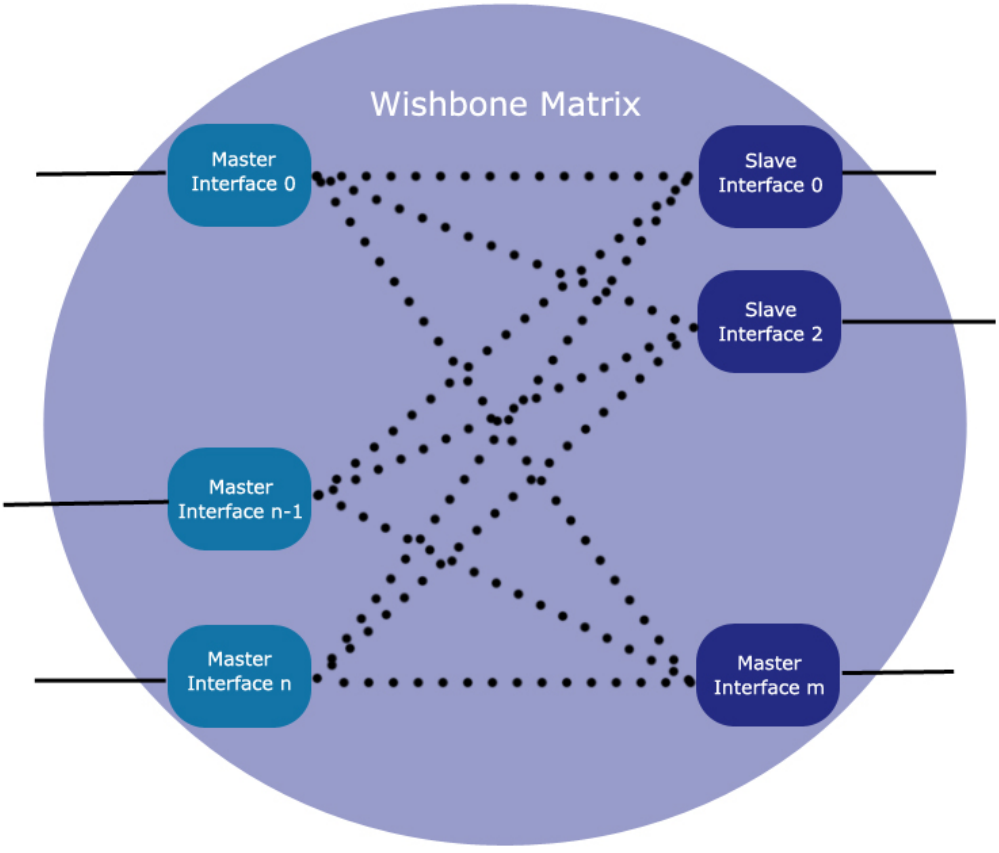

Figure 4.4: Wishbone Matrix

The matrix [2] shall provide interconnections of up to 8 masters and 16 slaves in order to provide scalability to the design. All the slaves interfaces shall implement a 4 level arbiter so as to select the master in case of multiple master access. If the masters have the same priority, the prioritization shall be based in a Round Robin algorithm. The arbiter shall provide 4 levels of priority, and shall be assigned as follows:

- Level 1 →Etherbone
- Level 2 →Soft Cores
- Level 3 →Host Bridge
- Level 4 →Free

The level 1 is the highest priority.

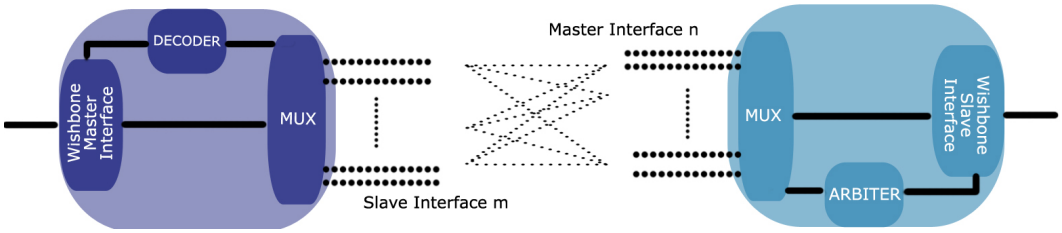

Figure 4.5: Wishbone Master and Slave Inteface

[2]This chapter has been inspired by the document [WBM]

Bibliography

[WRS] White Rabbit Specification.
http://www.ohwr.org/projects/white-rabbit

[1] White Rabbit Switch Technical Specification.
http://www.ohwr.org/projects/white-rabbit

[WRNS] White Rabbit Node Functional Specification
http://www.ohwr.org/projects/white-rabbit

[ETHBONE] Functional Specification Etherbone Core
http://www.ohwr.org/projects/white-rabbit

[WBM] Wishbone Interconnectect Matrix IP Core
http://www.opencores.org

[WRR] Robustness in White Rabbit
http://www.ohwr.org/projects/white-rabbit To be published

[CTR] The CTR User Guide
http://www.cern.ch