White Rabbit and the CERN BE-CO-HT standard hardware kit: an introduction

Javier Serrano
On behalf of the WR team
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Outline

- Introduction: the HW kit.
- White Rabbit.
- First ideas about collaboration with industry.
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Introduction: the **Controls HW Kit**

- Both VME and PCI/PCIe.
- Includes analog and digital I/O, field busses (incl. timing), stepping motor control and misc (pulse repeaters, adapters…).
- For each component, we (will) support:
  - Hardware: user manual, help in debugging…
  - Device driver with I/O emulation for Linux, with documentation. Comedi?
  - A test program on top of the driver, with documentation.
  - A library on top of the driver, with documentation and usage examples. We don’t support anyone bypassing this library.
  - A test program on top of the library, with documentation.
  - A test procedure.
  - An installation procedure.
  - A wiki with known issues and the level of support offered for a given module (if different from “complete support”).
  - Version management of all HW and SW above.
- All of the above are based on templates and standard procedures. This is of course important for maintainability.
Reasons to renew HW kit

- Standard hardware modules
  - Obsolescence problems
    - Some solutions are more than 30 years old → poor reliability.
    - Detailed knowledge has been lost: CAMAC, PSB matrix... → poor support.
  - Quality of support from some companies is poor.
  - New platforms: PCI/PCIe.

- Drivers
  - Reduced maintenance team.
    - Need to reduce maintenance costs by standardizing.
    - A standard approach for drivers/libraries and test programs is being defined.
    - Big upgrade operation needed after that, with help from industry and temporary labour.
  - New operating system (Linux) and new processor boards (KISS and A20).
Plans for renovation of HW modules

- Update of slides presented in the Renovation Workshop on December 3, 2008.
- Use the new FPGA Mezzanine Card (FMC) Vita 57 standard (more details later). Collaboration with CERN’s Beam Instrumentation group.
- Design/buy FMCs which can be placed on VME, PCI, PCIe... carriers. If possible use open hardware (more on the reasons later).
- Work is partitioned into work packages:
  - WP1: Analog input.
  - WP2: Analog output.
  - WP3: Digital I/O with interrupts.
  - WP4: timing and field busses.
  - WP5: stepping motor control.
  - WP6: misc developments, including carriers.
- Special work package (WP7) for the migration of legacy device drivers to the new front end platforms.
- The whole project should be over by the end of 2010.
FMC Vita 57 standard

- The FPGA Mezzanine Card (FMC) ANSI-VITA-57 provides a standardization for mezzanine cards and carriers.

- Typical carrier form factors are AMC, VME and PCI.

- Two connector types:
  - The Low Pin Count (LPC) connector provides 68 single-ended user-defined signals or 34 user-defined differential pairs, one Multi Gigabit pair, clocks, a JTAG interface, and an I2C interface to optionally support the base IPMI commands. All user signals should be routed to the same FPGA IO bank.
  - The High Pin Count (HPC) provides 160 single-ended user-defined signals or 80 user-defined differential pairs, 10 MGT pairs, and additional clocks.

- Two main advantages:
  - Cover 3 (or more) form factors very efficiently.
  - Improve our reaction time for new needs.
PCIe carrier (VME uses a similar concept)

1 Lane PCIe Slot

12V/3V3

PCIe 250MB/s

DC/DC

12V
2V5
VADJ (0-3V3)
3V3
1V8

FMC connectors

JTAG

ZBT SRAM 1
ZBT SRAM 2
SO DIMM module

Individual ID
PCB ID

Application (User) FPGA

Ethernet Phy + WR Mac

Conn1 6 diff IOs
Conn2 6 diff IOs

Flash Partition #0
Partition #1
...

Configuration Watchdog+
Monitoring

I2C

SFP socket

1V8

I2C

FPGA

Phy + WR
Mac

Phy+

1 Lane PCIe Slot
PCIe carrier preliminary layout
Introduction: the HW kit.

White Rabbit = synchronous Ethernet + PTP + WR protocol.

First ideas about collaboration with industry.
Reasons for White Rabbit

- New timing system at CERN/GSI with:
  - Higher bandwidth.
  - Bi-directional traffic, enabling:
    - Stand-alone receivers.
    - On-line compensation of cabling delays.

- New deterministic field bus for time-critical applications:
  - Open switch:
    - No black boxes in the way of time-critical data.
    - Complete determinism in hardware.
  - Supported by all FMC carriers.
Some potential applications of White Rabbit

- Timing Slave
- Distributed Scope
- Control loop
Synchronous Ethernet
Timing of a Gigabit Ethernet Link (1000Base-T)

- The Master PHY uses the internal 125 MHz clock generated from CLOCK_IN to transmit data on the 4 wire pairs.
- The Slave PHY uses the clock recovered from the opposite PHY as the transmit clock.
The Standard IEEE 1588
Determination of Delay and Offset

Delay $D = \frac{A + B}{2}$

Offset $O = \frac{A - B}{2}$

measured values $t_0, t_1, t_2, t_3$

$A = t_1 - t_0 = D + O$

$B = t_3 - t_2 = D - O$

$t_3 = t_2 - O + D$
White Rabbit Architecture

WR switches implement priority looking at Ethernet frame headers.
Switch design

- **WhiteRabbit switch MCH**
  - Uplink ports LC/E2K
  - Front panel
  - Backplane connector
  - IPMI-B
  - fabric A
  - TCLKA
  - fabric D
  - IPMI-A
  - Power supply/fan management

- **WhiteRabbit switch AMC**
  - Downlink ports LC/E2K
  - Front panel
  - Backplane connector
  - WR switch slave module FPGA
  - 1.25 Gbps Ethernet (LVDS)
  - 125 MHz switch reference clock, in-phase with master clock
  - 62.5/125 Mbps switch management sync. serial link (LVDS)

- **WhiteRabbit switch AMC**
  - Downlink ports twisted pair
  - Front panel
  - Backplane connector
  - WR switch slave module FPGA
  - AMC port 0/1
  - Fat Pipe 0

- **Other slave card**
  - Anything you like here :)
  - Front panel
  - Backplane connector
  - card mgmt.
  - Slave card Ethernet controller
  - Optional slave card timing

- **uTCA crate**
  - redundant PSU

- **cooling stuff**
WR Protocol

**OSI MODEL**

- Application
- Presentation
- Session
- Transport
- Network
- DataLink
- Physical

**White Rabbit Protocol**

- Not Specified
- PTP
- WRCMP
- White Rabbit MAC
- Synchronous Ethernet

Does things like WR device identification, enabling/disabling switch options, like PTP, etc.
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Advantages of **open design**

- **Peer review.**
  - Newsgroups/mailing lists.
  - Colleagues in other labs.
  - Industry!

- **Reuse.**
  - Take designs from other labs/companies.

- **Deal with commercial dependency problems, including cost issues.**

- **Make job easier for device driver developers.**

- **Give better support to our clients.**
Possible roles of companies

- **Companies as design partners:**
  - Pay a company to design for you, publishing the results.
  - Get specialized companies help you in areas where you are weak.

- **Companies as manufacturers and distributors:**
  - Decreases risk for customer, at the expense of price.
  - Get guarantee and support from company, i.e. go beyond simple manufacturing.
  - Go to another company if dissatisfied.

- **Big question: how to motivate companies?**
  - The WR switch is the first good candidate for this scheme.
  - Feedback from companies needed. Be creative!
Labs / Industry licensing schemes
(for hardware designed in labs)

- Traditional licensing
  - Company pays a license and gets somehow exclusive access to the technology.
  - Does not work for open designs.

- Open licenses.
  - Open Hardware License (OHL)
    - John Ackerman’s try at doing “GPL for HW”.
    - Tricky: protecting an expression of an idea is one thing, protecting the idea itself is another. Patents are typically used for this.
    - Private deal with company still possible to grant them the right not to publish results of modifications.
  - Non Commercial License (NCL).
    - Allows striking private deal with a company to allow it to do business with this design.
  - In any case: need for a collaboration agreement if design team is spread across many institutes/companies.
History of WR workshops

- **Workshop 1**
  - Held at CERN on 15 February 2008.
  - Exposed the problem and identified interested partners.

- **Workshop 2**
  - Demonstrated fiber length stabilization with Xilinx dev kits.

- **Workshop 3 (today)**
  - Track advancement in key work packages: switch development and network simulation.
  - Plan the immediate future.
Plan for the day

- Technical presentations and demo in the morning, with coffee break at 10:30.

- Lunch at 12:30 (in the glassbox for those of you on a visit).

- Technical brainstorming starting at 14:00 until the 15:30 coffee break.

- Non-technical brainstorming in the late afternoon.