

FIDU1  
Fiducial  
Mark  
FIDUCIAL

FIDU2  
Fiducial  
Mark  
FIDUCIAL

PanelIO  
PanelIO.Sch

VMPE1  
VMPE1.Sch

Fpga1  
Fpga1.Sch

|                |                 |
|----------------|-----------------|
| LCLK           | PCIBR#          |
| PCIBB#         | PCIDACK0#       |
| PCIBDP#        | PCIDACK1#       |
| PCIBG#         | PCUSERo         |
| PCIB#          | PCLINTo#        |
| PCIWAIT#       | PCIRETRY#       |
| PCIBURST#      | ETHIRQ          |
| PCICCS#        | LIT#            |
| PCIDP[0..3]    | vmeAS1*         |
| PCIDREQ0#      | vmeLWORDI*      |
| PCIDREQ1#      | vmeDTACKI*      |
| PCILINT#       | vmeWRITEI*      |
| PCILRESET#     | vmeDS1*0        |
| PCIMDREQ#      | vmeDS1*1        |
| PCIMEREQ#      | vmeBGOUT*[0..3] |
| PCUSERI        | vmeBCLRI*       |
| PCIRDWR#       | vmeBBSYI*       |
| PCITAF#        | vmeACFAIL*      |
| PCITEA#        | vmeACKIN*       |
| PCITSZ0#       | vmeRQI*[1..7]   |
| PCITSZ1#       | vmeBRI*[0..3]   |
| PCITS#         | vmeBERRI*       |
| LA[00..31]     | vmeSYSFAIL*     |
| LD[00..31]     | nGA[0..5]       |
| WE#            | vmeRETRYI*      |
| ETH#           | nEVGIF          |
| BE0#           | nEVRI#          |
| BE1#           | nIFHANDLE       |
| BE2#           | nURD            |
| BE3#           | nUWR            |
| RE#            | nUCS            |
| VMEMSTR        | ULE             |
| vmeASO*        | UA[0..16]       |
| vmeWRITEO*     |                 |
| vmeDTACKO*     |                 |
| vmeLWORDO*     |                 |
| DTACKEN        |                 |
| ADIR           |                 |
| nAOE           |                 |
| ACLKAB         |                 |
| ACLKBA         |                 |
| ALE            |                 |
| vmeAM[0..5]    |                 |
| vmeDSO*0       |                 |
| vmeDSO*1       |                 |
| nAMOE          |                 |
| AMDIR          |                 |
| AMCLKAB        |                 |
| AMLE           |                 |
| AMCLKBA        |                 |
| vmeACK*        |                 |
| nDCHENA        |                 |
| vmeBGIN*[0..3] |                 |
| nDOE           |                 |
| DDIR           |                 |
| DCLKAB         |                 |
| DLE            |                 |
| DCLKBA         |                 |
| vmeBBSYEN      |                 |
| vmeBCLREN      |                 |
| vmeLACKOUT*    |                 |
| nSYSCON        |                 |
| vmeSYSFAILO*   |                 |
| vmeBERRO*      |                 |
| SYSRESETO*     |                 |
| vmeBRO*[0..3]  |                 |
| vmeIROO*[1..7] |                 |
| SQ2A[0..18]    |                 |
| SQ1A[0..18]    |                 |
| SQ1WE*         |                 |
| SQ1OE*         |                 |
| SQ2OE*         |                 |
| SQ2WE*         |                 |
| SQ2CSA*        |                 |
| SQ2CSB*        |                 |
| SQ1CSB*        |                 |
| SQ1CSA*        |                 |
| SQ1D[0..7]     |                 |
| SQ2D[0..7]     |                 |
| DRD[0..31]     |                 |
| DRA[0..12]     |                 |
| DRCKE          |                 |
| DRCLK          |                 |
| DQM[0..3]      |                 |
| DRCS*          |                 |
| DRRAS*         |                 |
| DRCAS*         |                 |
| DRWE*          |                 |
| DRBA0          |                 |
| DRBA1          |                 |

Power  
Power.Sch

MGT  
MGT.Sch

virtexconf  
virtexconf.Sch

VMPE2  
VMPE2.Sch

Transceivers  
Transceivers.Sch

Ethernet  
Ethernet.Sch

Fpga2  
Fpga2.Sch

|                |            |
|----------------|------------|
| SQ2A[0..18]    | DIN        |
| SQ2OE*         | TxFaultB   |
| SQ2WE*         | RxLOS      |
| SQ2CSA*        | RxLOLB     |
| SQ2CSB*        | RxLOS      |
| SQ2D[0..7]     | BREFCLK2P  |
| IO[0..31]      | BREFCLK2N  |
| IOLE           | TxFault    |
| IOCLKAB        | RxLOS      |
| IODIR[0..3]    | RxSD       |
| nIOOE          | DLY[0..10] |
| IOCLKBA        | LENDTX     |
| nINIT          | LENRFOUT   |
| MOD_DEFB[0..2] | RXRECCLK   |
| TxDisableB     | LENRECCLK  |
| RXSCKB         | DTXFB      |
| RXSDAB         | DRFB       |
| MOD_DEF[0..2]  | RXRECFB    |
| TxDisable      | RXRECFB    |
| BREFCLKP       | RXRECN     |
| BREFCLKN       | CGCS       |
| CGLOCK         | CGDI       |
|                | CGSK       |

HotSwap  
HotSwap.Sch

|        |  |
|--------|--|
| LIT*   |  |
| nRESET |  |

Memory  
Memory.Sch

|             |  |
|-------------|--|
| SQ2A[0..18] |  |
| SQ1A[0..18] |  |
| SQ1WE*      |  |
| SQ1OE*      |  |
| SQ2OE*      |  |
| SQ2WE*      |  |
| SQ2CSA*     |  |
| SQ2CSB*     |  |
| SQ1CSB*     |  |
| SQ1CSA*     |  |
| SQ1D[0..7]  |  |
| SQ2D[0..7]  |  |
| DRD[0..31]  |  |
| DRA[0..12]  |  |
| DRCKE       |  |
| DRCLK       |  |
| DQM[0..3]   |  |
| DRCS*       |  |
| DRRAS*      |  |
| DRCAS*      |  |
| DRWE*       |  |
| DRBA0       |  |
| DRBA1       |  |

|       |          |
|-------|----------|
| RXD1P | TXD2P    |
| RXD1N | TXD2N    |
| RXD2N | RFRECLKN |
| RXD2P | RFRECLKP |

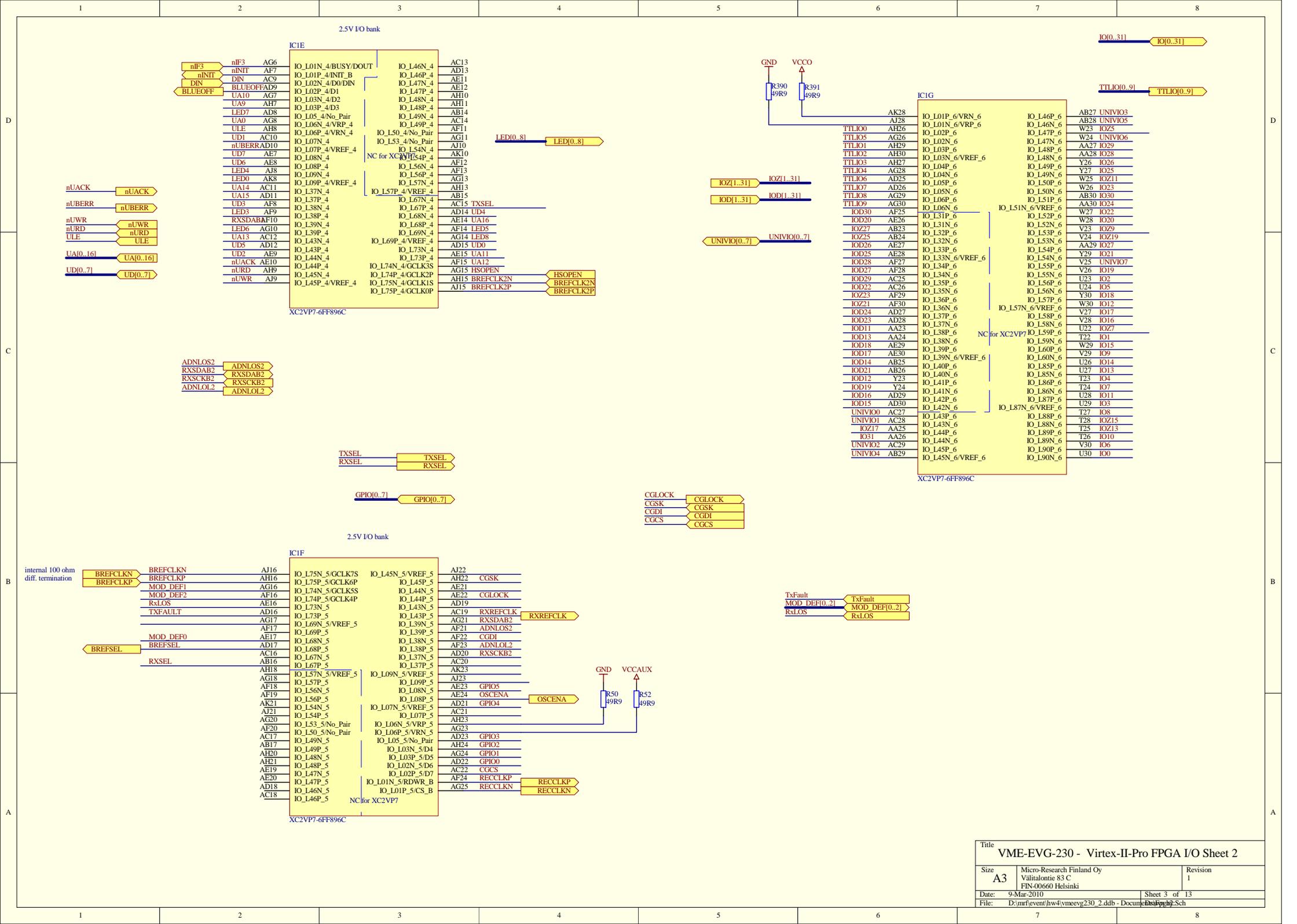
|          |               |
|----------|---------------|
| nINIT    | nURD          |
| nUIRQ    | nUWR          |
| TDO_PCI  | DIN           |
| UD[0..7] | TDI_PCI       |
| nRESET   | TCK           |
|          | TMS           |
|          | nTRST         |
|          | nUCS          |
|          | ULE           |
|          | UA[0..16]     |
|          | vmeSYSRESETO* |
|          | SYSRESETO*    |
|          | nURESET       |

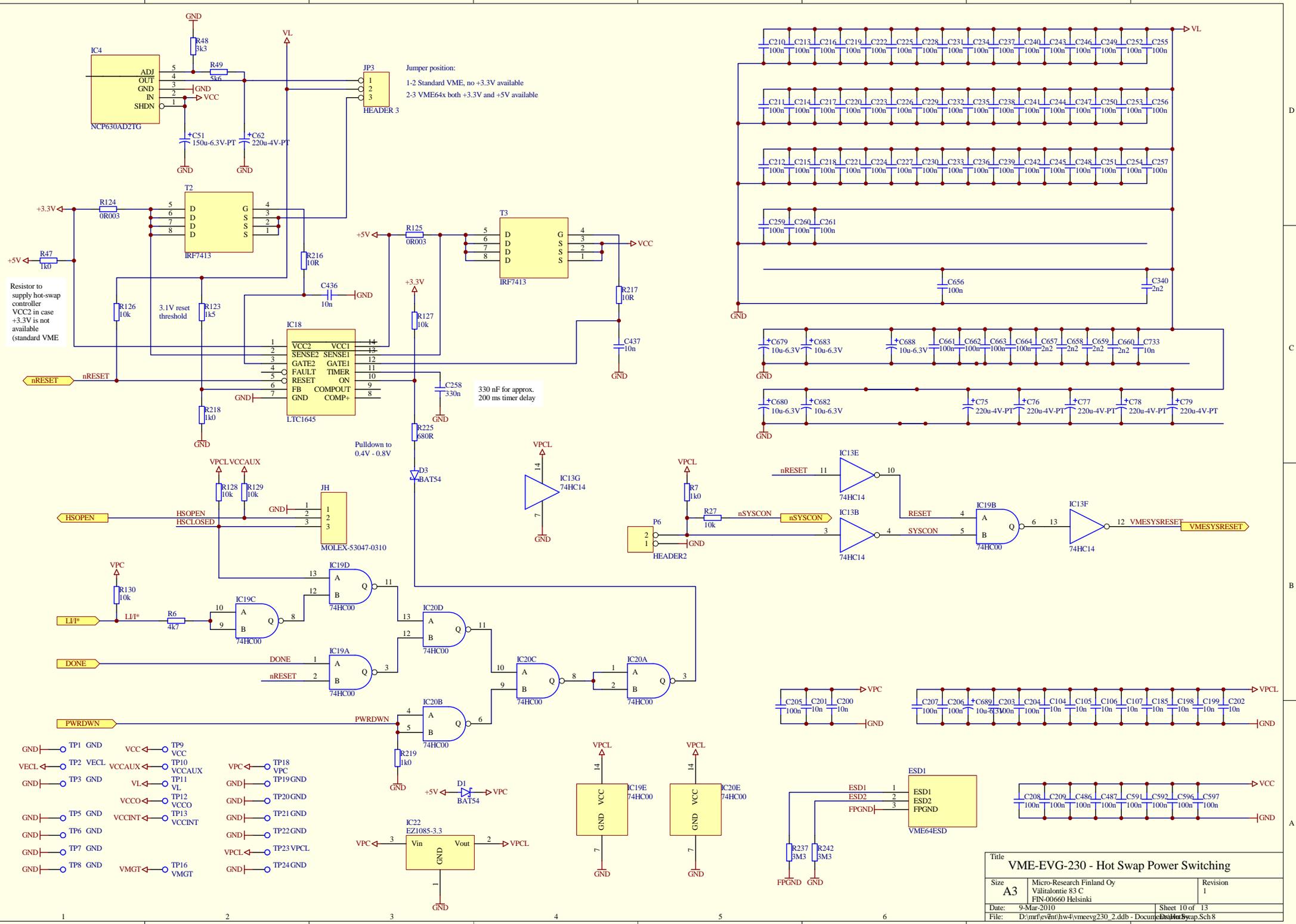
|             |            |
|-------------|------------|
| RETRYEN     | vmeRETRYI* |
| vmeRETRYO*  | nEVGIF     |
| LA[00..31]  | nEVRI#     |
| ADIR        | nIFHANDLE  |
| nAOE        | nPEVGI#    |
| ACLKAB      | nPEVRI#    |
| ACLKBA      | nPIFHANDLE |
| ALE         |            |
| LD[00..31]  |            |
| nDOE        |            |
| DDIR        |            |
| DCLKAB      |            |
| DLE         |            |
| DCLKBA      |            |
| PMCI[0..31] |            |
| IO[0..31]   |            |
| IOLE        |            |
| IODIR[0..3] |            |
| nIOOE       |            |
| IOCLKBA     |            |
| PWRONIF     |            |

|               |           |
|---------------|-----------|
| MOD_DEF[0..2] | TxDisable |
| TxFault       | TXD1N     |
| RxLOS         | TXD1P     |
| RXD1P         | TXD2P     |
| RXD1N         | TXD2N     |
| RXD2N         | TXD3P     |
| RXD2P         | TXD3N     |

|            |         |
|------------|---------|
| ETHCLK     | ETHINT# |
| GNT1#      | REQ1#   |
| C/BE0#     | RST#    |
| C/BE1#     |         |
| C/BE2#     |         |
| C/BE3#     |         |
| DEVSEL#    |         |
| FRAME#     |         |
| IRDY#      |         |
| PAR        |         |
| PERR#      |         |
| SERR#      |         |
| STOP#      |         |
| TRDY#      |         |
| AD[10..31] |         |
| AD0[0..9]  |         |







Jumper position:  
 1-2 Standard VME, no +3.3V available  
 2-3 VME64x both +3.3V and +5V available

Resistor to supply hot-swap controller VCC2 in case +3.3V is not available (standard VME)

330 nF for approx. 200 ms timer delay

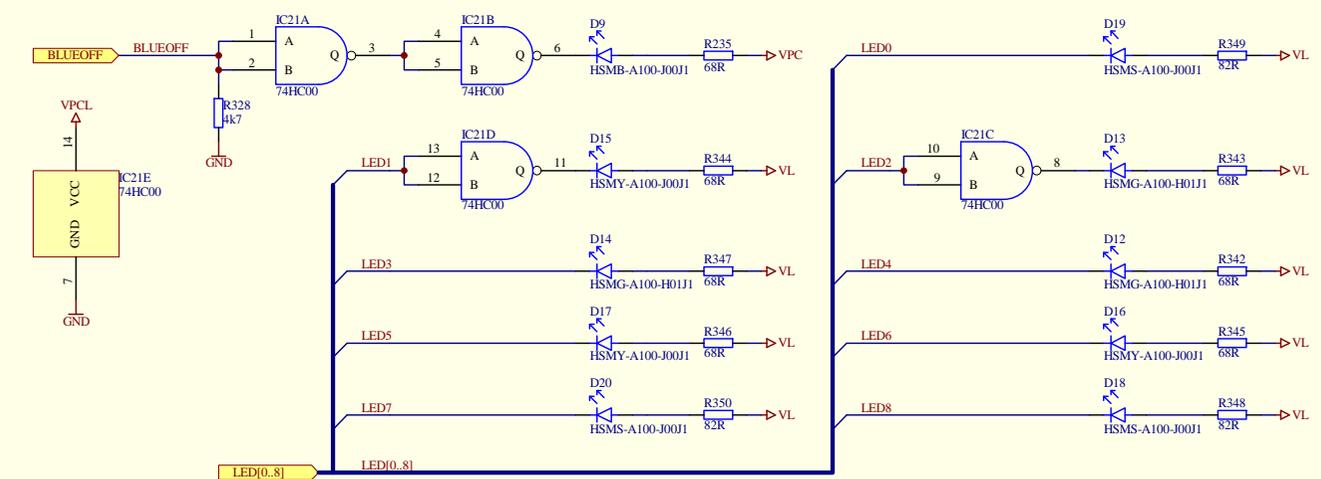
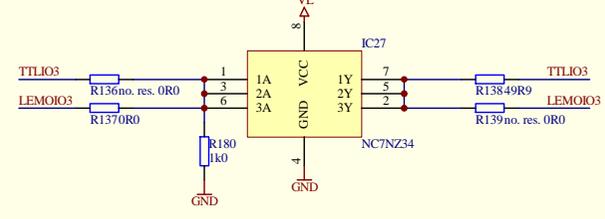
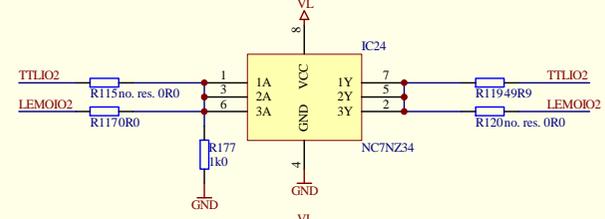
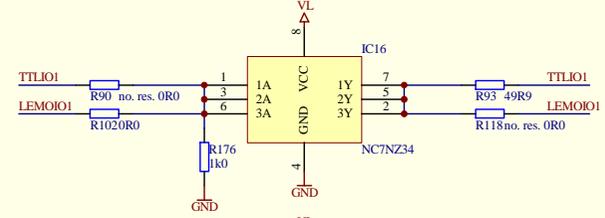
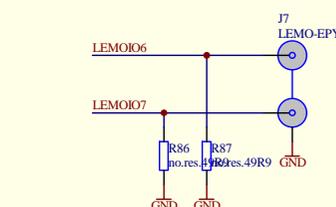
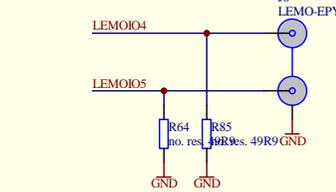
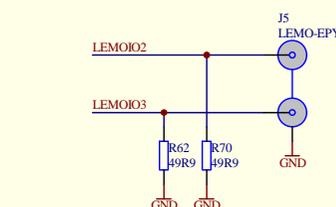
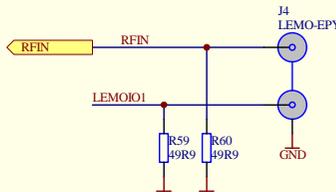
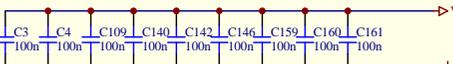
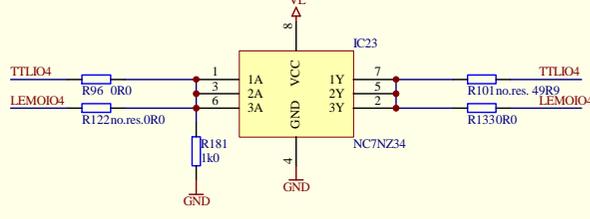
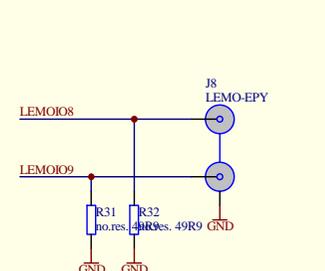
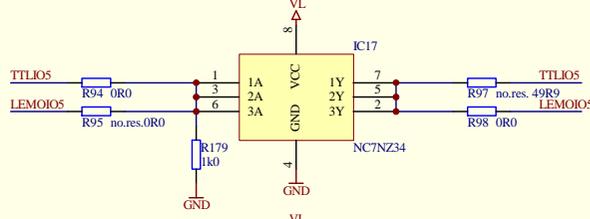
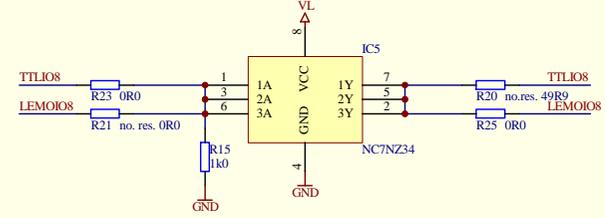
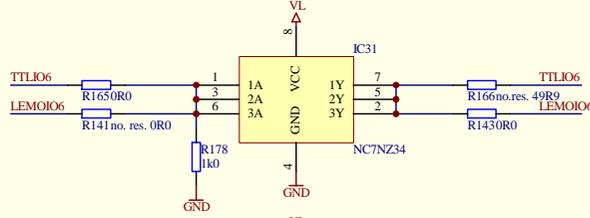
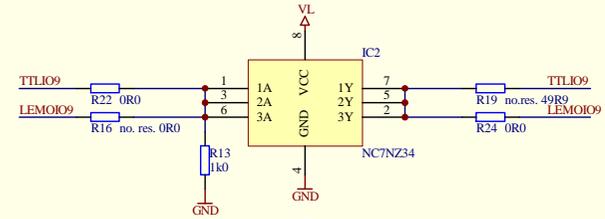
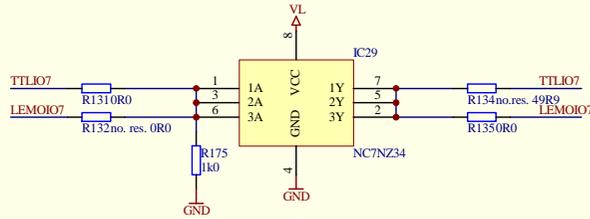
Pulldown to 0.4V - 0.8V

- GND TP1 GND
- VECL TP2 VECL
- GND TP3 GND
- GND TP5 GND
- GND TP6 GND
- GND TP7 GND
- GND TP8 GND
- VCC TP9 VCC
- VCCAUX TP10 VCCAUX
- VL TP11 VL
- VCCO TP12 VCCO
- VCCINT TP13 VCCINT
- VPGND TP14 VPGND
- VMGT TP16 VMGT
- VPC TP18 VPC
- GND TP19 GND
- GND TP20 GND
- GND TP21 GND
- GND TP22 GND
- VPCL TP23 VPCL
- GND TP24 GND

|  |   |               |
|--|---|---------------|
| Title<br><b>VME-EVG-230 - Hot Swap Power Switching</b> |   |               |
| Size<br><b>A3</b>                                      | Micro-Research Finland Oy<br>Valittontie 83 C<br>FIN-00660 Helsinki | Revision<br>1 |
| Date:<br>9-Mar-2010                                    | Sheet 10 of 13  |               |
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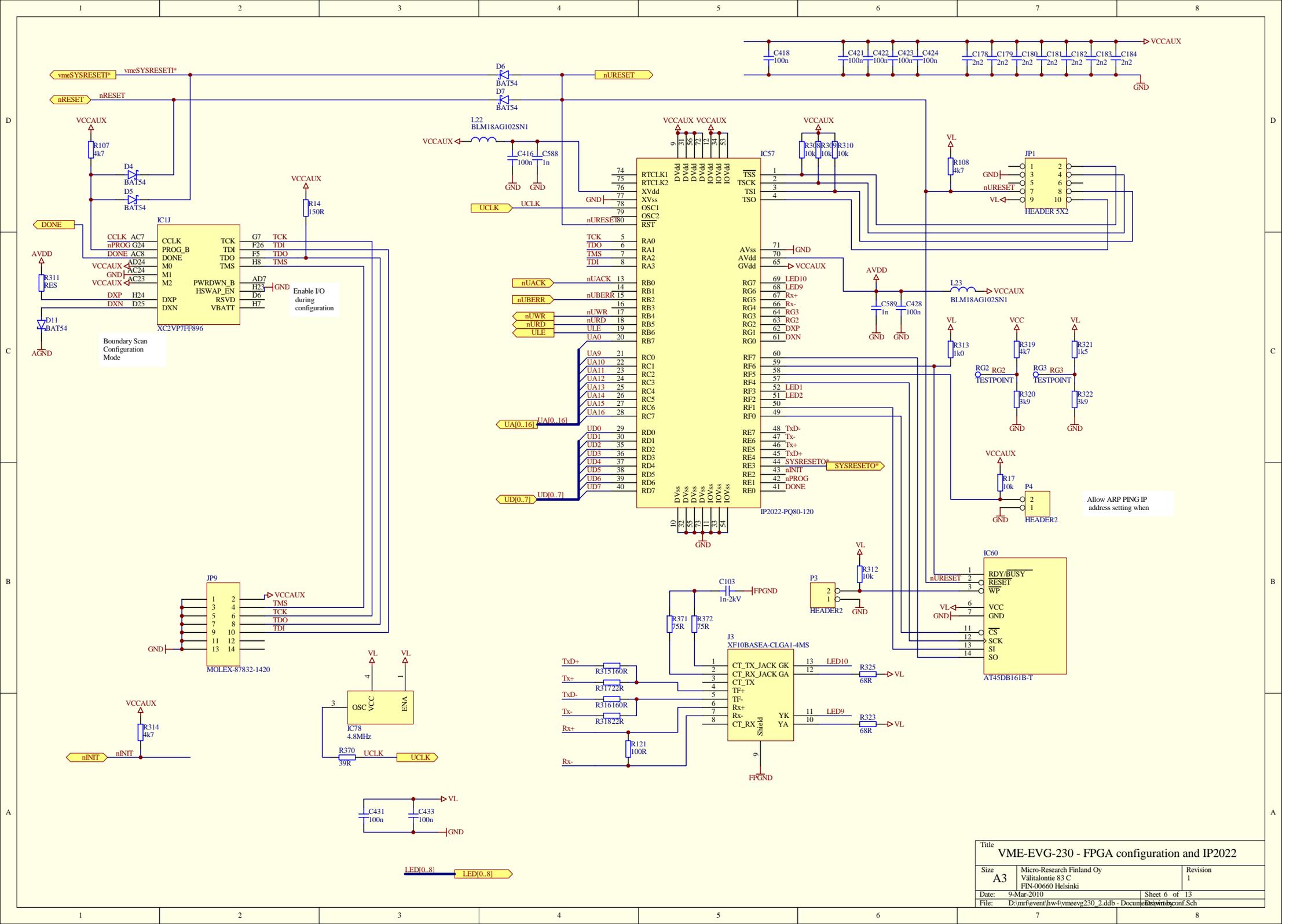
TTLIO[0..9]

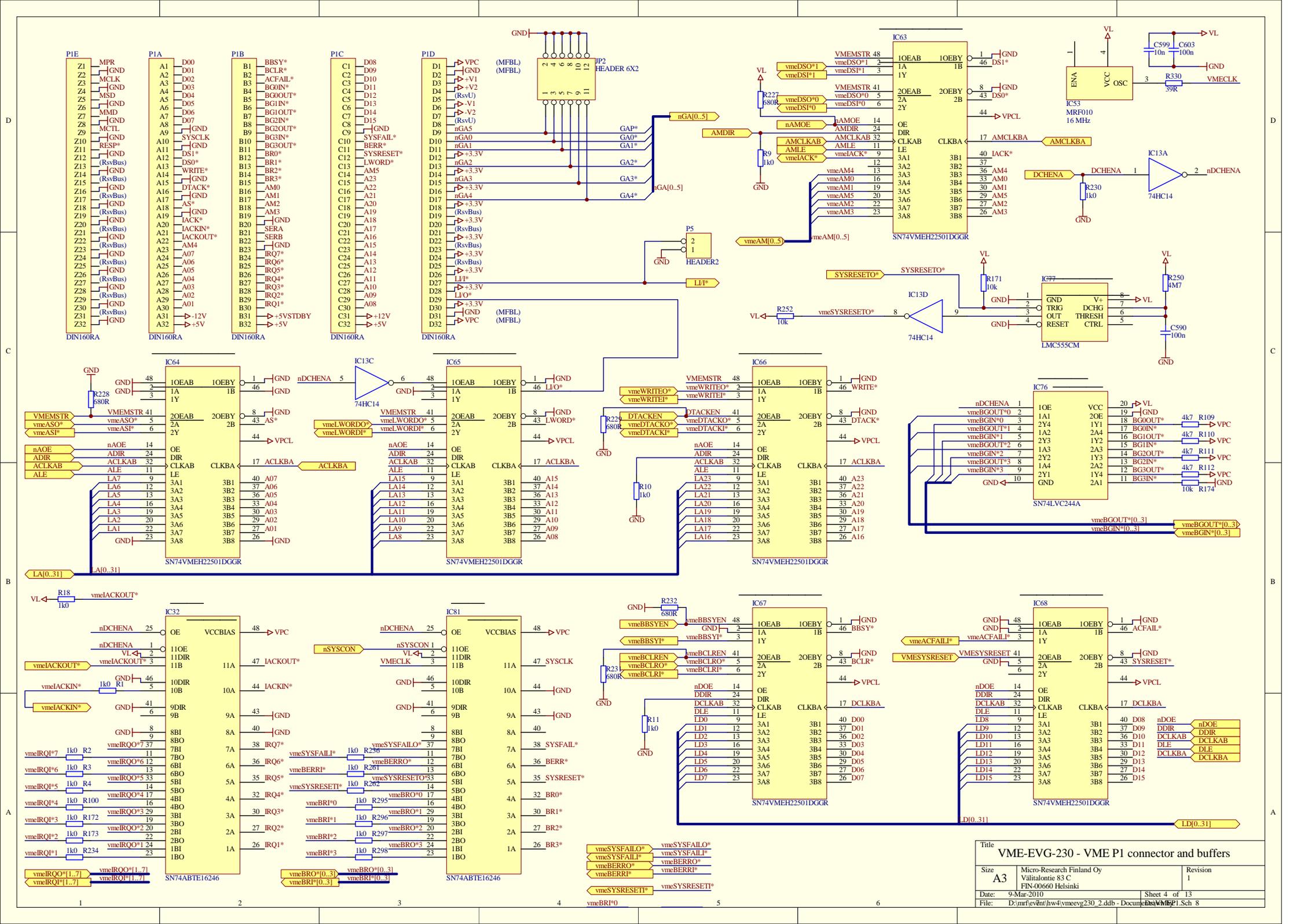


- LP1 LPIPE-1270.1010
- LP2 LPIPE-1270.1010
- LP3 LPIPE-1270.1010
- LP4 LPIPE-1270.1010
- LP5 LPIPE-1270.1010

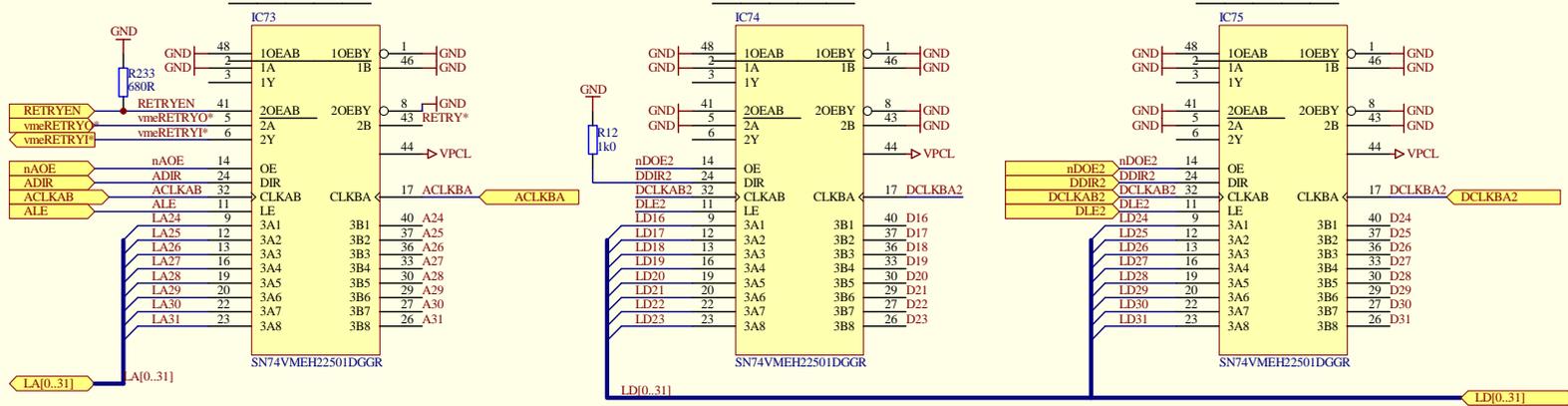
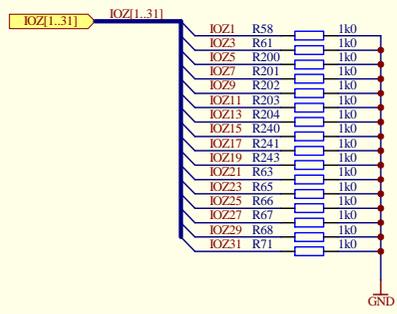
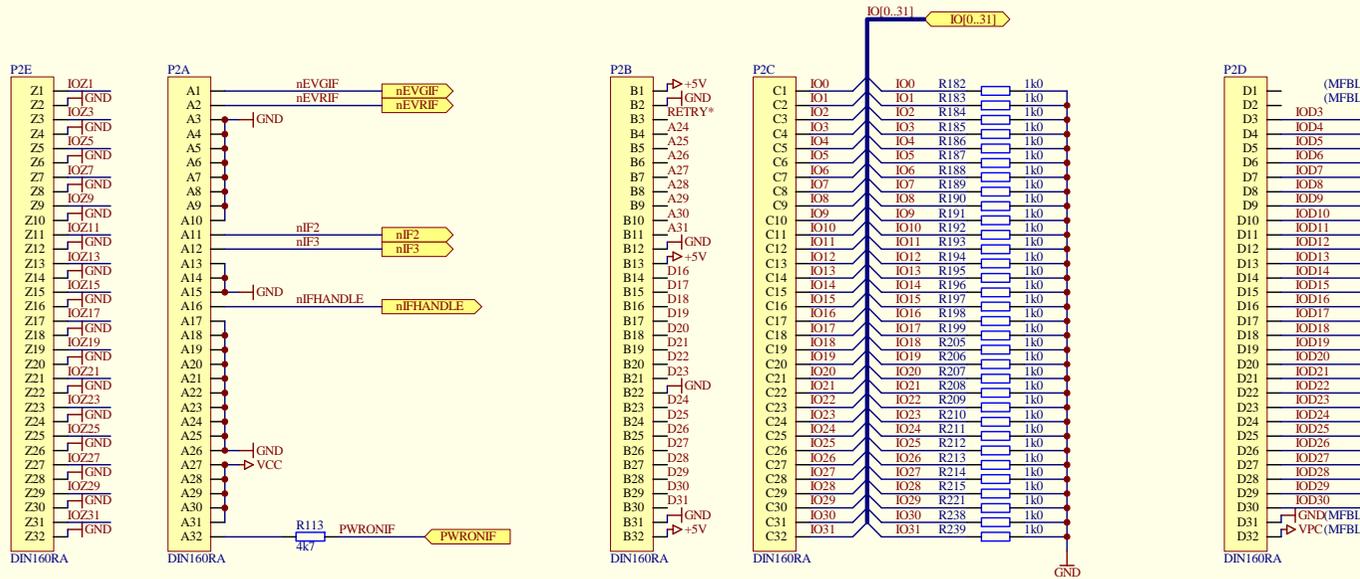
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|---|--|---------------|
| Title<br>VME-EVG-230 - Front Panel I/O and Leds |  |               |
| Size<br>A3                                      | Micro-Research Finland Oy<br>Valitalontie 83 C<br>FIN-00660 Helsinki | Revision<br>1 |
| Date:<br>9-Mar-2010                             | Sheet<br>9 of 13   |               |
| File:<br>D:\mr\event\hw4\vmeevg230_2.ddb - Docu |  |               |



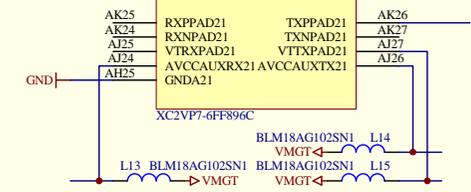
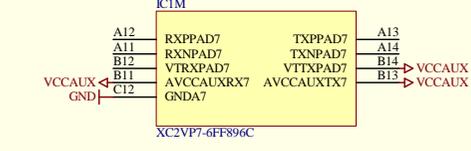
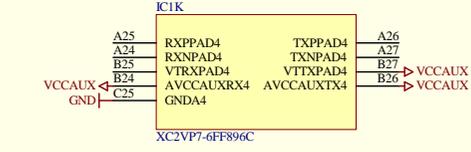
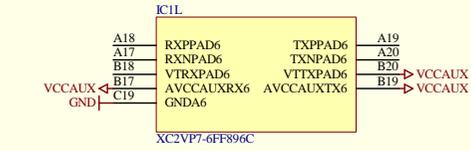
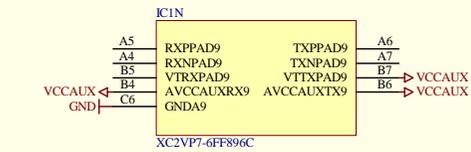
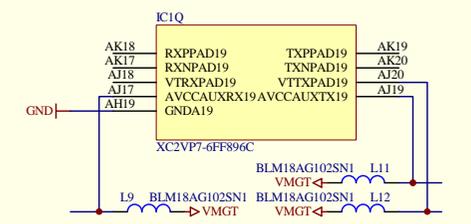
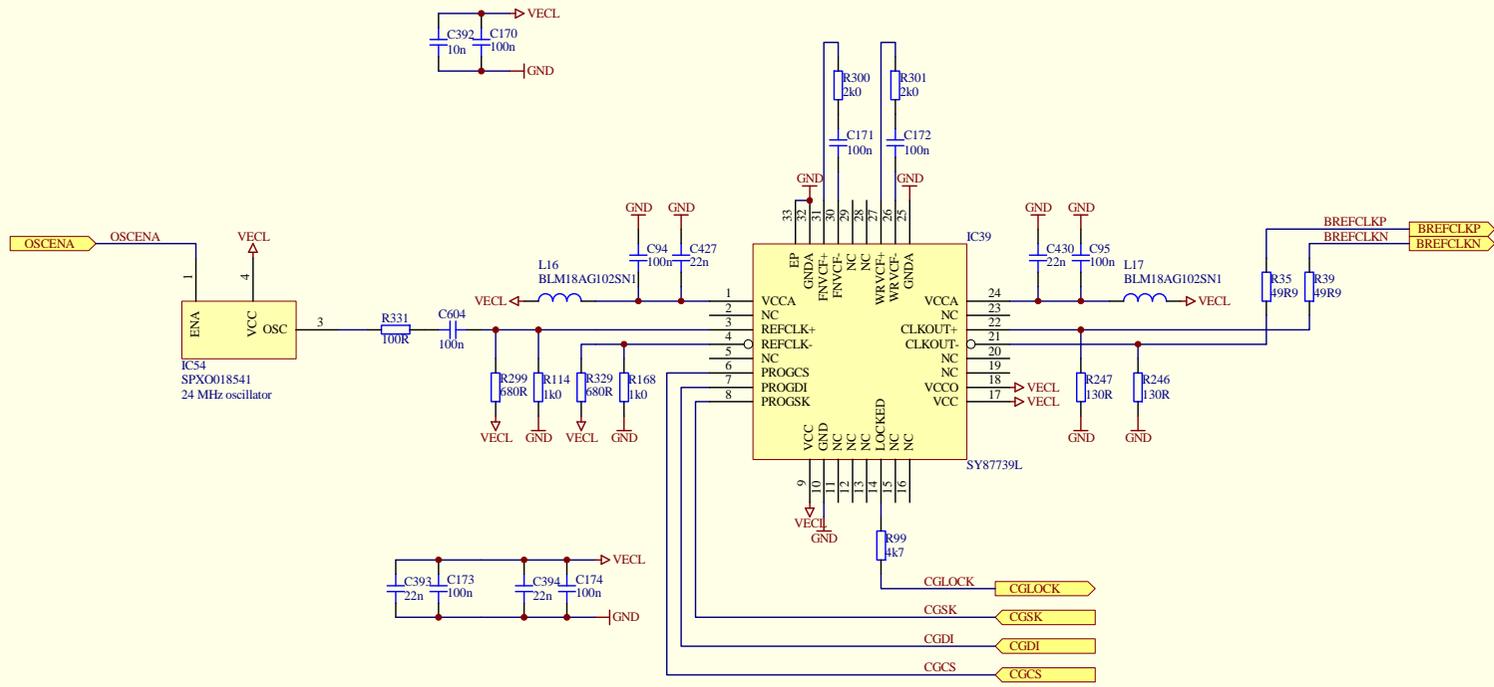




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|--|---|---------------|
| Title<br><b>VME-EVG-230 - VME P1 connector and buffers</b> |   |               |
| Size<br><b>A3</b>  | Micro-Research Finland Oy<br>Valittontie 83 C<br>FIN-00660 Helsinki | Revision<br>1 |
| Date:<br>9-Mar-2010  | Sheet 4 of 13   |               |
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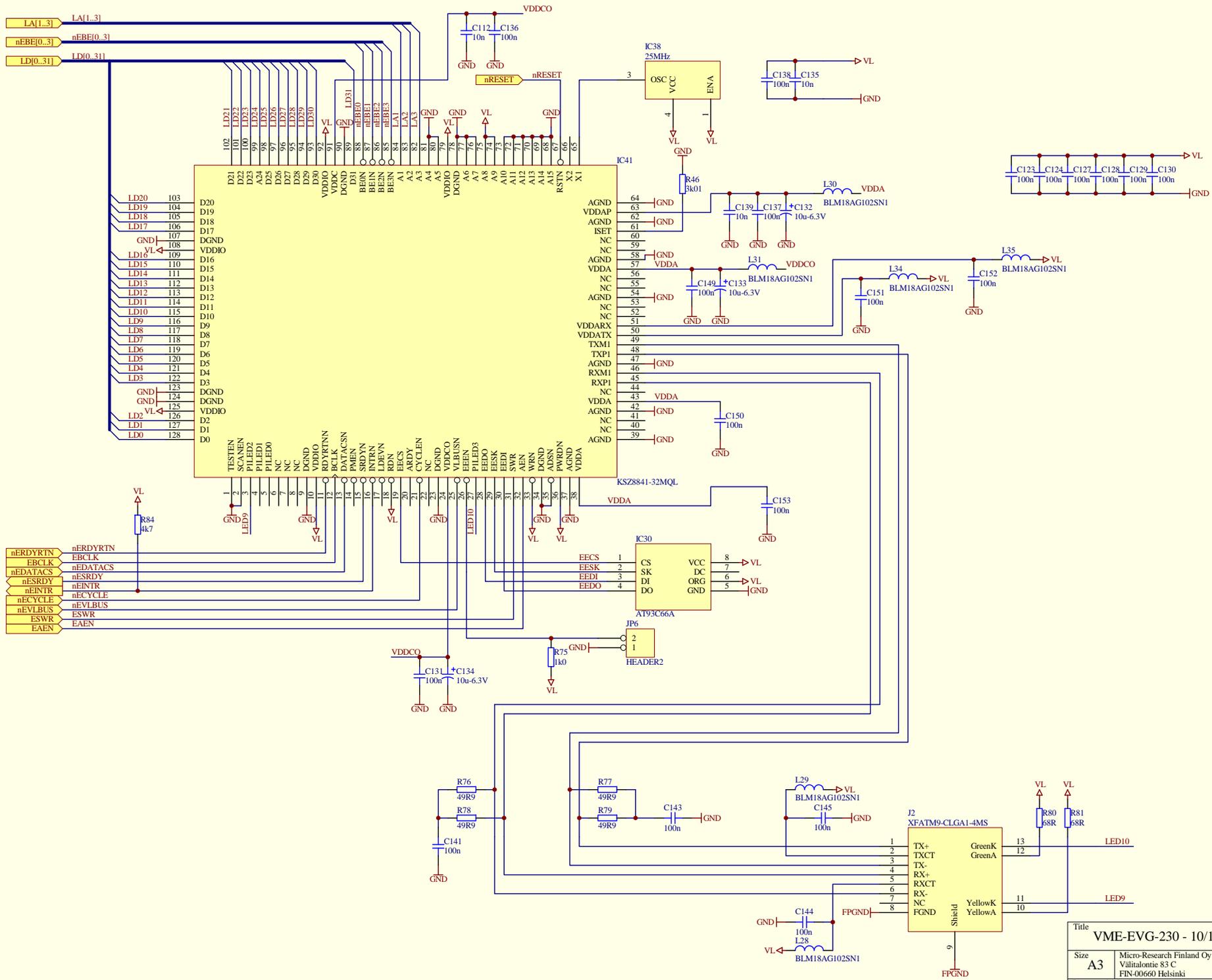


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|--|---|---------------|
| Title<br><b>VME-EVG-230 - VME P2 connector and buffers</b> |   |               |
| Size<br><b>A3</b>  | Micro-Research Finland Oy<br>Valittontie 83 C<br>FIN-00660 Helsinki | Revision<br>1 |
| Date:<br>9-Mar-2010  | Sheet 5 of 13   |               |
| File:<br>D:\mrf\ent\hw4\vmeevg230_2.ddb - Docu             | VME P2.Sch 8  |               |



|                                    |   |                |
|------------------------------------|---|----------------|
| Title<br><b>VME-EVG-230 - MGTs</b> |   |                |
| Size<br><b>A3</b>                  | Micro-Research Finland Oy<br>Valitalonie 83 C<br>FIN-00660 Helsinki | Revision<br>1  |
| Date:<br>9-Mar-2010                | File:<br>D:\mr\event\hw4\vmeevg230_2.ddb - Docu                     | Sheet 13 of 13 |





|  |   |               |
|--|---|---------------|
| Title<br><b>VME-EVG-230 - 10/100 MAC &amp; PHY</b> |   |               |
| Size<br><b>A3</b>                                  | Micro-Research Finland Oy<br>Valitalonie 83 C<br>FIN-00660 Helsinki | Revision<br>1 |
| Date:<br>9-Mar-2010                                | Sheet 7 of 13   |               |
| File:<br>D:\mr\evnt\hw4\vmeevg230_2.ddb - Docu     | Bldmet.Sch 8  |               |