FTRN PMC – Measurement of current consumption per voltage rail

Ljubljana, 12.05.2016

Goal

The goal of the measuremet was to determine current output on the voltage rails of the LTM4620 and LTM4619 DC-DC converters at different FPGA functions running and then estimate whether LTM4620 can be replaced with LTM4619.

Scope

To measure current consumption in regard to FPGA operation, FPGA gateware load was incrementally added by running following tasks:

- idle (after image load, no IO activity, no PCI activity, no USB activity, no fiber attached)
- WR fiber attached, locked
- 200MHz clock generation on all 5 Lemo IOs (60/40 duty cyle)
- PCI bus operation (running eb-info command in a loop)
- USB bus operation (running eb-info command in a loop)

Equipment used

Equipment part	**Manufacturer and model**	**Serial Number**
FTRN PMC	Cosylab, FTRN PMC RevA	89282
FTRN Pexaria	GSI, PE	
Multimeter	Agilent U1272A	MY50500002, HW-2011-003
Current Sense SMD resistor	VISHAY , WSL1206R0330FEA	N/A
PCI to PMC bus extender	AMFELTEC, SKU-013-01	A1301134

Preparations

Prior to each current measurement on the selected voltage rail, solder joint (see Appendix A) was replaced with current sense resistor and measuremet leads for the multimeter were soldered to the resistor.

Setup

PMC card was attached to the bus extender card and bus extender card was plugged into the PCI slot in the PC (see Appendix B). For WR connection Pexaria FTRN was used in the PCIe slot of the PC.

Results

Table shows maximum current consumption achieved where 1% current resistor tolerance is included and numbers for current are rounded up to mA value.

Regulator	**LTM4620**		**LTM4619**	
Voltage Rail [V]	2,5	1,1	3,3	1,15
Max Measured Current [A]	**0,282**	**0,723**	**0,664**	**0,075**
Max regulator Current [A]	13	13	4	4

% of the regulator maximum current	2,2	4,1	16,6	1,9

Table 1 : Mesured current on each voltage rail of the LTM4620 and LTM4619 power reglators.

Results of the measurement in Table 1 show that LTM4620 regulator output rails are loaded below 5% of its 13A rated current per rail and LTM4619 regulator output rails are loaded below 17% of its 4A rated current per rail.

Regulator	**LTM4619 (instead of 4620)**		**LTM4619**	
Voltage Rail [V]	2,5	1,1	3,3	1,15
Max Measured Current I_{max} [A]	**0,282**	**0,723**	**0,664**	**0,075**
% of LTM4619's maximum current	7,1	18,1	16,6	1,9
2*I_{max} [A]	0,564	1,446	1,328	0,15
% of the LTM4619 maximum current if 2*I_{max} is consumed	14,2	36,2	33,2	3,8
3*I_{max} [A]	3*0,282 =0,846	3*0,723 =2,169	3*0,664= 1,992	3*0,664=0, 225
% of the LTM4619 maximum current if 3*I_{max} is consumed	21,15	54,225	49,8	5,625

Table 2:Calculated percentage of the rated current per voltage rail for LTM4619

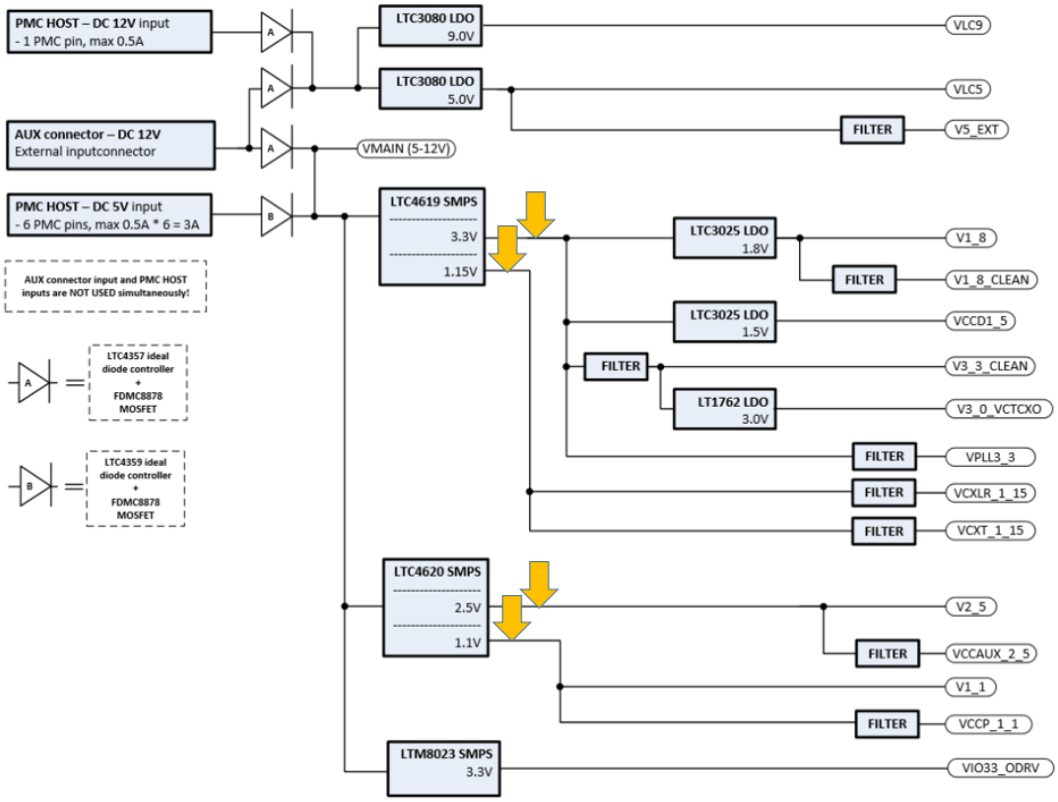
NOTE: Only the current consumption on rail 1.1V depends on FPGA logic utilization. Other rails are feeding periphery or IO banks and are thus not expected to increase by a factor of 2 or 3. But even in such case, LTM4619 capacity is enough.

Conclusion

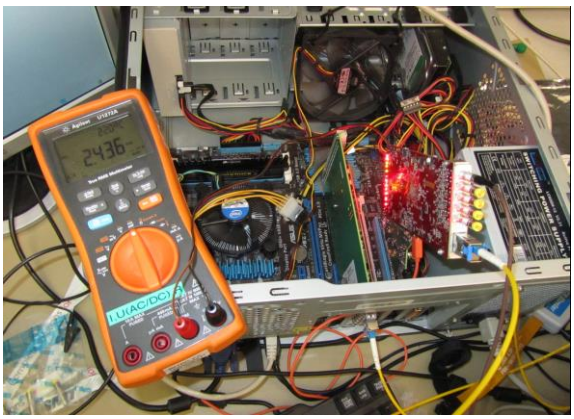
Given that FPGA gateware currently utilizes approximately 50% of the FPGA resources and even if we use 3x safety margin for future gateware features, the estimated 2,2A current on 1.1V rail (for FPGA core) can be provided by LTM4619 no problem (See Table 2).

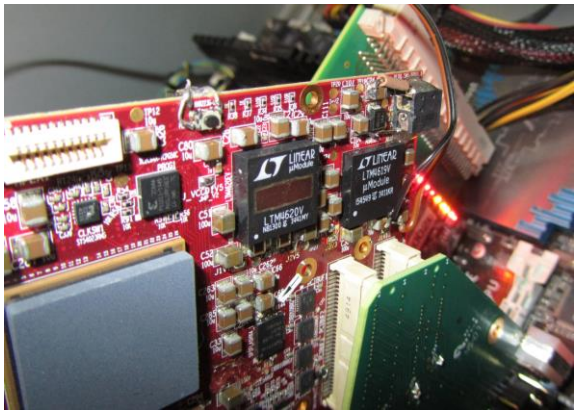
Therefore in terms of current requirement, LTM4619 can replace existing LTM4620 power regulator.

Appendix A: Measurement points



Appendix B: Measurement Setup





Appendix C Test Gateware

Project : pci_pmc

Platform : pmc

FPGA model : Arria V (5AGXMA3D4F27I3)

Build type : developer preview

Build date : Fri Apr 08 15:42:54 CEST 2016

Prepared by : Dusan Slavinec dusan.slavinec@cosylab.com

Perpared on : gsi-altera-SL64

OS version : Scientific Linux release 6.7 (Carbon), kernel 2.6.32-573.3.1.el6.x86_64

Quartus : Version 13.1.4 Build 182 03/12/2014 SJ Full Version

Appendix D: Fitter report

Fitter Status Successful - Tue Apr 12 14:53:56 2016

Quartus II 64-Bit Version 13.1.4 Build 182 03/12/2014 SJ Full Version

Revision Name pci_pmc

Top-level Entity Name pci_pmc

Family Arria V

Device 5AGXMA3D4F27I3

Timing Models Final

Logic utilization (in ALMs) 27,116 / 58,900 (46 %)

Total registers 31820

Total pins 201 / 378 (53 %)

Total virtual pins 0

Total block memory bits 3,189,832 / 10,762,240 (30 %)

Total DSP Blocks 6 / 396 (2 %)

Total HSSI RX PCSs 1 / 9 (11 %)

Total HSSI PMA RX Deserializers 1 / 9 (11 %)

Total HSSI TX PCSs 1 / 9 (11 %)

Total HSSI TX Channels 1 / 9 (11 %)

Total PLLs 3 / 19 (16 %)

Total DLLs 0 / 5 (0 %)