FAIR Timing Receiver (FTRN) PMC form factor - CSL_FTRN_PMC

SHEET	TITLE
1	TITLE PAGE
2	Block diagram
3	Power Tree
4	POWER DC-DC
5	POWER LDOs, FPGA BYPASS
6	FPGA configuration
7	FPGA user interface
8	WR clocking, system CLOCKS
9	PMC, SFP to FPGA
10	PMC host
11	IO to FPGA
12	IO blocks 1-3
13	IO blocks 4-5, IO clk

DATE	REVISION DESCRIPTION	DRAWN	REV
04.12.2014	Initial version	dslavinec	A
21.4.2015	Added fixes found during HDL synthesis check and changes during PCB layout	dslavinec, bpecnik	A
21.5.2015	PCB layout ready for review	dslavinec, bpecnik	A
19.9.2016	Page 04: - LTM4620 replaced with LTM4628 - LTM4628, core voltage set at to 1.13V (R4, 68.1K), - added resistors R380-R383, R370-R371 for configuration of DCDC converters - added solder jumper SJMP2 to sense signals on LTM4628 Page 05: - LOGIC P, VCCIO3A and VCCIO3D from 2.5V to 3.3V supply - LOGIC G, VCCPD3 from 2.5V to 3.3V supply - capacitors C147, C148, C151, C157, C159, C160 for FPGA BANK3 moved from 2.5V to 3.3V supply - voltage indicator LED resistors (R21, R23, R26, R29) replaced with 10K Page 06: - fixed bug, swapped signals SPI_SO_D1 and SPI_WP2_D2 on LOGIC - SPIFLASHX4_I, N25Q512A13GF840 E replaced with M25QS256A13EF840 Page 07: - fixed Title Block - 10K pull-up resistors for display (R64-R70) replaced with 1K - added buttons PBF2 parallel to PBF1 and PBF2 parallel to PBP1 - USB1A microcontroller, added pull-up and pull-down on URES (R84) and WAKEUP (R93) signals - lighter values for LED resistors Page 08: - changed reference designators L1A > L6, L1B > L7, L1C > L8 Page 09: - LOGIC N (BANK GX8_L1), unused RX pins connected to GND - LOGIC M (BANK GX8_L0), unused RX and REFCLK pins connected to GND - WR clock to LOGIC L (BANK 8D), added 0R resistors (R390, R391, R392, R393) parallel to capacitors - PCI clock to LOGIC L (BANK 8D) pins C15, B15, removed caps C348, C349, now clock is DC coupled - removed LOGIC K (BANK 8A) - moved BANK 4D to this page, for PCI bus signals, added GNT, REQ, INTx#-D Page 10: - replaced voltage translators with bus switches (PCISW1-9) on PCI-signals - added 0R resistors (R330-R355) between bus switches and PMC connectors - added circuit for bus switches power (DS42, R364, R363) - added 0R resistor (R362) on signal PCI_M66EN to GND Page 11: - removed LOGIC E (BANK 4D) - placed LOGIC K (BANK 8A) - on OSC_RTC K clock to BANK 8A, added 0R resistors (R392, R393) parallel to capacitors - changed Reference Designator J33_ODRV to JODRV_33 Page 12: - added 0R resistors parallel to fuses on IOs - different resistors for IO leds (swapped values) - marked IO pair with 50R impedance Page 13: - added 0R resistors parallel to fuses on IOs - different resistors for IO leds (swapped values) - marked IO pair with 50R impedance	dslavinec	B
15.11.2016	After review fixes, added JTAG to backplane connection: Page 06: - JTAG signals from JTAGCON1 routed through 0R resistors to PN1/PN2 (p10) then back to DTV1 (PMC connector added parallel to JTAGCON1) Page 07: - FPGA PBF1, PBF2 button pull-up, powers supply from 2.5V to 3.3V - R72 is placed, R94 is DNP (Do Not Place) Page 10: - JTAG signals on PN1/PN2 connected parallel to JTAGCON1 on p06	dslavinec	B
21.4.2017	PCI bus switch enable bug fix: Page 09: - PCI_BSW_EN# signal connected to BANK4D Page 10: - PCI_BSW_EN# drives bus switch enable (pulled-up during FPGA boot, then FPGA enables bus switches by pulling line down)	dslavinec	B
20.11.2017	JTAG split modification Page 6: micro USB JTAG connector connected directly to 100R resistors Page 10: added DIP switch on JTAG signals to PMC connectors	dslavinec	C
16.05.2018	Page 5: added load resistors R1033, R1034 to outputs of the voltage regulators for display Page all: added license text	dslavinec	C
21.09.2018	Page 4: CMC bezel (FP1) added and connected to GND through jumper J1	mlevicnik	C
19.11.2018	Page 7: : changed values of R115, R111, R112, R114, R119, R116 and led colors of D26, D28, D30, D31, D27, D29,	dslavinec	C

Value	Capatitors used
12p	0402, 50V, C0G, 1%
22p	0402, 50V, C0G, 1%
10n	0402, 25V, X7R, 10%
100n	0402, 25V, X7R, 10%
1u	0603, 16V, X7R, 10%
2.2u	1210, 100V, X7R, 10%
10u	1210, 25V, X7R, 10%
22u	1210, 10V, X7R, 10%
100u	1210, 10V, X5R, 20%

All resistors are SMD 0402, 63mW, 1% except where marked differently.

Components marked DNP (Do Not Place) are foreseen for testing purposes.

TOP layer

FM1 FIDUCIAL FM2 FIDUCIAL FM3 FIDUCIAL

BOTTOM layer

FM4 FIDUCIAL FM5 FIDUCIAL FM6 FIDUCIAL

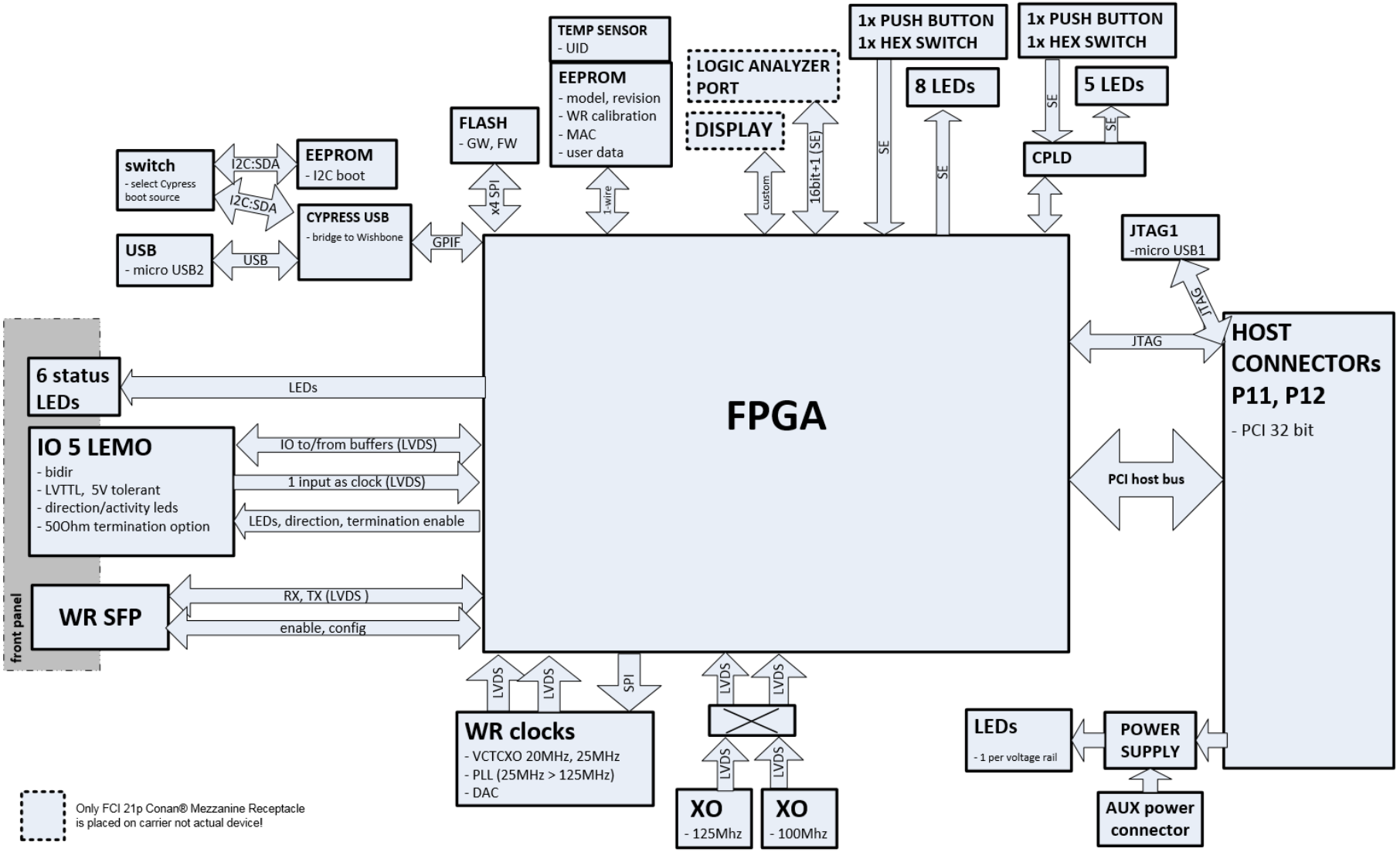
DRAWN	Dušan Slavinec		19.9.2016
CHECKED	-		
APPROVED	-		

Title: FAIR Timing Receiver (FTRN) PMC form factor - CSL_FTRN_PMC

Size: A3 | Type: SE | DWG.NO. CSL_FTRN_PMC | REV. C

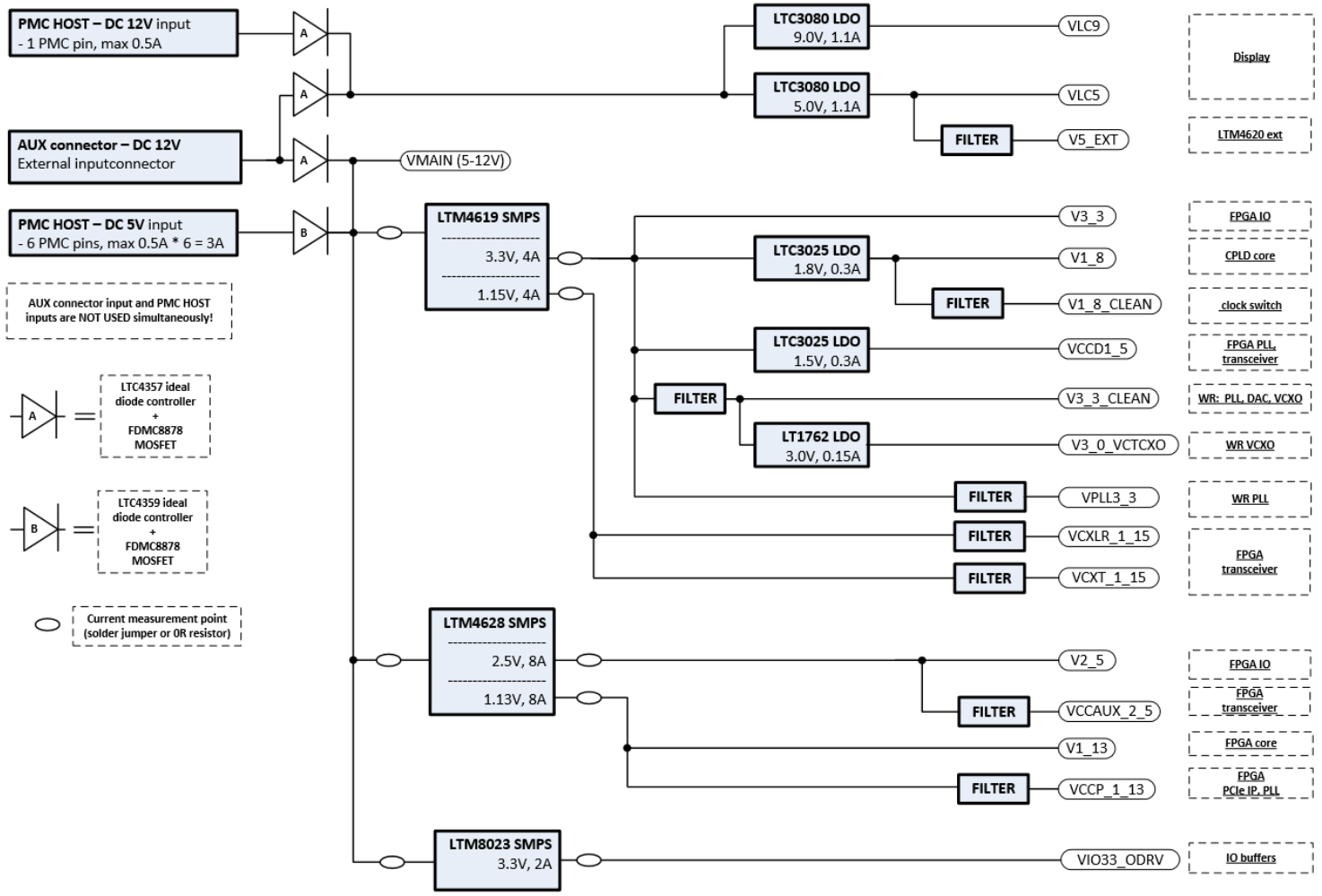
SHEET 1 OF 13

Block Diagram



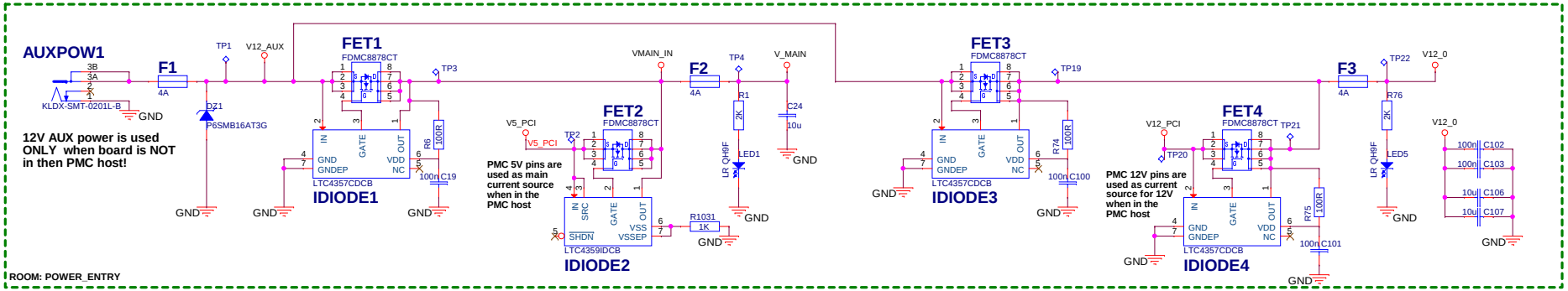
Title: Block Diagram				
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PMC	REV. B	
			SHEET 2 OF 13	

Power tree block scheme

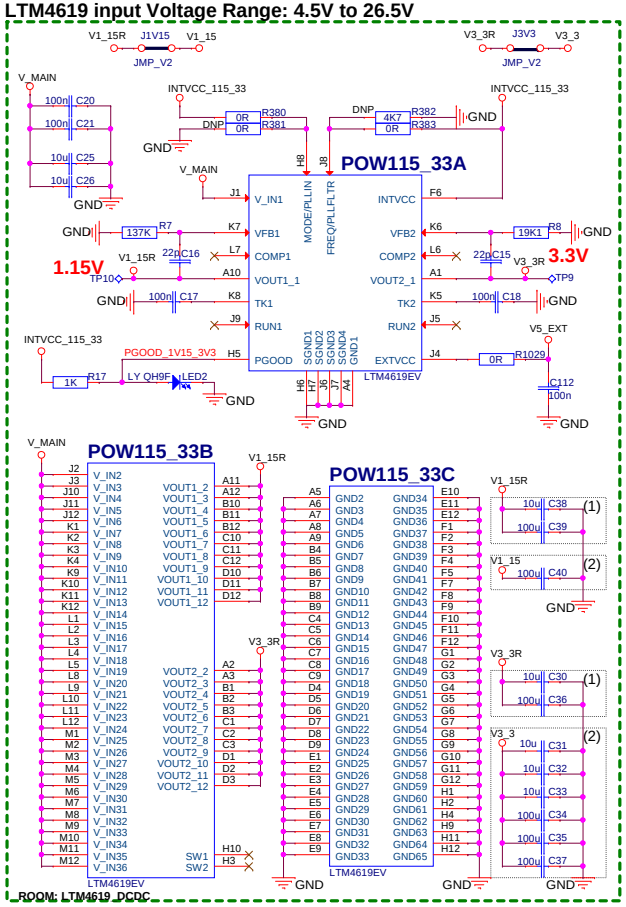


Title: Power tree block scheme				
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PMC		REV. B
			SHEET 3 OF 13	

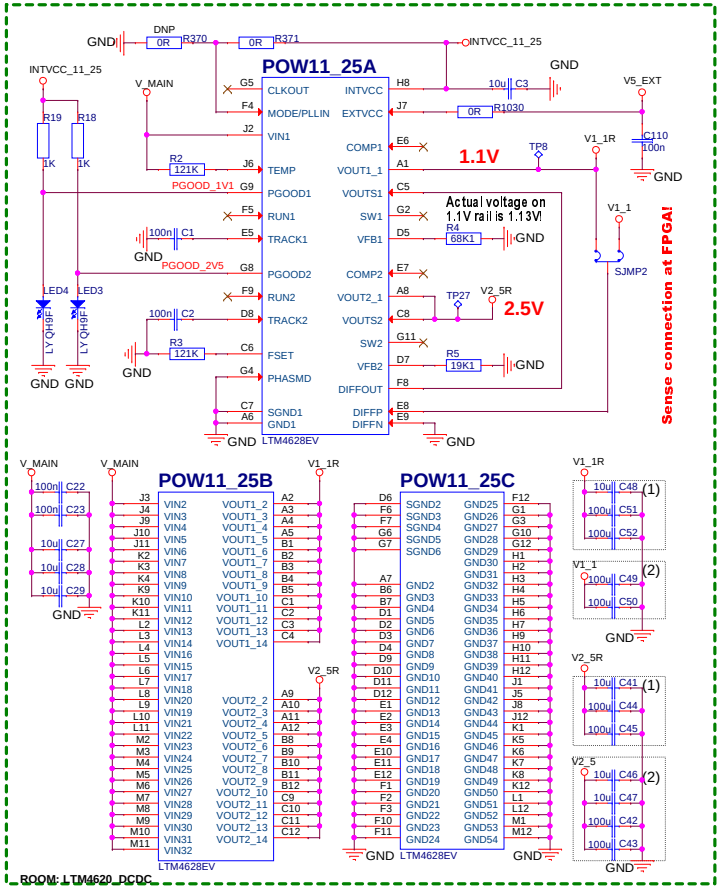
Power entry and main DCDC power regulators



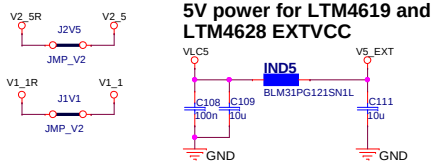
LTM4619 input Voltage Range: 4.5V to 26.5V



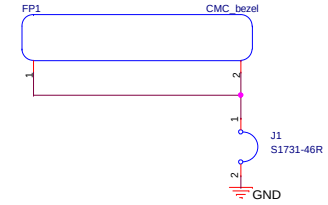
LTM4628 input Voltage Range: 4.5V to 16V



5V power for LTM4619 and LTM4628 EXTVCC



Optional CMC bezel connection to GND

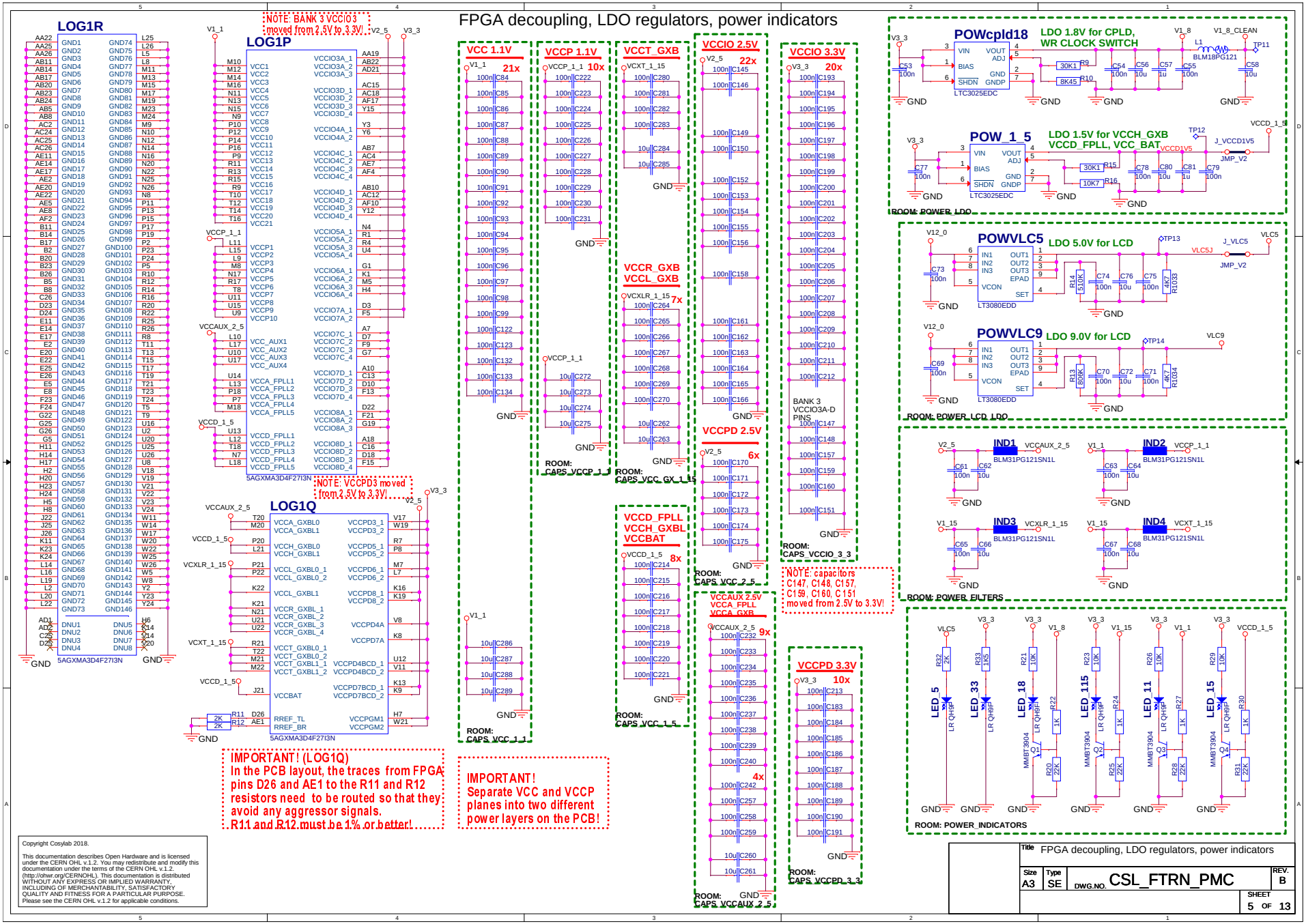


(1) - place capacitors at the regulator outputs

(2) - place capacitors away from the regulator outputs

Title: Power entry and main DCDC power regulators				
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PMC		REV. B
			SHEET 4 OF 13	

FPGA decoupling, LDO regulators, power indicators



Title	FPGA decoupling, LDO regulators, power indicators
Size	A3
Type	SE
DWG.NO.	CSL_FTRN_PMC
REV.	B
SHEET	5 OF 13

FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash

JTAGCON1 and PN1/PN2 JTAG signals are connected in parallel when DIP switch is on!

Micro USB JTAG connector

JTAGCON1

ZX62-B-5PA(11)

DTV1

TPD6E05U06RVZR

DTV1 pins 1-4 and 6-7 are NC, but can be used for straight-through routing.

To PN1/PN2 PMC JTAG, see p10

JTAG buffer and protection

DRV1

SN74LVC125ARGY

JTAG signal pull-ups, FPGA-CPLD side

JTAG signal pull-ups, connector side

ROOM: JTAG_INPUT

FPGA configuration and JTAG

LOG1O

5AGXMA3D4F27I3N

FPGA configuration FLASH

SPIFLASHX4_1

N25Q256A13EF840

Board ID ROM, temp. sensor

ROM1

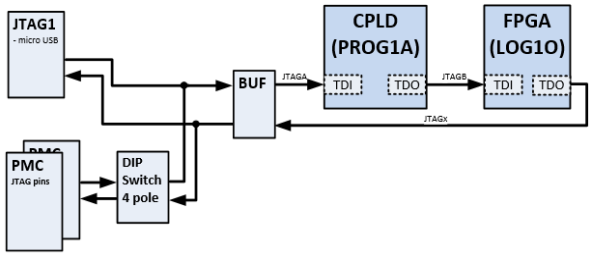
DS18B20U+

User FLASH

ROM2

DS28EC20P

ROOM: MEMORY



Reset supervisors

RST1

RST2

TPS3823-33DBVT

PROG1C

XC2C64A-7CPG56C

ROOM: PROG_CPLD

XOF1

ECS-2033-500-BN

PROG1A

XC2C64A-7CPG56C

PROG1B

XC2C64A-7CPG56C

LOG1H

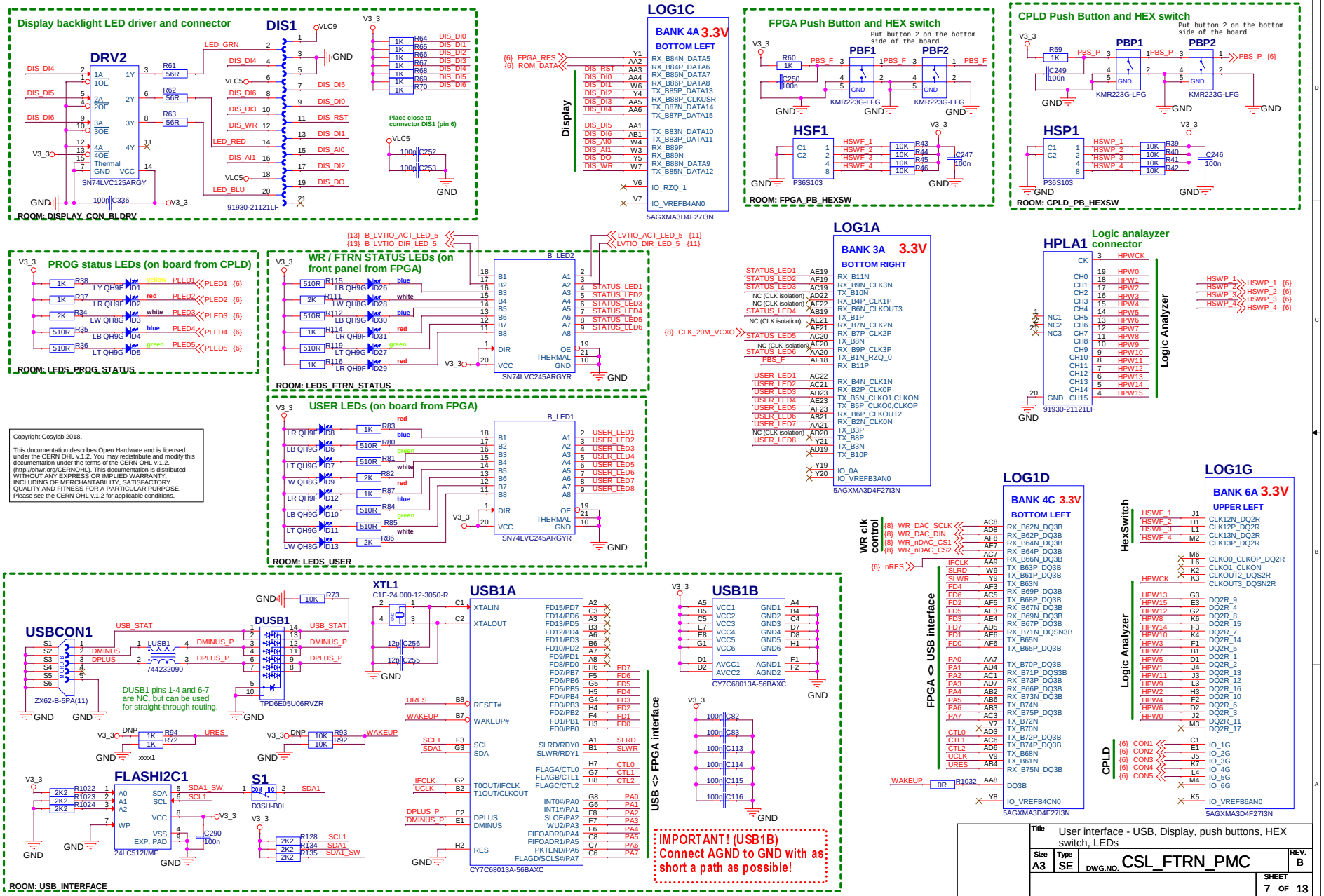
BANK 7A

TOP LEFT 3.3V

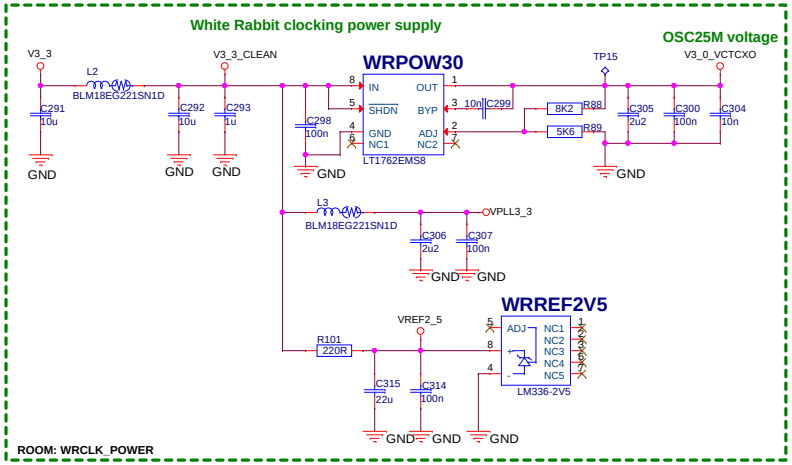
5AGXMA3D4F27I3N

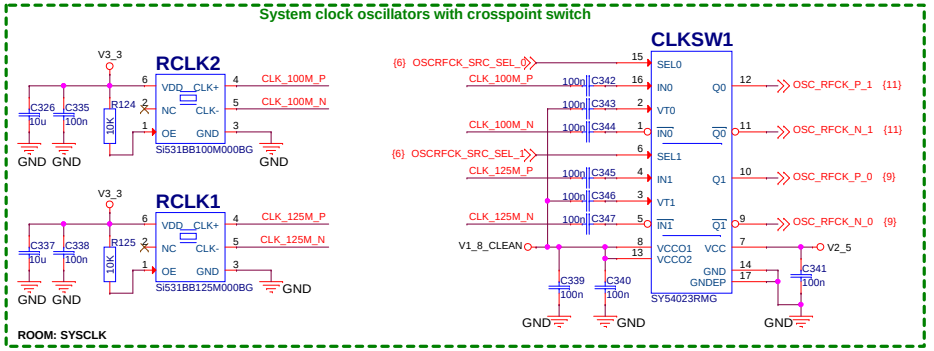
Title	FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
			SHEET 6 OF 13

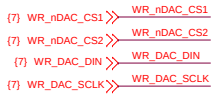
User interface - USB, Display, push buttons, HEX switch, LEDs

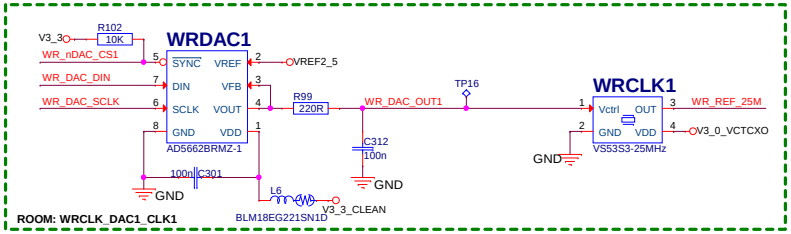


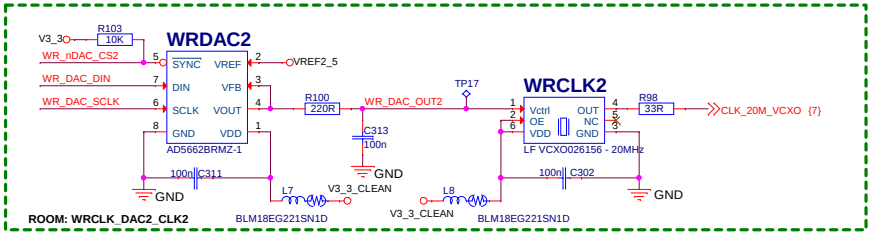
Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch

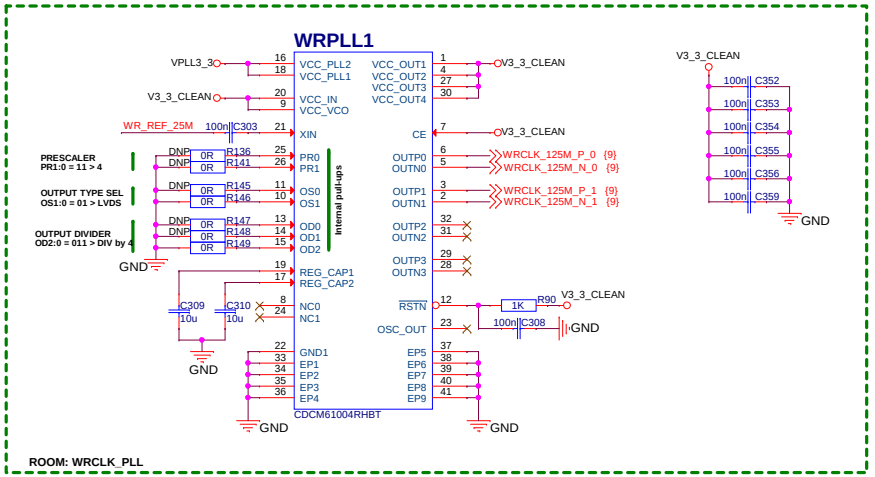






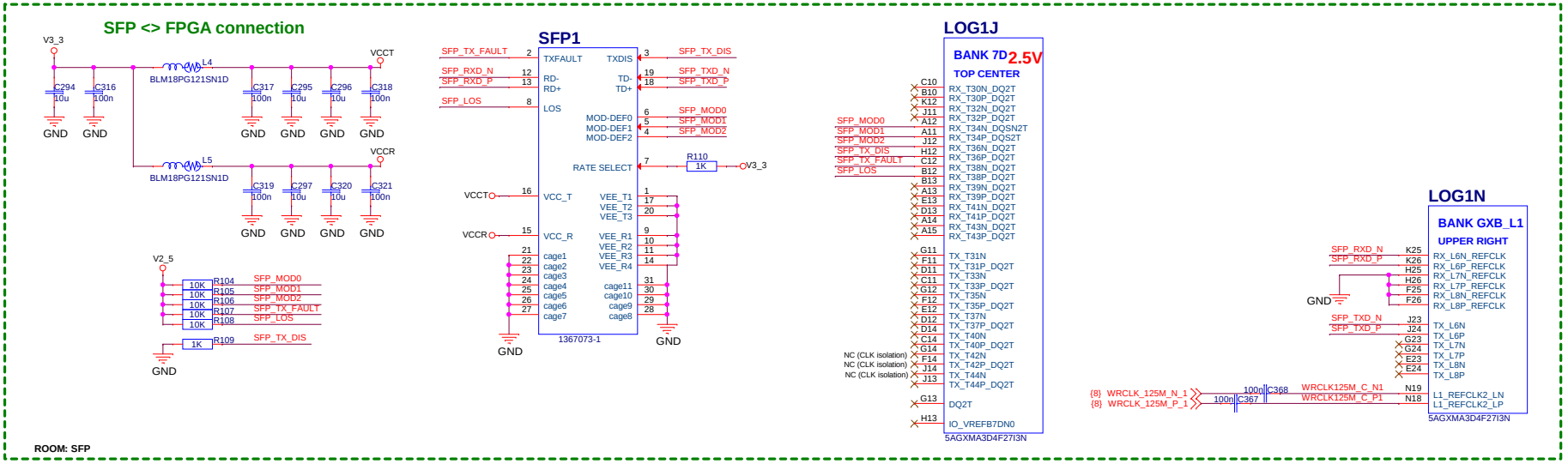


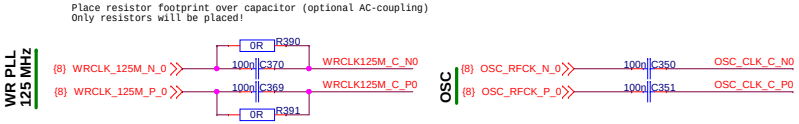


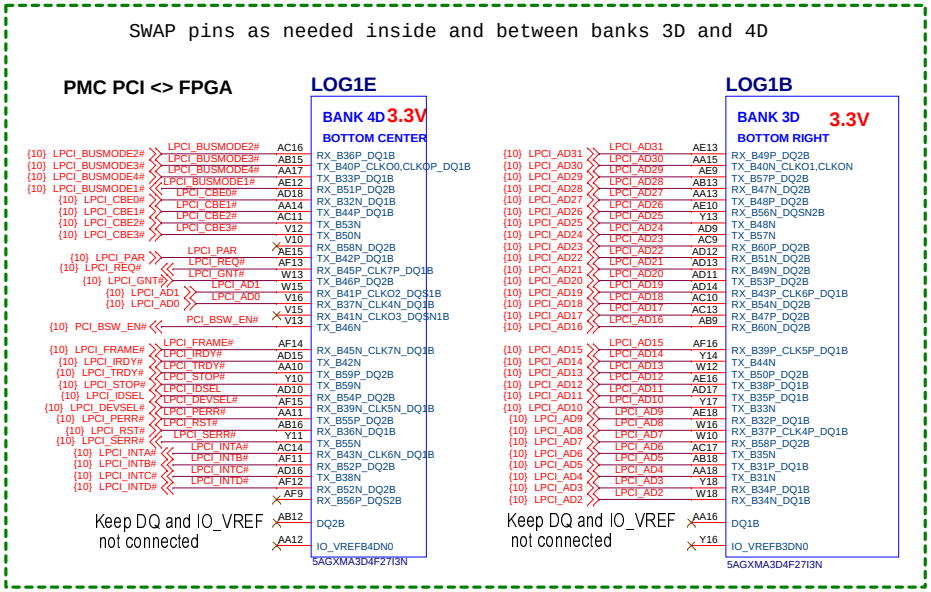


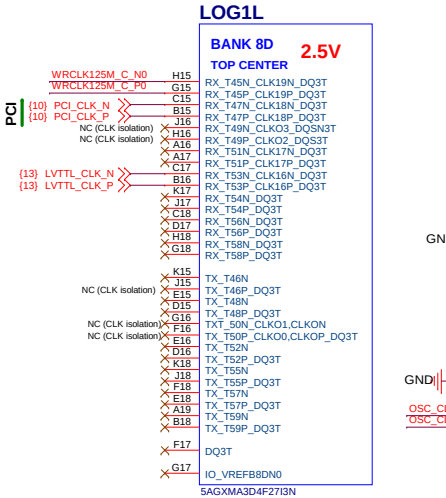
Title	Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
			SHEET 8 OF 13

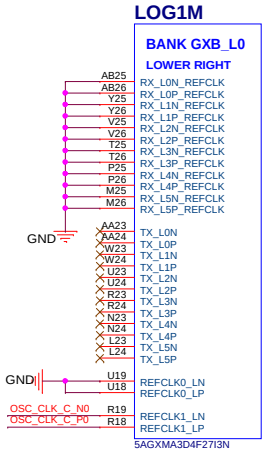
Fiber SFP, PCI <> FPGA connections





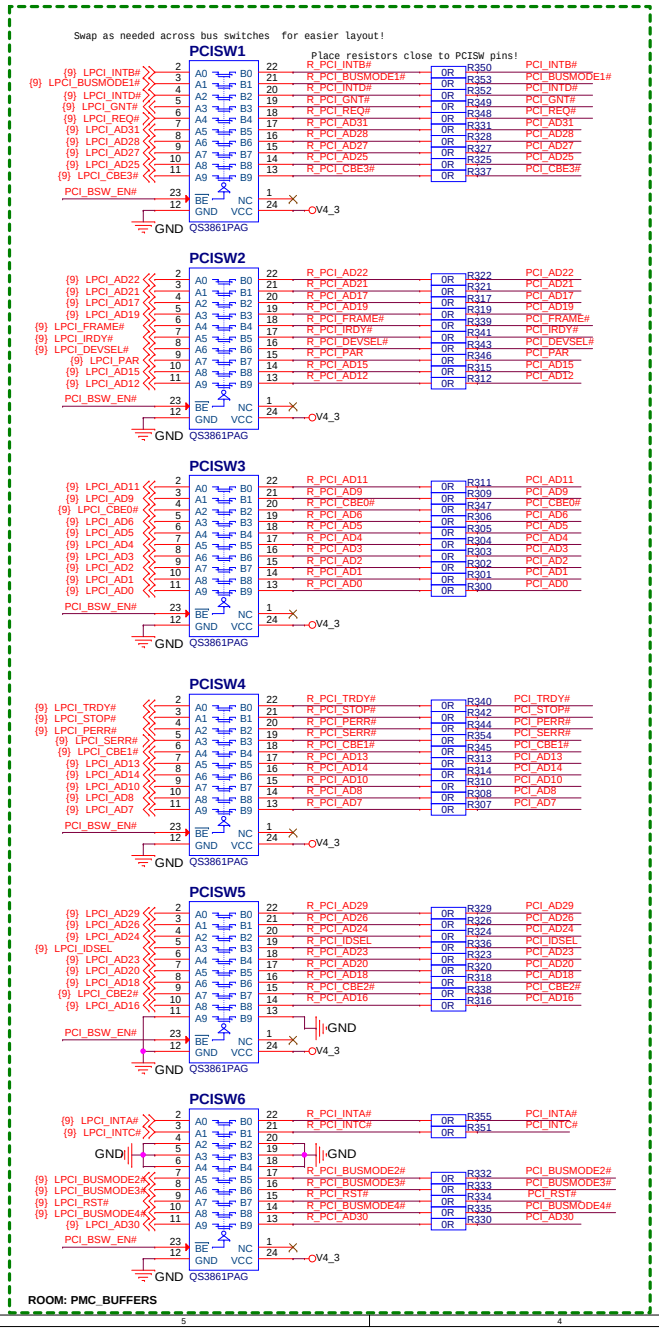


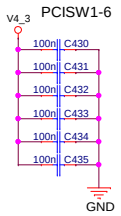


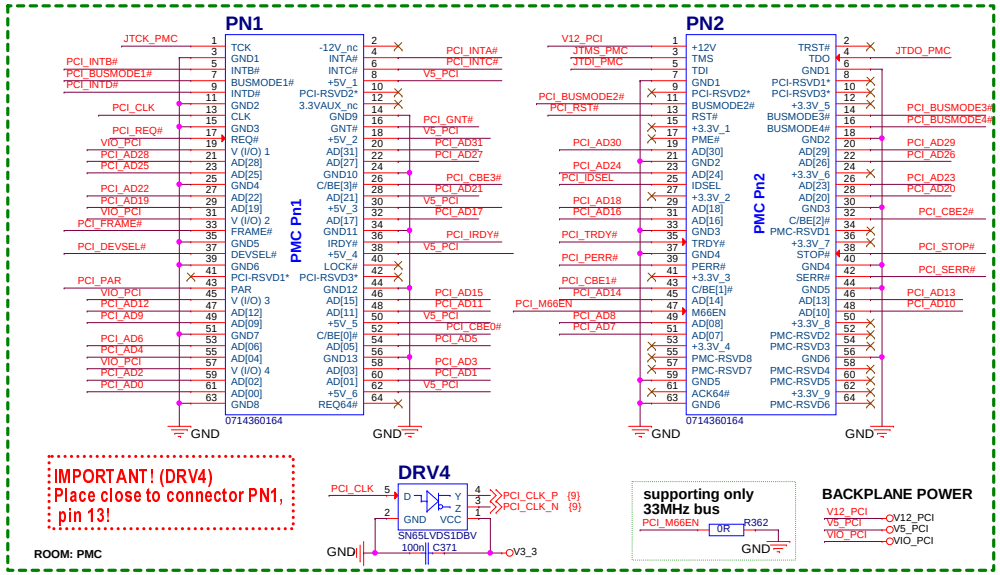


Title	Fiber SFP, PCI <> FPGA connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
			SHEET 9 OF 13

PMC host interface

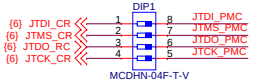






Bus switch enable (pulled low by FPGA after FPGA boot when FPGA enters user mode)

CPLD-FPGA JTAG chain <---> PMC connector JTAG pins



VCC for bus switches, see
- https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/ds/ds_stratix_pci_bd.pdf
- https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an330.pdf

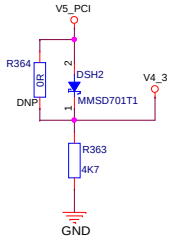
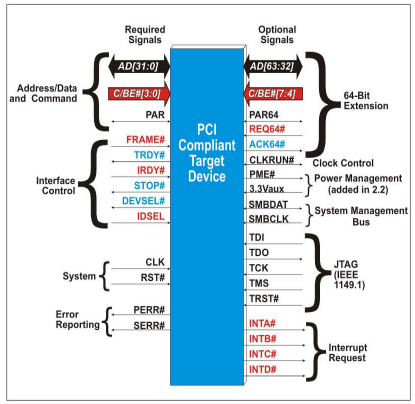
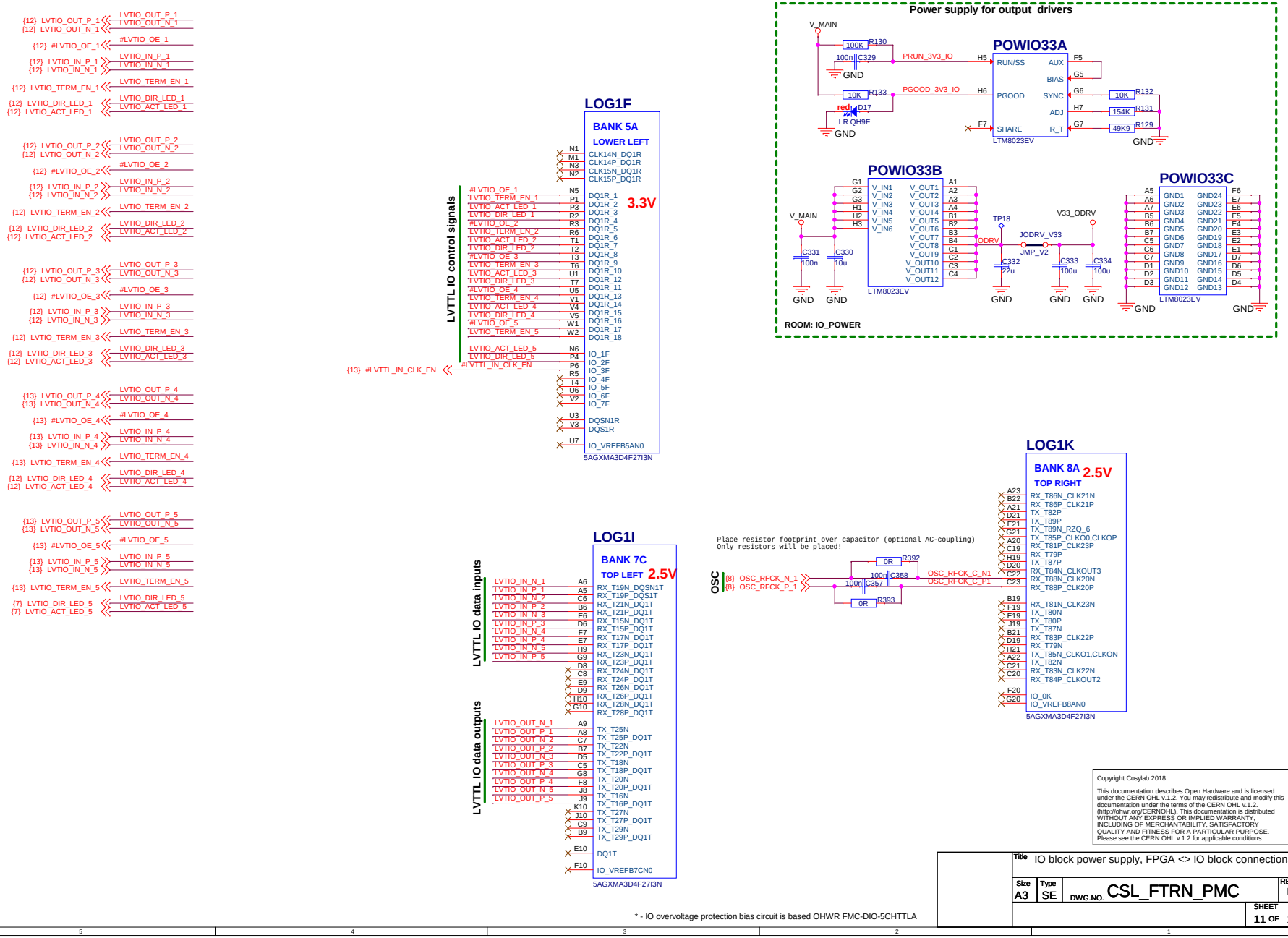


Figure 4-2: PCI-Compliant Target Device Signals



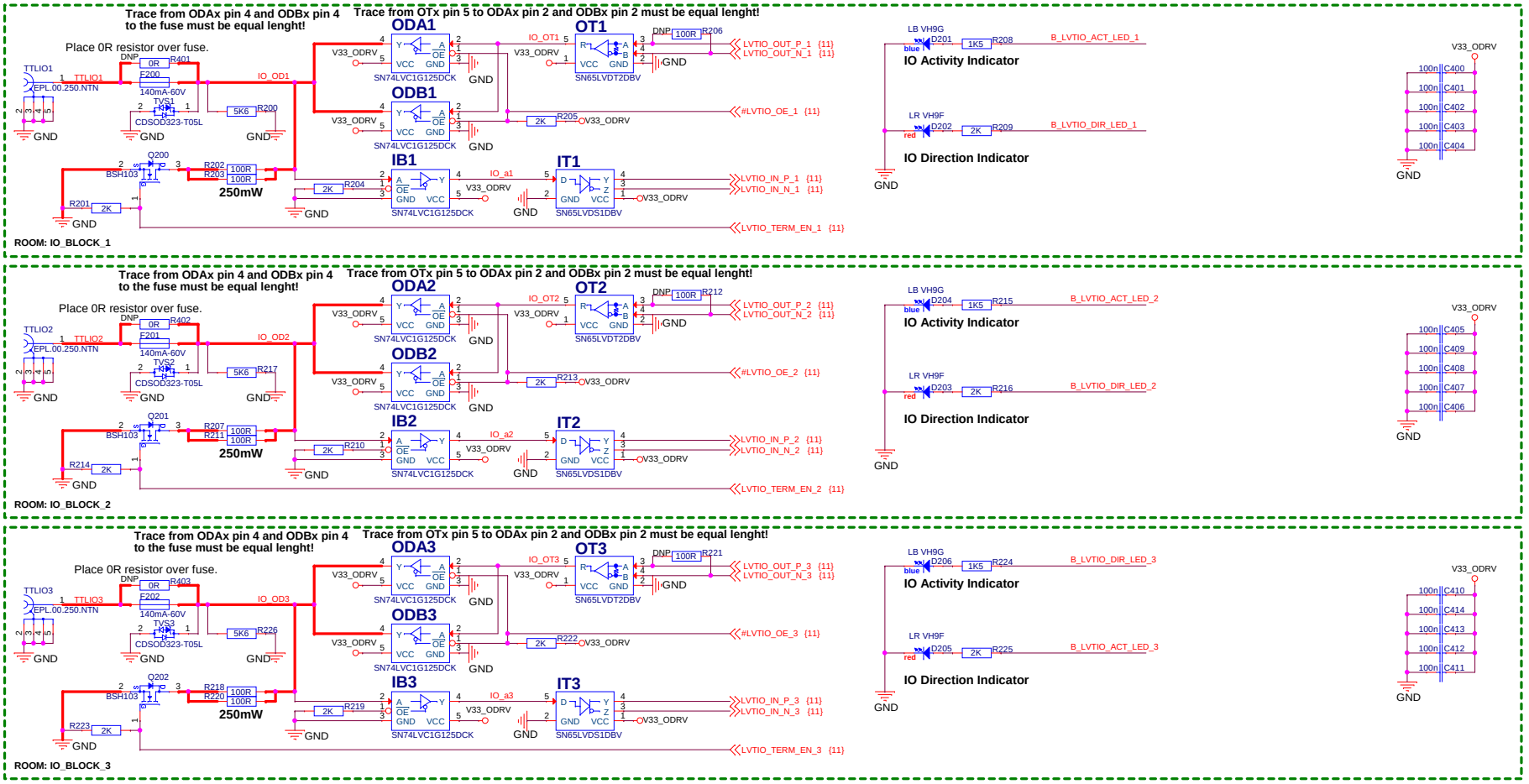
Title: PMC host interface				
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PMC	REV. B	
			SHEET 10 OF 13	

IO block power supply, FPGA <> IO block connections

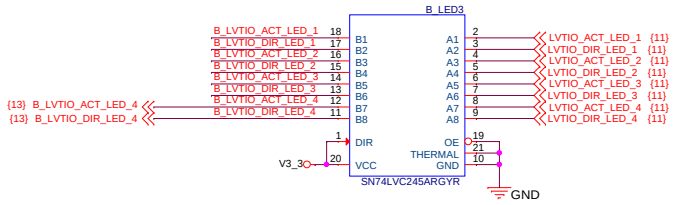


Title: IO block power supply, FPGA <> IO block connections			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PMC	REV. B
			SHEET 11 OF 13

LVTTL IO blocks 1-3

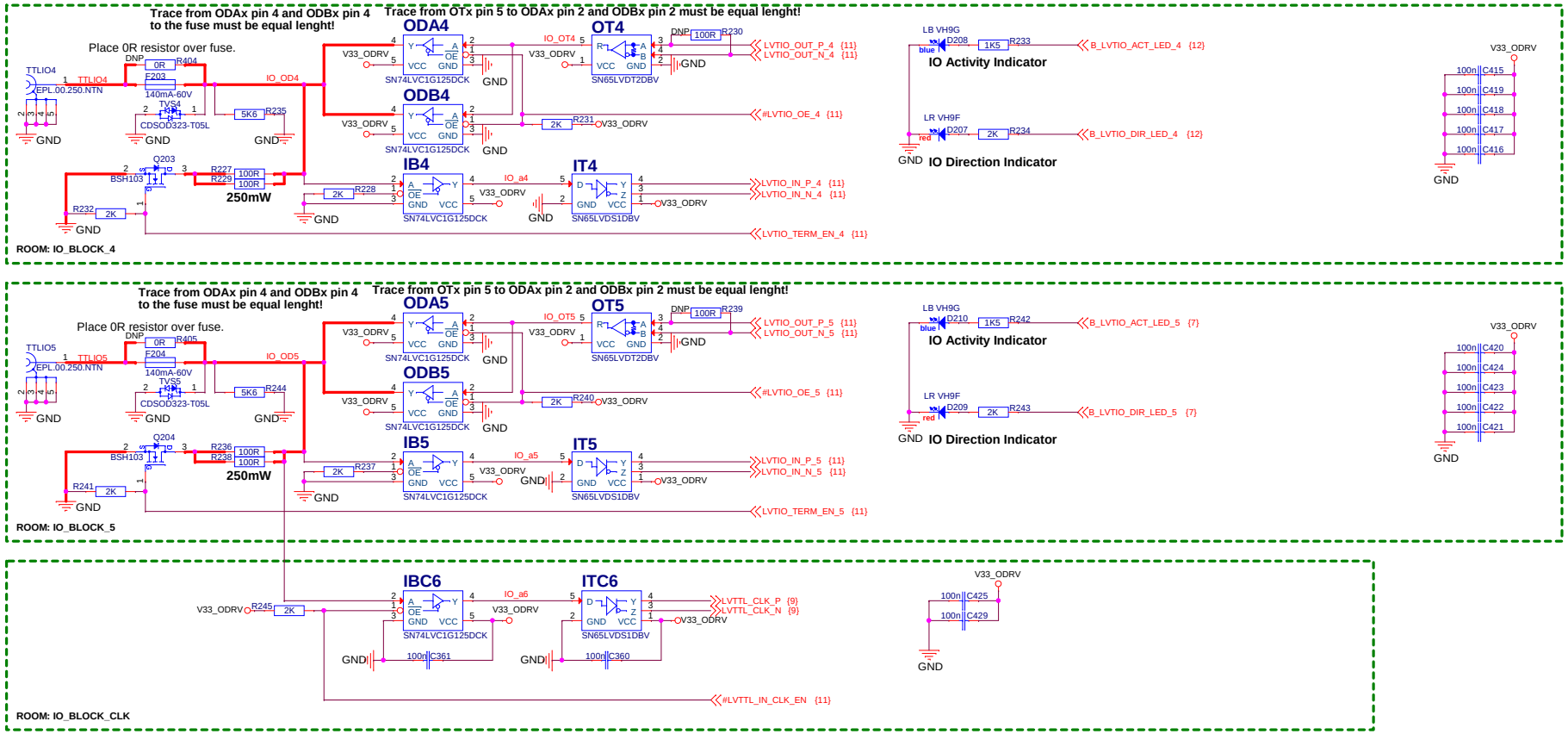


Z = 50R !



Title	LVTTL IO blocks 1-3		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
			SHEET 12 OF 13

LVTTL IO blocks 4-5, IO CLOCK input



Title	LVTTL IO blocks 4-5, IO CLOCK input		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
			SHEET 13 OF 13