FAIR Timing Receiver (FTRN) PMC form factor - CSL_FTRN_PMC

SHEET	TITLE
1	TITLE PAGE
2	Block diagram
3	Power Tree
4	POWER DC-DC
5	POWER LDOs, FPGA BYPASS
6	FPGA configuration
7	FPGA user interface
8	WR clocking, system CLOCKS
9	PMC, SFP to FPGA
10	PMC host
11	IO to FPGA
12	IO blocks 1-3
13	IO blocks 4-5, IO clk

Value	Capatitors used
12p	0402, 50V, C0G, 1%
22p	0402, 50V, C0G, 1%
10n	0402, 25V, X7R, 10%
100n	0402, 25V, X7R, 10%
1u	0603, 16V, X7R, 10%
2.2u	1210, 100V, X7R, 10%
10u	1210, 25V, X7R, 10%
22u	1210, 10V, X7R, 10%
100u	1210, 10V, X5R, 20%

All resistors are SMD 0402, 63mW, 1% except where marked differently.

Components marked DNP (Do Not Place) are foreseen for testing purposes.

DATE	REVISION DESCRIPTION	DRAWN	REV
04.12.2014	Initial version	dslavinec	A
21.4.2015	Added fixes found during HDL synthesis check and changes during PCB layout	dslavinec, bpecnik	A
21.5.2015	PCB layout ready for review	dslavinec, bpecnik	A
19.9.2016	Page 04: - LTM4620 replaced with LTM4628 - LTM4628, core voltage rail set to 1.13V (R4, 68.1K), - added resistors R380-R383, R370-R371 for configuration of DCDC converters - added solder jumper SJMP2 to sense signals on LTM4628 Page 05: - LOG1P, VCCIO3A and VCCIO3D from 2.5V to 3.3V supply - LOG1Q, VCCPD3 from 2.5V to 3.3V supply - capacitors C147, C148, C151, C157, C159, C160 for FPGA BANK3 moved from 2.5V to 3.3V supply - voltage indicator LED resistors (R21, R23, R26, R29) replaced with 10K Page 06: - fixed bug, swapped signals SPI_SO_D1 and SPI_WP2_D2 on LOG1O - SPIFLASHX4_1, N25Q512A13GF840E replaced with N25Q256A13EF840 Page 07: - fixed Title Block - 10K pull-up resistors for display (R64-R70) replaced with 1K - added buttons PBF2 parallel to PBF1 and PBP2 parallel to PBP1 - USB1A microcontroller, added pull-up and pull-down on URES (R94) and WAKEUP (R93) signals - higher values for LED resistors Page 08: - changed reference designators L1A > L6, L1B > L7, L1C > L8 Page 09: - LOG1N (BANK GXB_L1), unused RX pins connected to GND - LOG1M (BANK GXB_L0), unused RX and REFCLK pins connected to GND - WR clock to LOG1L (BANK 8D), added 0R resistors (R390, R391, R392, R393) parallel to capacitors - PCI clock to LOG1L (BANK 8D) pins C15, B15, removed caps C348, C349, now clock is DC coupled - removed LOG1K (BANK 8A) - moved BANK 4D to this page, for PCI bus signals, added GNT, REQ, INTxB-D Page 10: - replaced voltage translators with bus switches (PCISW1-6) on PCI signals - added 0R resistors (R300-R355) between bus switches and PMC connectors - added circuit for bus switches power (DSH2, R364, R363) - added 0R resistor (R362) on signal PCI_M66EN to GND Page 11: - removed LOG1E (BANK 4D) - placed LOG1K (BANK 8A) - on OSC_RFCK clock to BANK 8A, added 0R resistors (R392, R393) parallel to capacitors - changed Reference Designator J33_ODRV to JODRV_33 Page 12: - added 0R resistors parallel to fuses on IOs - different resistors for IO leds (swapped values) - marked IO path with 50R impedance Page 13: - added 0R resistors parallel to fuses on IOs - different resistors for IO leds (swapped values) - marked IO path with 50R impedance	dslavinec	B
15.11.2016	After review fixes, added JTAG to backplane connection: Page 06: - JTAG signals from JTAGCON1 routed through 0R resistors to PN1/PN2 (p10) then back to DTV1 (PMC connector added parallel to JTAGCON1) Page 07: - FPGA PBF1, PBF2 button pull-up power supply from 2.5V to 3.3V - R72 is placed, R94 is DNP (Do Not Place) Page 10: - JTAG signals on PN1/PN2 connected parallel to JTAGCON1 on p06	dslavinec	B
21.4.2017	PCI bus switch enable bug fix: Page 09: - PCI_BSW_EN# signal connected to BANK4D Page 10: - PCI_BSW_EN# drives bus switch enable (pulled-up during FPGA boot, then FPGA enables bus switches by pulling line down)	dslavinec	B

TOP layer

FM1 FIDUCIAL FM2 FIDUCIAL FM3 FIDUCIAL

BOTTOM layer

FM4 FIDUCIAL FM5 FIDUCIAL FM6 FIDUCIAL

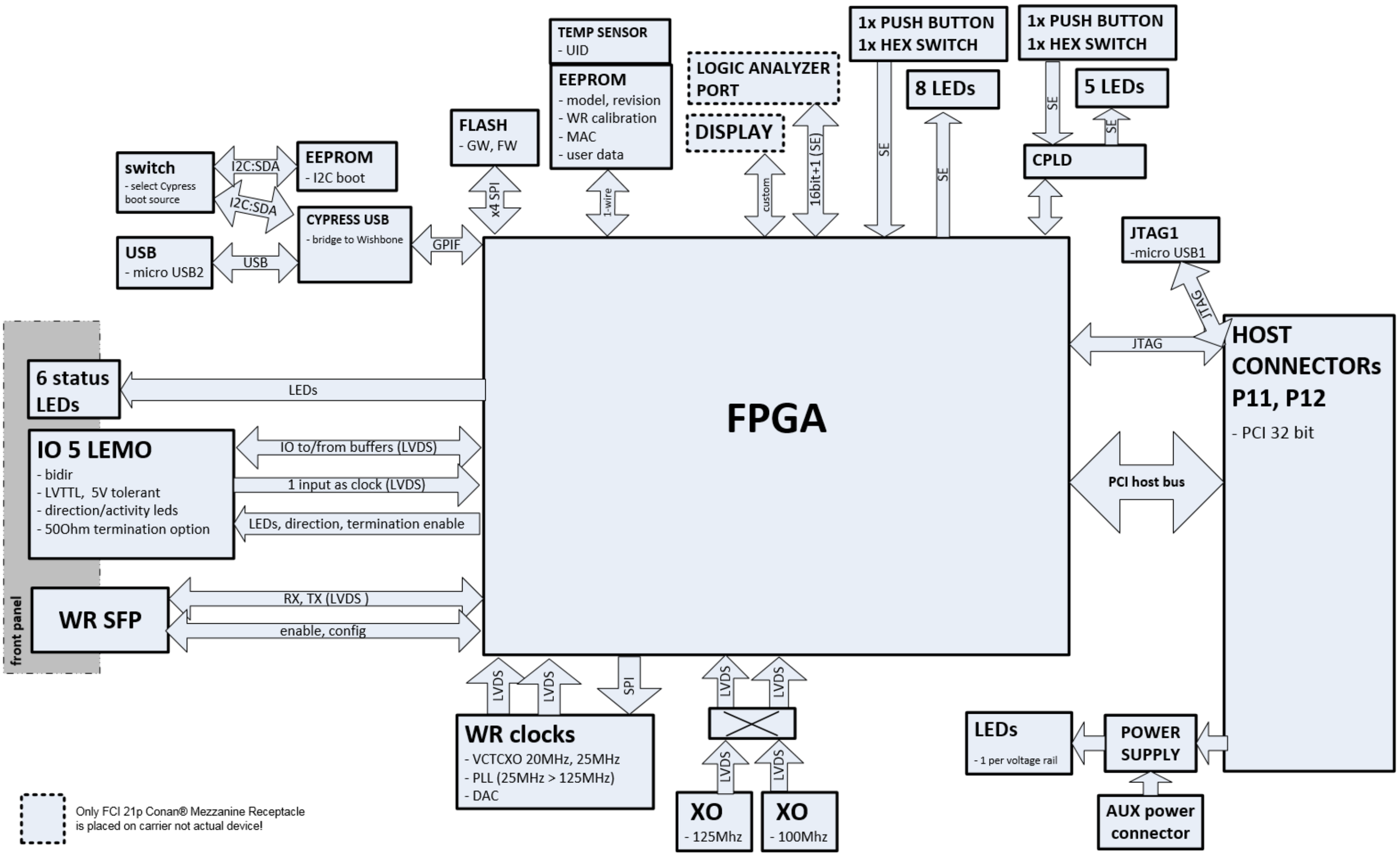
DRAWN	Dušan Slavinec		19.9.2016
CHECKED	-		
APPROVED	-		

Title: FAIR Timing Receiver (FTRN) PMC form factor - CSL_FTRN_PMC

Size: A3 | Type: SE | DWG.NO.: CSL_FTRN_PMC | REV.: B

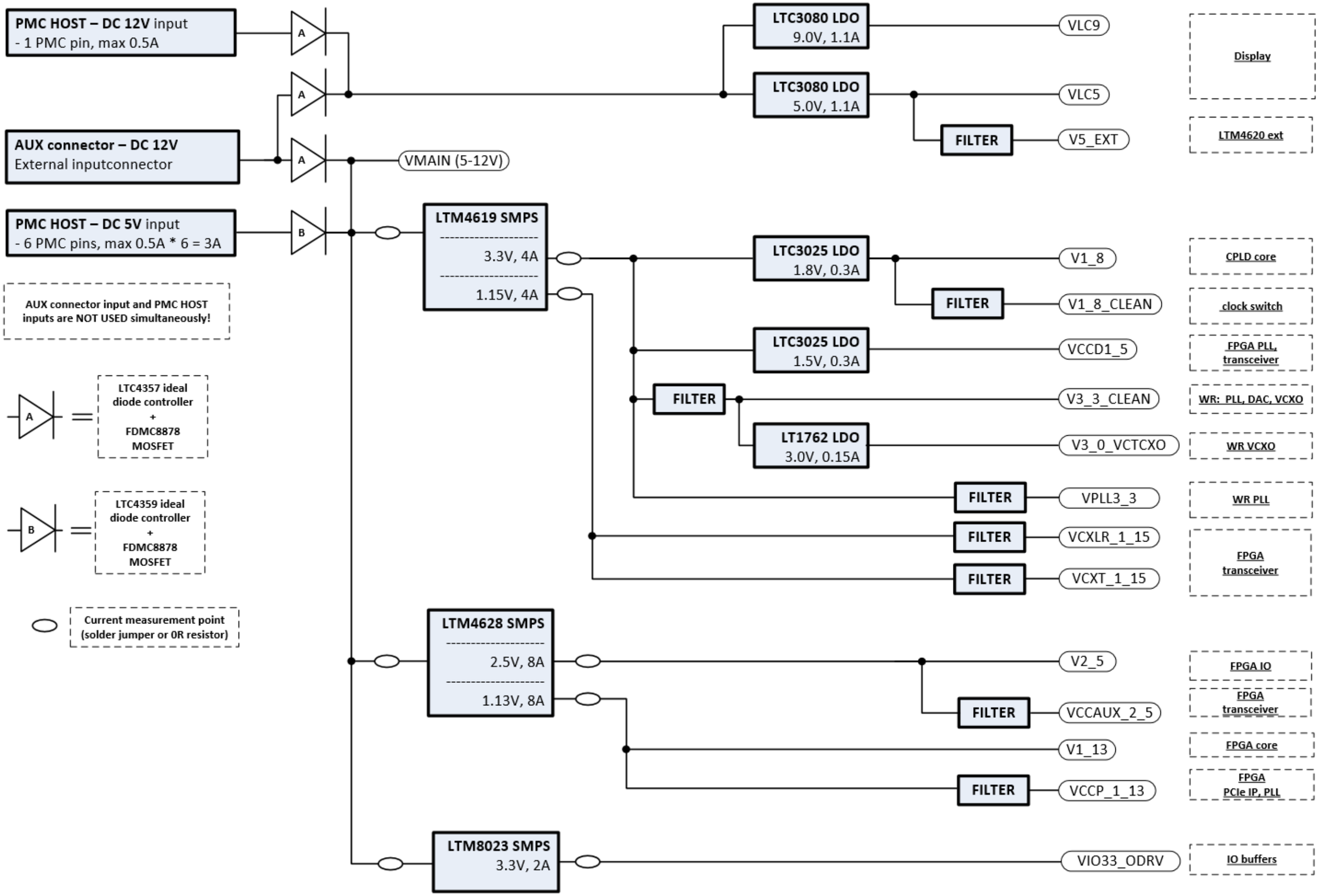
SHEET 1 OF 13

Block Diagram



Title: Block Diagram			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PMC	REV. B
		SHEET 2 OF 13	

Power tree block scheme



Title	Power tree block scheme		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
			SHEET 3 OF 13

Power entry and main DCDC power regulators

AUXPOW1

KLDX-SMT-0201L-B

F1 4A

TP1 V12_AUX

DZ1 P6SMB16AT3G

12V AUX power is used ONLY when board is NOT in then PMC host!

FET1 FDMC8878CT

LTC4357CDCB **IDIODE1**

TP3

FET2 FDMC8878CT

VMAIN_IN F2 4A TP4 V_MAIN

V5_PCI TP2

PMC 5V pins are used as main current source when in the PMC host

LTC4359IDCB **IDIODE2**

R1 2K LED1 LR QH9F C24 10u R1031 1K

FET3 FDMC8878CT

LTC4357CDCB **IDIODE3**

TP19

F3 4A TP22 V12_0

R76 2K LED5 LR QH9F

FET4 FDMC8878CT

V12_PCI TP20 TP21

PMC 12V pins are used as current source for 12V when in the PMC host

LTC4357CDCB **IDIODE4**

100n C102 100n C103 10u C106 10u C107

ROOM: POWER_ENTRY

LTM4619 input Voltage Range: 4.5V to 26.5V

V1_15R J1V15 V1_15 JMP_V2

V3_3R J3V3 V3_3 JMP_V2

V_MAIN 100n C20 100n C21 10u C25 10u C26

INTVCC_115_33

POW115_33A

1.15V TP10 137K R7 100n C17

3.3V TP9 19K1 R8 100n C18

PGOOD_1V15_3V3 1K R17 LY QH9F LED2

V5_EXT 0R R1029 C112 100n

LTM4619EV

POW115_33B

POW115_33C

V1_15R 10u C38 (1) 100u C39

V1_15 100u C40

V3_3R 10u C30 (1) 100u C36

V3_3 10u C31 (2) 10u C32 10u C33 100u C34 100u C35 100u C37

ROOM: LTM4619_DCDC

LTM4628 input Voltage Range: 4.5V to 16V

POW11_25A

INTVCC_11_25 R370 0R R371 0R

1.1V TP8 V1_1R C110 100n

Actual voltage on 1.1V rail is 1.13V!

R4 68K1 R5 19K1

2.5V TP27 V2_5R

V1_1 SJMP2

Sense connection at FPGA!

LED4 LED3 LY QH9F

R1030 0R

LTM4628EV

POW11_25B

POW11_25C

V1_1R 10u C48 (1) 100u C51 100u C52

V1_1 100u C49 (2) 100u C50

V2_5R 10u C41 (1) 100u C44 100u C45

V2_5 10u C46 (2) 10u C47 100u C42 100u C43

ROOM: LTM4620_DCDC

V2_5R V2_5 J2V5 JMP_V2

V1_1R V1_1 J1V1 JMP_V2

5V power for LTM4619 and LTM4628 EXTVCC

VLC5 IND5 BLM31PG121SN1L V5_EXT

C108 100n C109 10u C111 10u

(1) - place capacitors on the regulator outputs

(2) - place capacitors away from the regulator outputs

Title: Power entry and main DCDC power regulators			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PMC	REV. B
		SHEET 4 OF 13	

FPGA decoupling, LDO regulators, power indicators

LOG1R

5AGXMA3D4F27I3N

AA22	GND1	GND74	L25
AA25	GND2	GND75	L26
AA26	GND3	GND76	L5
AB11	GND4	GND77	L8
AB14	GND5	GND78	M11
AB17	GND6	GND79	M13
AB20	GND7	GND80	M15
AB23	GND8	GND81	M17
AB24	GND9	GND82	M19
AB5	GND10	GND83	M23
AB8	GND11	GND84	M24
AC2	GND12	GND85	M9
AC24	GND13	GND86	N10
AC25	GND14	GND87	N12
AC26	GND15	GND88	N14
AE11	GND16	GND89	N16
AE14	GND17	GND90	N20
AE17	GND18	GND91	N22
AE2	GND19	GND92	N25
AE20	GND20	GND93	N26
AE22	GND21	GND94	N8
AE5	GND22	GND95	P11
AE8	GND23	GND96	P13
AF2	GND24	GND97	P15
B11	GND25	GND98	P17
B14	GND26	GND99	P19
B17	GND27	GND100	P2
B2	GND28	GND101	P23
B20	GND29	GND102	P24
B23	GND30	GND103	P5
B26	GND31	GND104	R10
B5	GND32	GND105	R12
B8	GND33	GND106	R14
C26	GND34	GND107	R16
D23	GND35	GND108	R20
D24	GND36	GND109	R22
E11	GND37	GND110	R25
E14	GND38	GND111	R26
E17	GND39	GND112	R8
E2	GND40	GND113	T11
E20	GND41	GND114	T13
E22	GND42	GND115	T15
E25	GND43	GND116	T17
E26	GND44	GND117	T19
E5	GND45	GND118	T21
E8	GND46	GND119	T23
F23	GND47	GND120	T24
F24	GND48	GND121	T5
G22	GND49	GND122	T9
G25	GND50	GND123	U16
G26	GND51	GND124	U2
G5	GND52	GND125	U20
H11	GND53	GND126	U25
H14	GND54	GND127	U26
H17	GND55	GND128	U8
H2	GND56	GND129	V18
H20	GND57	GND130	V19
H23	GND58	GND131	V21
H24	GND59	GND132	V22
H5	GND60	GND133	V23
H8	GND61	GND134	V24
J22	GND62	GND135	W11
J25	GND63	GND136	W14
J26	GND64	GND137	W17
K11	GND65	GND138	W20
K23	GND66	GND139	W22
K24	GND67	GND140	W25
L14	GND68	GND141	W26
L16	GND69	GND142	W5
L19	GND70	GND143	W8
L2	GND71	GND144	Y2
L20	GND72	GND145	Y23
L22	GND73	GND146	Y24
AD1	DNU1	DNU5	H6
AD2	DNU2	DNU6	K14
C25	DNU3	DNU7	V14
D25	DNU4	DNU8	V20

GND GND

LOG1P

NOTE: BANK 3 VCCIO3 moved from 2.5V to 3.3V!

V1_1 V2_5 V3_3

5AGXMA3D4F27I3N

M10	VCC1	VCCIO3A_1	AA19
M12	VCC2	VCCIO3A_2	AB22
M14	VCC3	VCCIO3A_3	AD21
M16	VCC4	VCCIO3D_1	AC15
N11	VCC5	VCCIO3D_2	AC18
N13	VCC6	VCCIO3D_3	AF17
N15	VCC7	VCCIO3D_4	Y15
N9	VCC8		
P10	VCC9	VCCIO4A_1	Y3
P12	VCC10	VCCIO4A_2	Y6
P14	VCC11		
P16	VCC12	VCCIO4C_1	AB7
P9	VCC13	VCCIO4C_2	AC4
R11	VCC14	VCCIO4C_3	AE7
R13	VCC15	VCCIO4C_4	AF4
R15	VCC16		
R9	VCC17	VCCIO4D_1	AB10
T10	VCC18	VCCIO4D_2	AC12
T12	VCC19	VCCIO4D_3	AF10
T14	VCC20	VCCIO4D_4	Y12
T16	VCC21		
		VCCIO5A_1	N4
		VCCIO5A_2	R1
L11	VCCP1	VCCIO5A_3	R4
L15	VCCP2	VCCIO5A_4	U4
L9	VCCP3		
M8	VCCP4	VCCIO6A_1	G1
N17	VCCP5	VCCIO6A_2	K1
R17	VCCP6	VCCIO6A_3	M5
T8	VCCP7	VCCIO6A_4	H4
U11	VCCP8		
U15	VCCP9	VCCIO7A_1	D3
U9	VCCP10	VCCIO7A_2	F5
		VCCIO7C_1	A7
L10	VCC_AUX1	VCCIO7C_2	D7
L17	VCC_AUX2	VCCIO7C_3	F9
U10	VCC_AUX3	VCCIO7C_4	G7
U17	VCC_AUX4		
		VCCIO7D_1	A10
U14	VCCA_FPLL1	VCCIO7D_2	C13
L13	VCCA_FPLL2	VCCIO7D_3	D10
P18	VCCA_FPLL3	VCCIO7D_4	F13
P7	VCCA_FPLL4		
M18	VCCA_FPLL5	VCCIO8A_1	D22
		VCCIO8A_2	F21
U13	VCCD_FPLL1	VCCIO8A_3	G19
L12	VCCD_FPLL2	VCCIO8D_1	A18
T18	VCCD_FPLL3	VCCIO8D_2	C16
N7	VCCD_FPLL4	VCCIO8D_3	D18
L18	VCCD_FPLL5	VCCIO8D_4	F15

NOTE: VCCPD3 moved from 2.5V to 3.3V!

V2_5 V3_3

LOG1Q

5AGXMA3D4F27I3N

T20	VCCA_GXBL0	VCCPD3_1	V17
M20	VCCA_GXBL1	VCCPD3_2	W19
P20	VCCH_GXBL0	VCCPD5_1	R7
L21	VCCH_GXBL1	VCCPD5_2	P8
P21	VCCL_GXBL0_1	VCCPD6_1	M7
P22	VCCL_GXBL0_2	VCCPD6_2	L7
K22	VCCL_GXBL1	VCCPD8_1	K16
		VCCPD8_2	K19
K21	VCCR_GXBL_1		
N21	VCCR_GXBL_2		
U21	VCCR_GXBL_3	VCCPD4A	V8
U22	VCCR_GXBL_4		
		VCCPD7A	K8
R21	VCCT_GXBL0_1		
T22	VCCT_GXBL0_2		
M21	VCCT_GXBL1_1	VCCPD4BCD_1	U12
M22	VCCT_GXBL1_2	VCCPD4BCD_2	V11
		VCCPD7BCD_1	K13
J21	VCCBAT	VCCPD7BCD_2	K9
R11	RREF_TL	VCCPGM1	H7
R12	RREF_BR	VCCPGM2	W21

R11 2K, R12 2K, D26, AE1

VCCAUX_2_5 VCCD_1_5 VCXLR_1_15 VCXT_1_15 VCCD_1_5 VCCP_1_1 GND

IMPORTANT! (LOG1Q)
In the PCB layout, the traces from FPGA pins D26 and AE1 to the R11 and R12 resistors need to be routed so that they avoid any aggressor signals.
R11 and R12 must be 1% or better!

IMPORTANT!
Separate VCC and VCCP planes into two different power layers on the PCB!

VCC 1.1V

V1_1 — 21x

100n C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C122, C123, C132, C133, C134

GND

ROOM: CAPS_VCC_1_1

VCCP 1.1V

VCCP_1_1 — 10x

100n C222, C223, C224, C225, C226, C227, C228, C229, C230, C231

GND

VCCP_1_1

10u C272, C273, C274, C275

GND

ROOM: CAPS_VCCP_1_1

VCCT_GXB

VCXT_1_15

100n C280, C281, C282, C283

10u C284, C285

GND

VCCR_GXB VCCL_GXB

VCXLR_1_15 — 7x

100n C264, C265, C266, C267, C268, C269, C270

10u C262, C263

GND

ROOM: CAPS_VCC_GX_1_15

VCCD_FPLL VCCH_GXBL VCCBAT

VCCD_1_5 — 8x

100n C214, C215, C216, C217, C218, C219, C220, C221

GND

ROOM: CAPS_VCC_1_5

V1_1

10u C286, C287, C288, C289

GND

ROOM: CAPS_VCC_1_1

VCCIO 2.5V

V2_5 — 22x

100n C145, C146, C149, C150, C152, C153, C154, C155, C156, C158, C161, C162, C163, C164, C165, C166

GND

VCCPD 2.5V

V2_5 — 6x

100n C170, C171, C172, C173, C174, C175

GND

ROOM: CAPS_VCC_2_5

VCCAUX 2.5V VCCA_FPLL VCCA_GXB

VCCAUX_2_5 — 9x

100n C232, C233, C234, C235, C236, C237, C238, C239, C240

4x

100n C242, C257, C258, C259

10u C260, C261

GND

ROOM: CAPS_VCCAUX_2_5

VCCIO 3.3V

V3_3 — 20x

100n C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212

BANK 3 VCCIO3A-D PINS

100n C147, C148, C157, C159, C160, C151

GND

ROOM: CAPS_VCCIO_3_3

NOTE: capacitors C147, C148, C157, C159, C160, C 151 moved from 2.5V to 3.3V!

VCCPD 3.3V

V3_3 — 10x

100n C213, C183, C184, C185, C186, C187, C188, C189, C190, C191

GND

ROOM: CAPS_VCCPD_3_3

POWcpld18 — LDO 1.8V for CPLD, WR CLOCK SWITCH

V3_3 — VIN, BIAS, SHDN, VOUT, ADJ, GND, GNDP — LTC3025EDC

C53 100n; 30K1 R9; 8K45 R10; C54 100n, C56 10u, C57 1u, C55 100n; V1_8; L1 BLM18PG121; V1_8_CLEAN; TP11; C58 10u

GND

POW_1_5 — LDO 1.5V for VCCH_GXB VCCD_FPLL, VCC_BAT

V3_3 — VIN, BIAS, SHDN, VOUT, ADJ, GND, GNDP — LTC3025EDC

C77 100n; 30K1 R15; 10K7 R16; C78 100n, C80 10u, C81 1u, C79 100n; VCCD1V5; TP12; J_VCCD1V5; JMP_V2; VCCD_1_5

GND

ROOM: POWER_LDO

POWVLC5 — LDO 5.0V for LCD

V12_0 — IN1, IN2, IN3, VCON, OUT1, OUT2, OUT3, EPAD, SET — LT3080EDD

C73 100n; R14 510K; C74 100n, C76 10u, C75 100n; TP13; VLC5J; J_VLC5; JMP_V2; VLC5

GND

POWVLC9 — LDO 9.0V for LCD

V12_0 — IN1, IN2, IN3, VCON, OUT1, OUT2, OUT3, EPAD, SET — LT3080EDD

C69 100n; R13 806K; C70 100n, C72 10u, C71 100n; TP14; VLC9

GND

ROOM: POWER_LCD_LDO

IND1

V2_5 — BLM31PG121SN1L — VCCAUX_2_5

C61 100n, C62 10u

GND

IND2

V1_1 — BLM31PG121SN1L — VCCP_1_1

C63 100n, C64 10u

GND

IND3

V1_15 — BLM31PG121SN1L — VCXLR_1_15

C65 100n, C66 10u

GND

IND4

V1_15 — BLM31PG121SN1L — VCXT_1_15

C67 100n, C68 10u

GND

ROOM: POWER_FILTERS

LED_5

VLC5 — R32 2K — LR QH9PG

GND

LED_33

V3_3 — R33 1K5 — LR QH9PG

GND

LED_18

V3_3 — R21 10K — LR QH9PG — MMBT3904 Q1 — R22 1K — R20 22K

GND

LED_115

V3_3 — R23 10K — LR QH9PG — MMBT3904 Q2 — R24 1K — R25 22K

V1_15

GND

LED_11

V3_3 — R26 10K — LR QH9PG — MMBT3904 Q3 — R27 1K — R28 22K

V1_1

GND

LED_15

V3_3 — R29 10K — LR QH9PG — MMBT3904 Q4 — R30 1K — R31 22K

VCCD_1_5

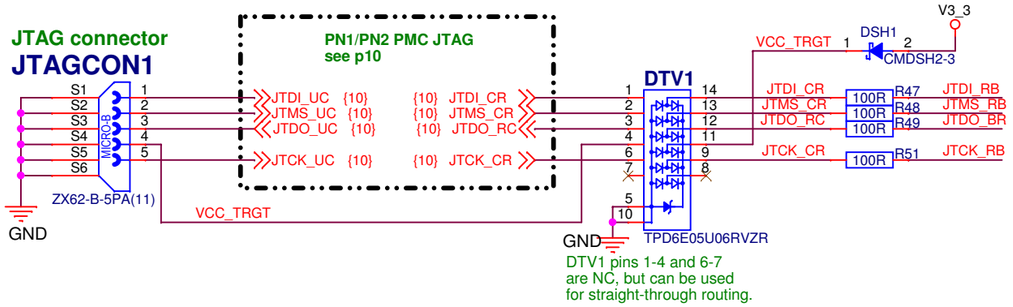
GND

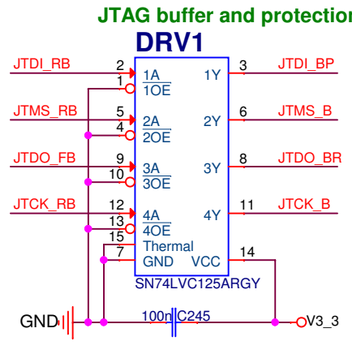
ROOM: POWER_INDICATORS

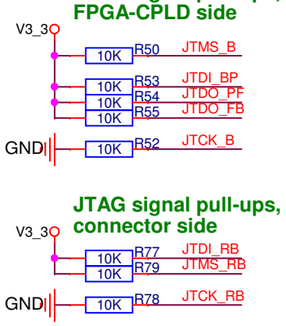
Title	FPGA decoupling, LDO regulators, power indicators		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
			SHEET 5 OF 13

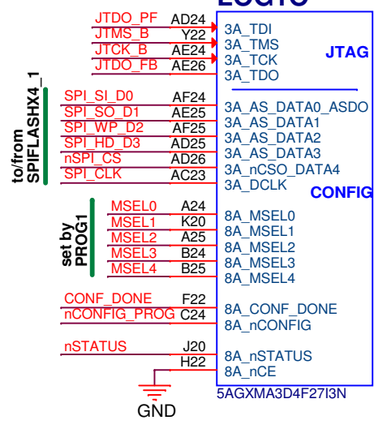
FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash

USB connector JTAG signals flow : U (USB connector) > C (PMC connector) > R (resistor) > B (buffer) > P (PROG - CPLD) > F (FPGA) > B > C > U
JTAGCON1 and PN1/PN2 JTAG signals are connected in parallel!

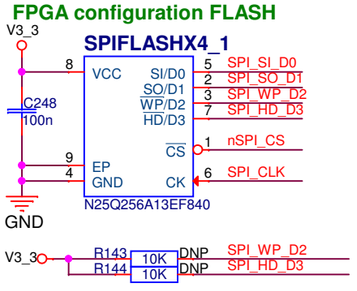


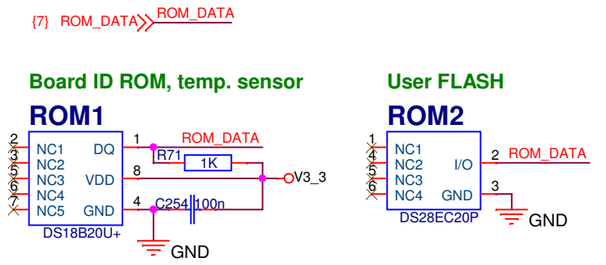




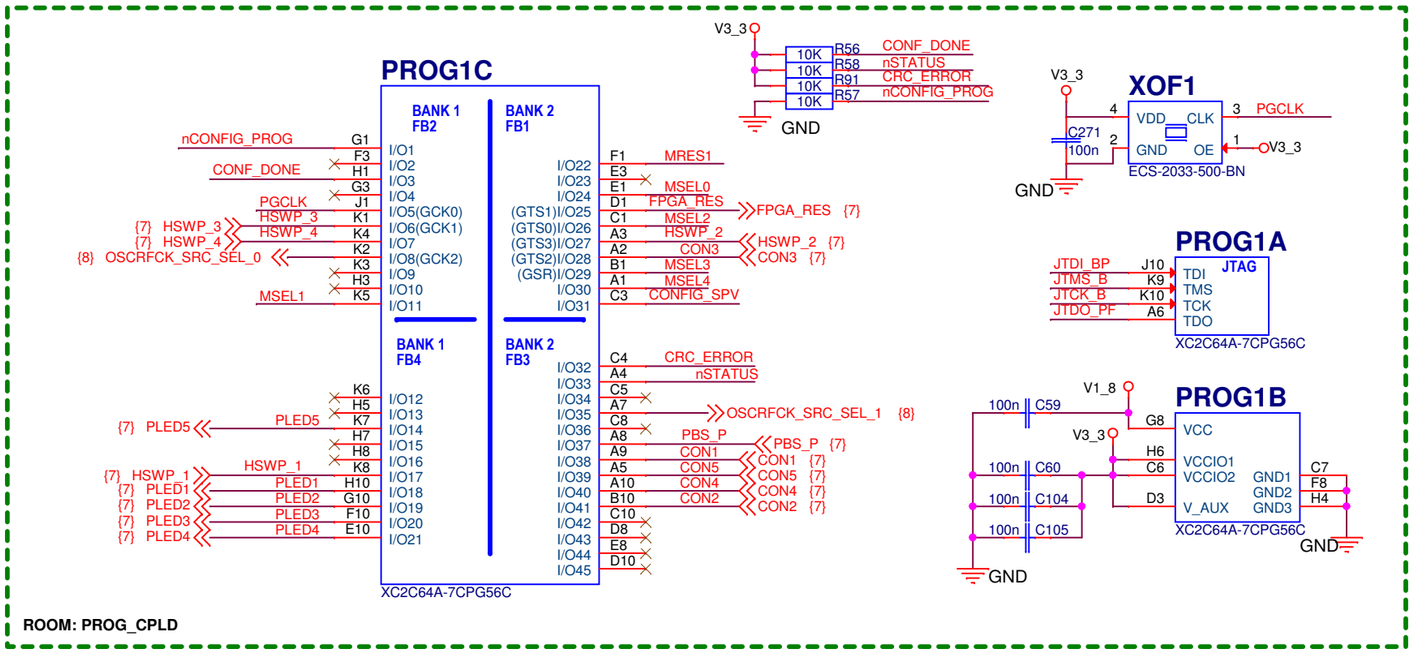


ROOM: JTAG_INPUT

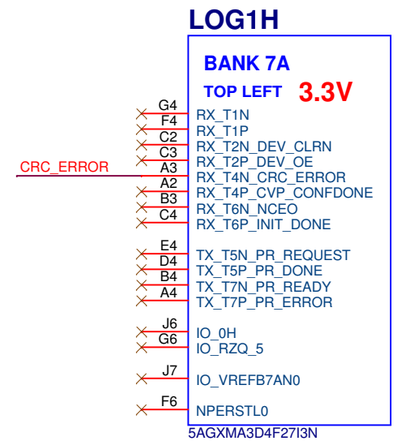


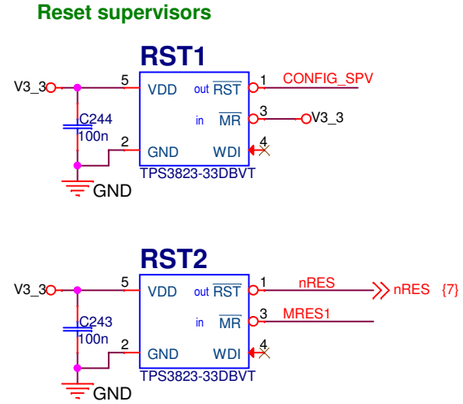


ROOM: MEMORY



ROOM: PROG_CPLD

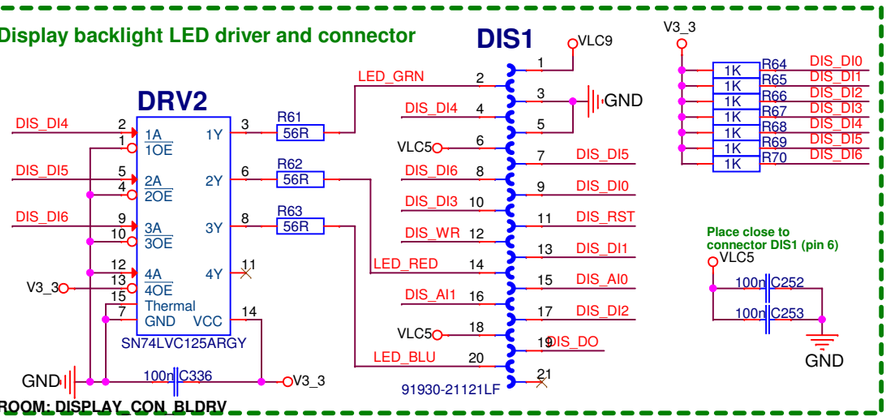




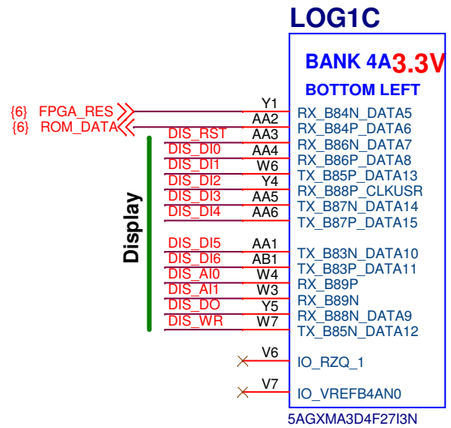
Title	FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
		SHEET 6 OF 13	

User interface - USB, Display, push buttons, HEX switch, LEDs

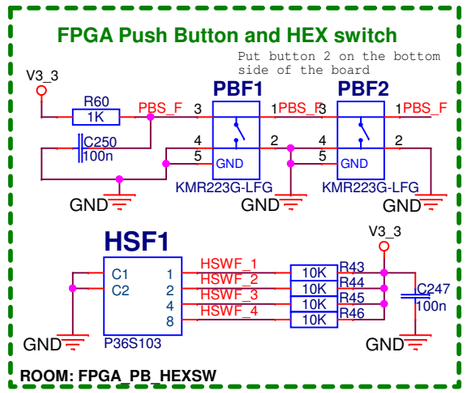
Display backlight LED driver and connector



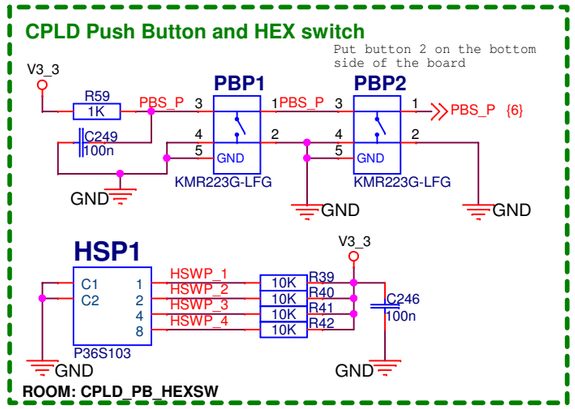
LOG1C



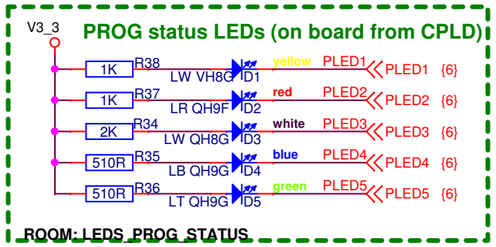
FPGA Push Button and HEX switch



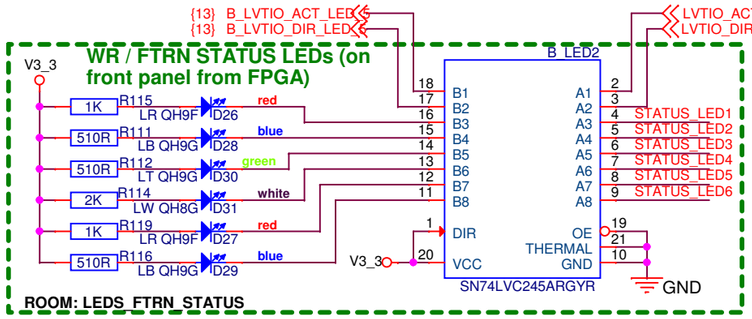
CPLD Push Button and HEX switch



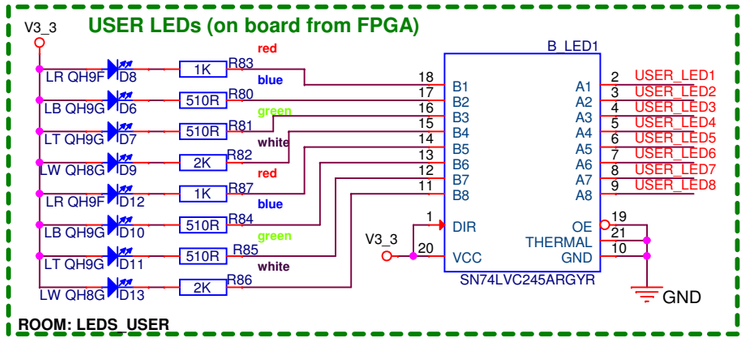
PROG status LEDs (on board from CPLD)



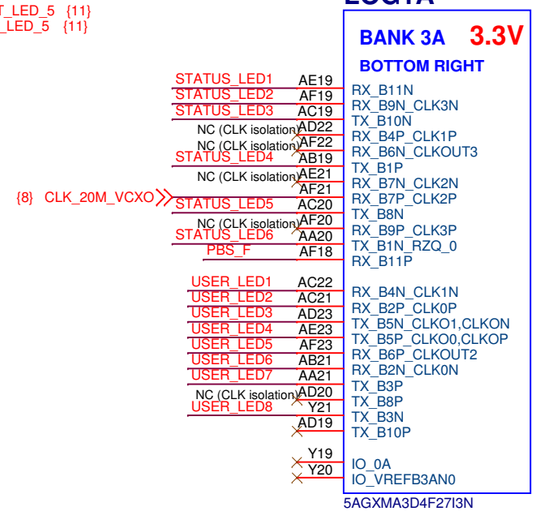
WR / FTRN STATUS LEDs (on front panel from FPGA)



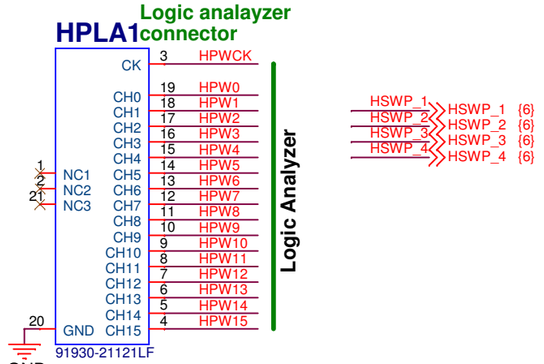
USER LEDs (on board from FPGA)



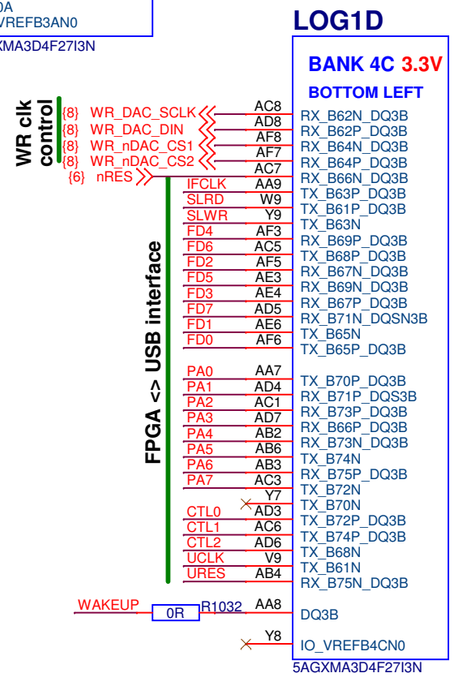
LOG1A



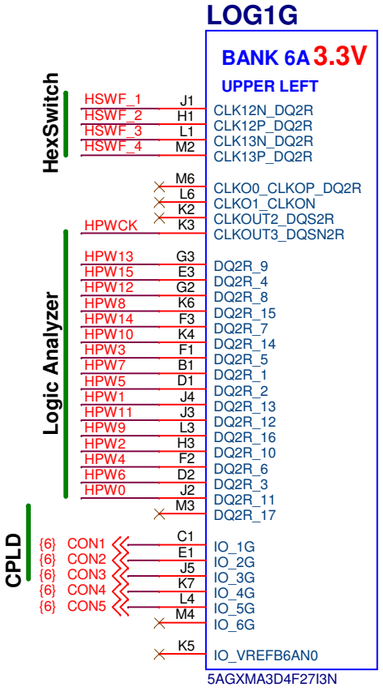
Logic analayzer connector



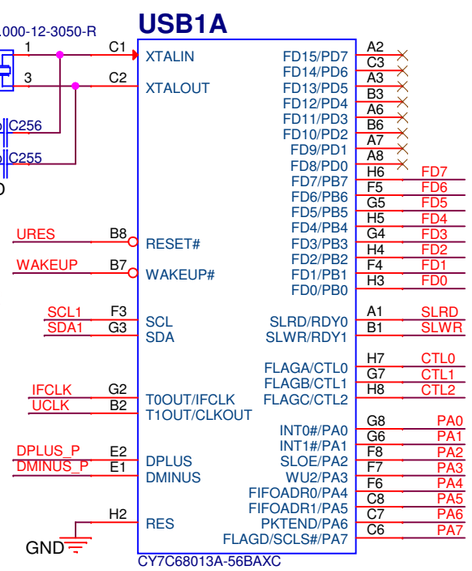
LOG1D



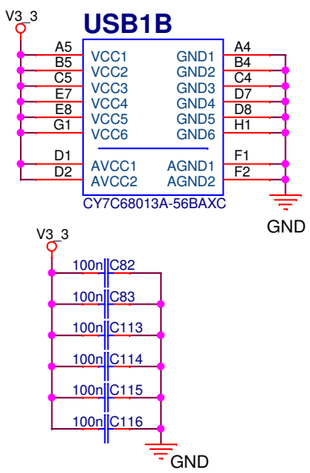
LOG1G



USB1A

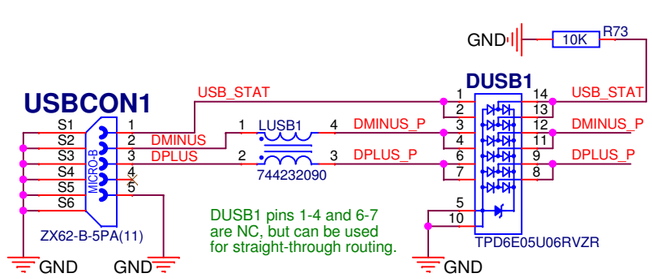


USB1B



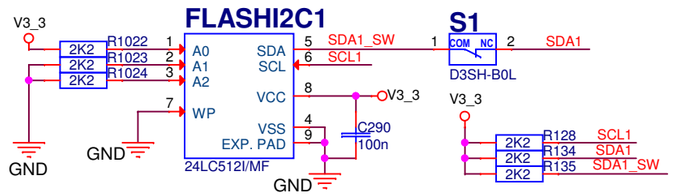
IMPORTANT! (USB1B)
Connect AGND to GND with as short a path as possible!

USBCON1



XTL1

FLASHI2C1



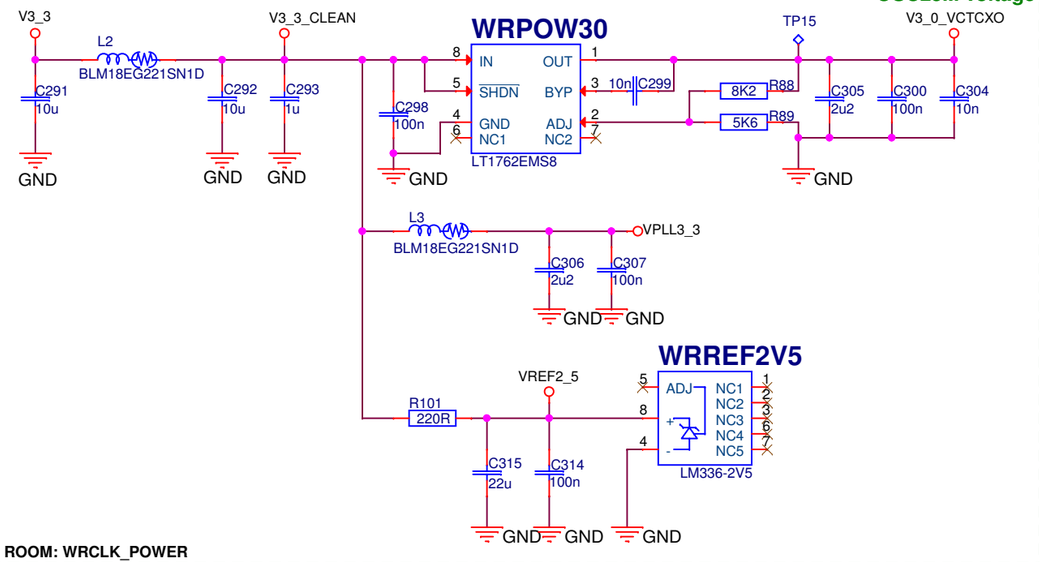
ROOM: USB_INTERFACE

Title	User interface - USB, Display, push buttons, HEX switch, LEDs		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
		SHEET 7 OF 13	

Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch

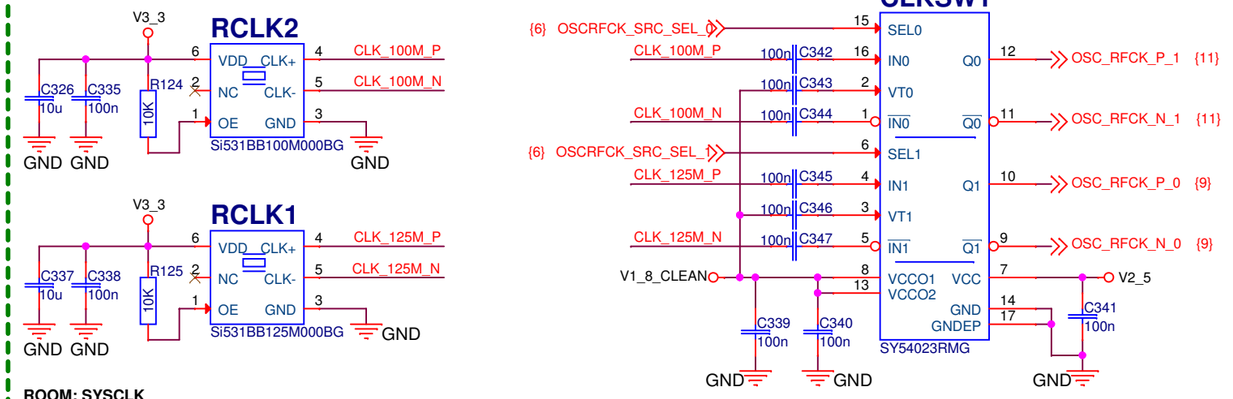
White Rabbit clocking power supply

OSC25M voltage



ROOM: WRCLK_POWER

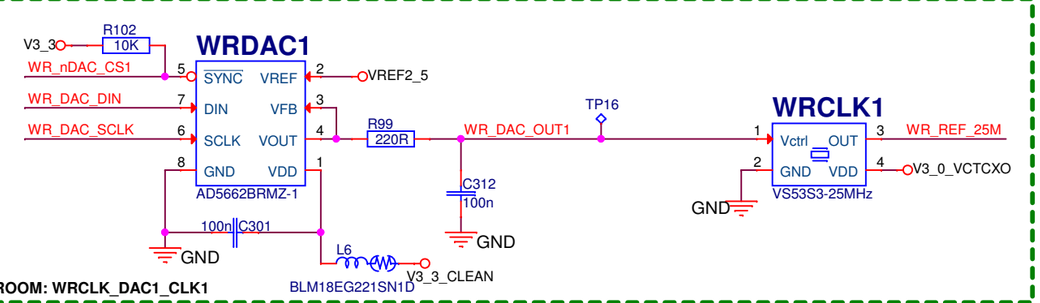
System clock oscillators with crosspoint switch



ROOM: SYSCLK

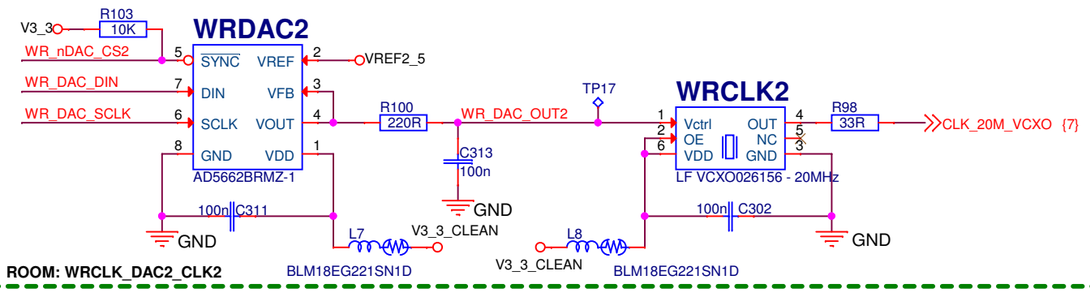
{7} WR_nDAC_CS1 → WR_nDAC_CS1
{7} WR_nDAC_CS2 → WR_nDAC_CS2
{7} WR_DAC_DIN → WR_DAC_DIN
{7} WR_DAC_SCLK → WR_DAC_SCLK

WRDAC1



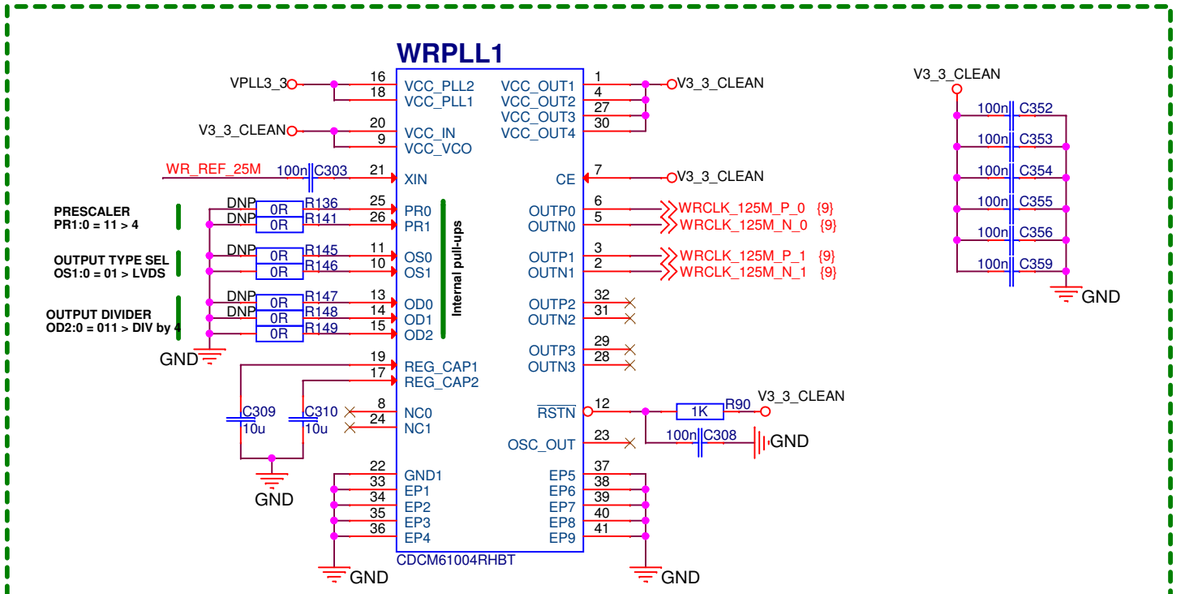
ROOM: WRCLK_DAC1_CLK1

WRDAC2



ROOM: WRCLK_DAC2_CLK2

WRPLL1

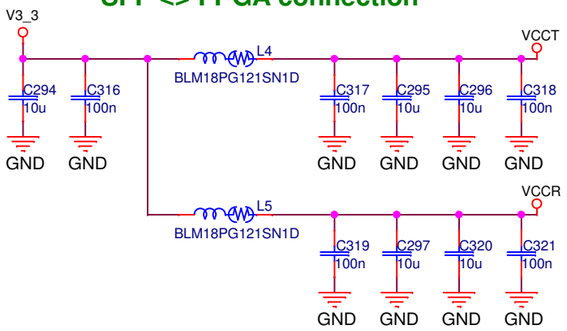


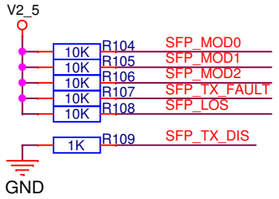
ROOM: WRCLK_PLL

Title	Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
		SHEET 8 OF 13	

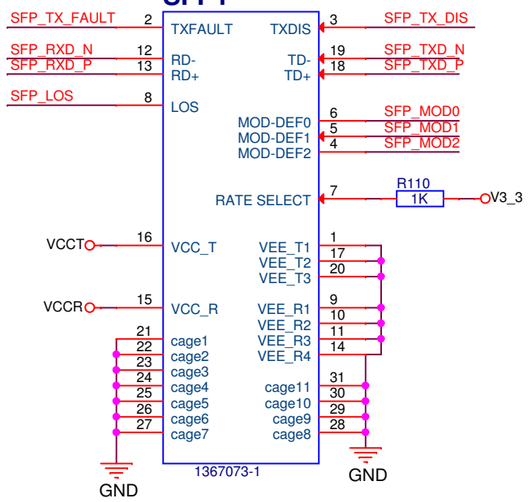
Fiber SFP, PCI <> FPGA connections

SFP <> FPGA connection

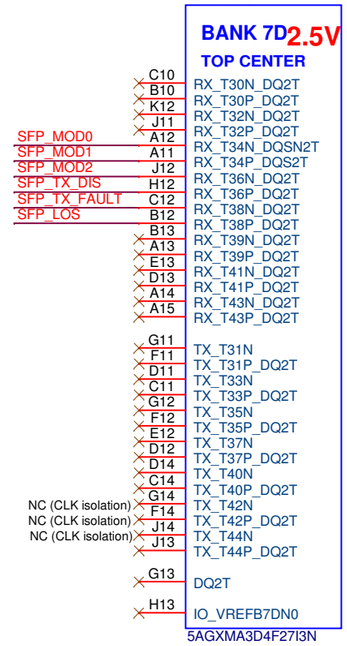




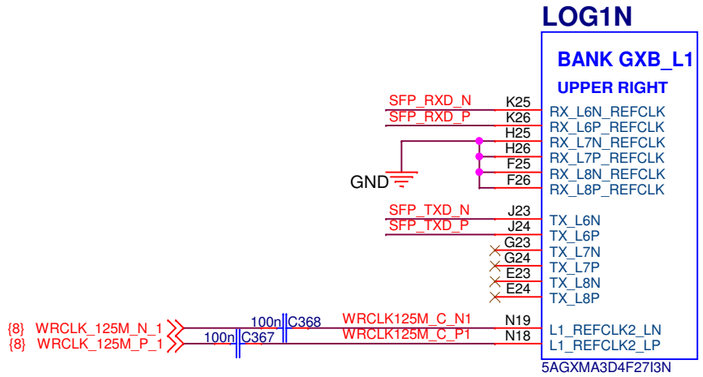
SFP1



LOG1J

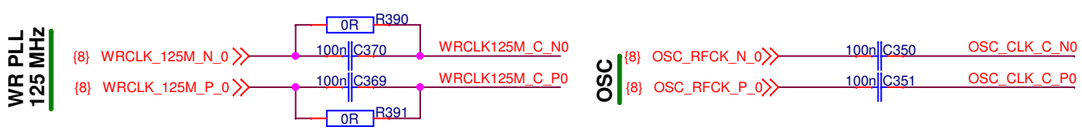


LOG1N

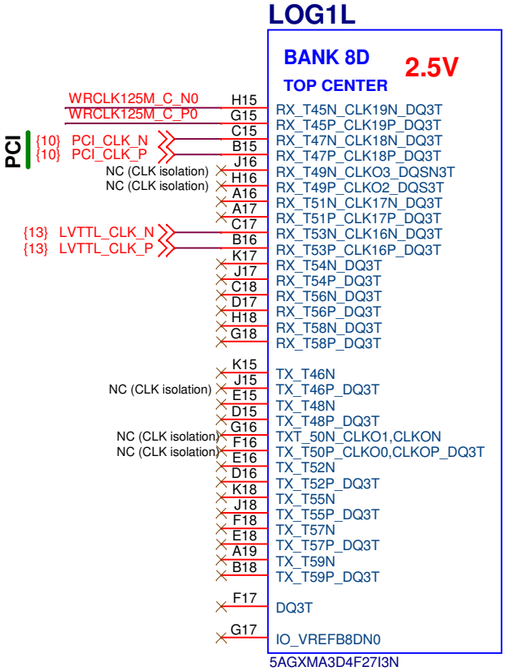


ROOM: SFP

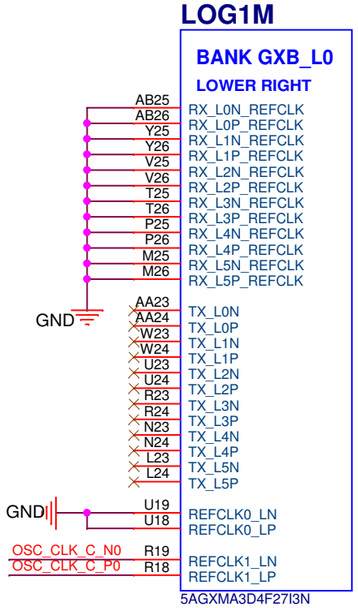
Place resistor footprint over capacitor (optional AC-coupling)
Only resistors will be placed!



LOG1L



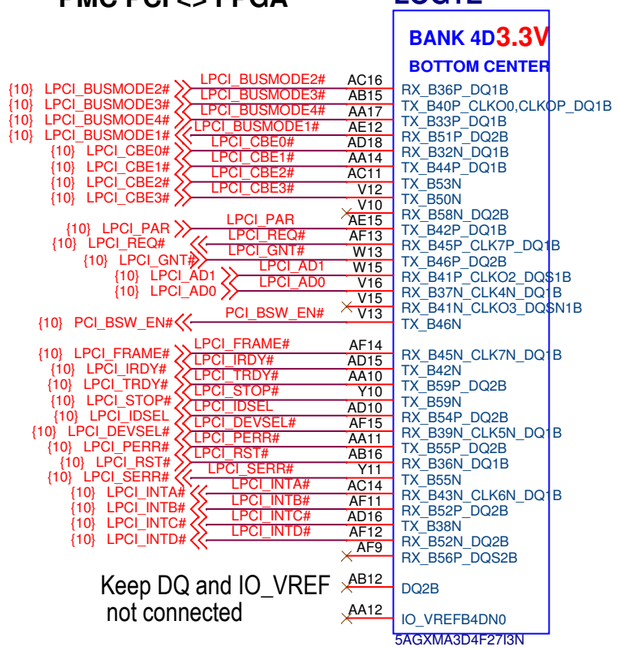
LOG1M



SWAP pins as needed inside and between banks 3D and 4D

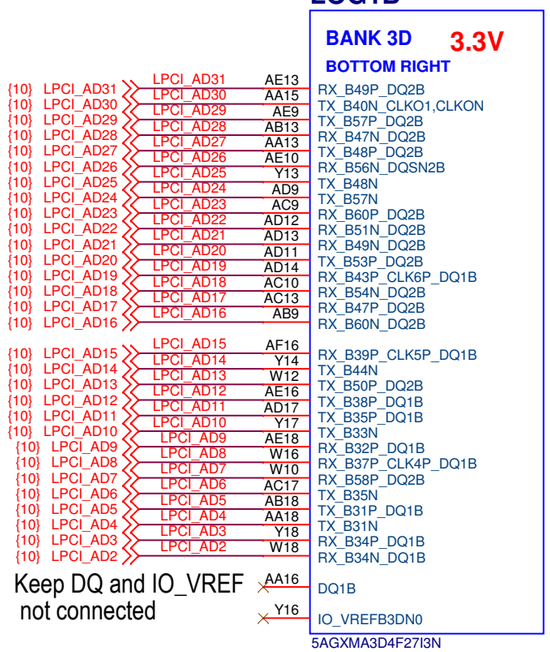
PMC PCI <> FPGA

LOG1E



Keep DQ and IO_VREF not connected

LOG1B



Keep DQ and IO_VREF not connected

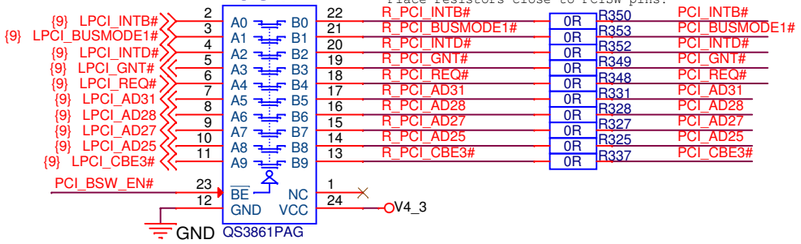
Title	Fiber SFP, PCI <> FPGA connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
		SHEET 9 OF 13	

PMC host interface

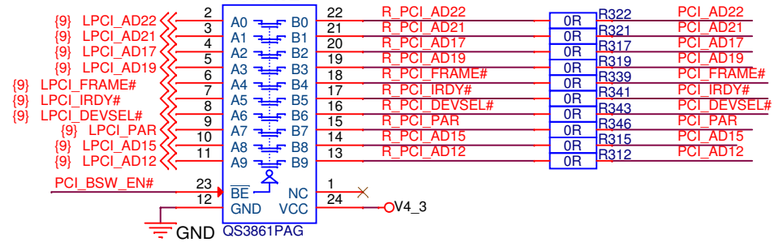
Swap as needed across bus switches for easier layout!

Place resistors close to PCISW pins!

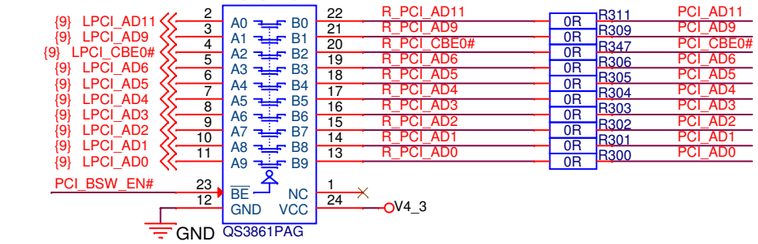
PCISW1



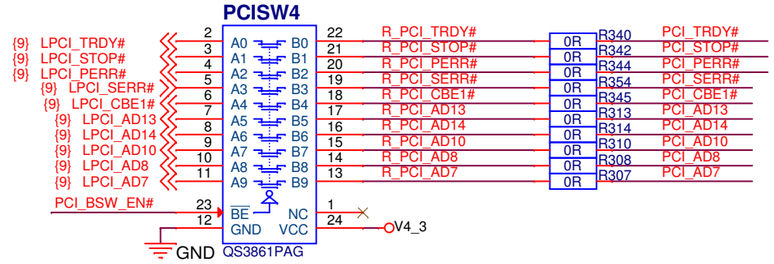
PCISW2



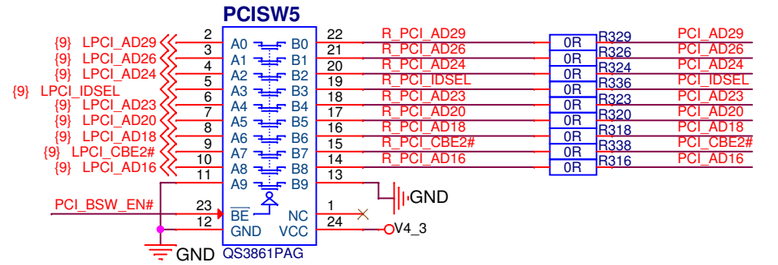
PCISW3



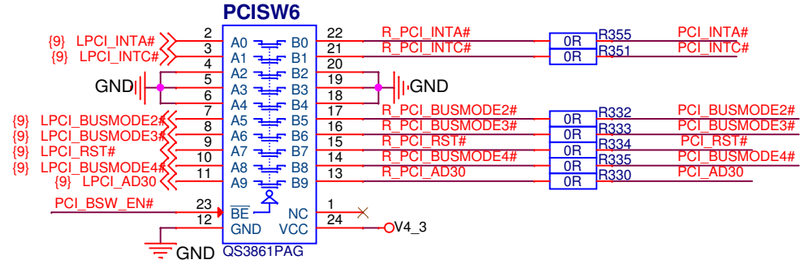
PCISW4



PCISW5

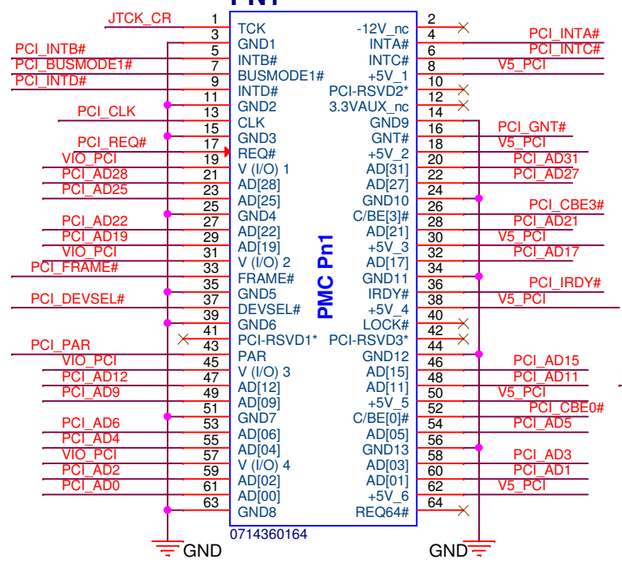


PCISW6

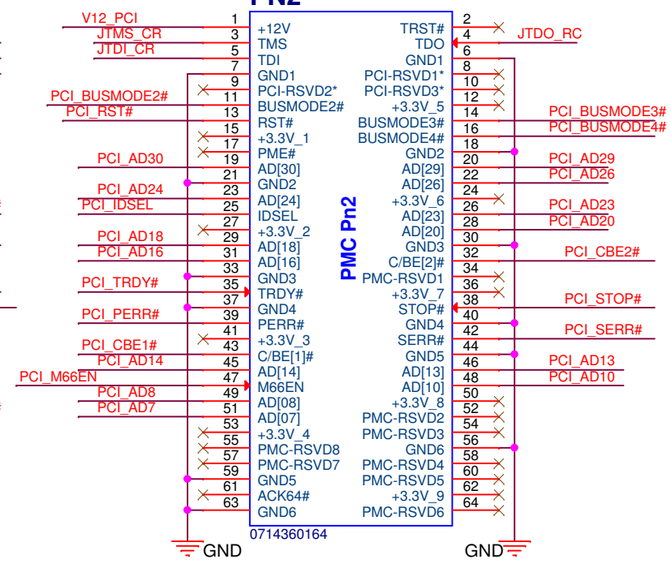


ROOM: PMC_BUFFERS

PN1

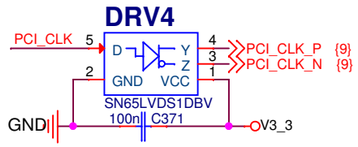


PN2

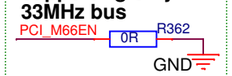


IMPORTANT! (DRV4)
Place close to connector PN1, pin 13!

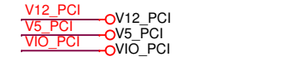
DRV4



supporting only 33MHz bus



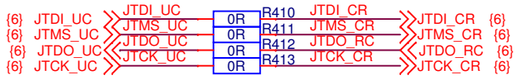
BACKPLANE POWER



ROOM: PMC

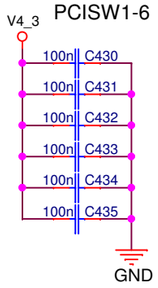
Bus switch enable (pulled low by FPGA after FPGA boot, when in user mode)

USB JTAG connector <---> PMC connector, buffer, CPLD-FGA



Place resistors close to PN1, PN2 connector pins!

PCISW1-6



VCC for bus switches, see
- https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/ds/ds_stratix_pci_bd.pdf
- https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an330.pdf

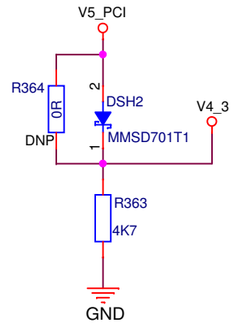
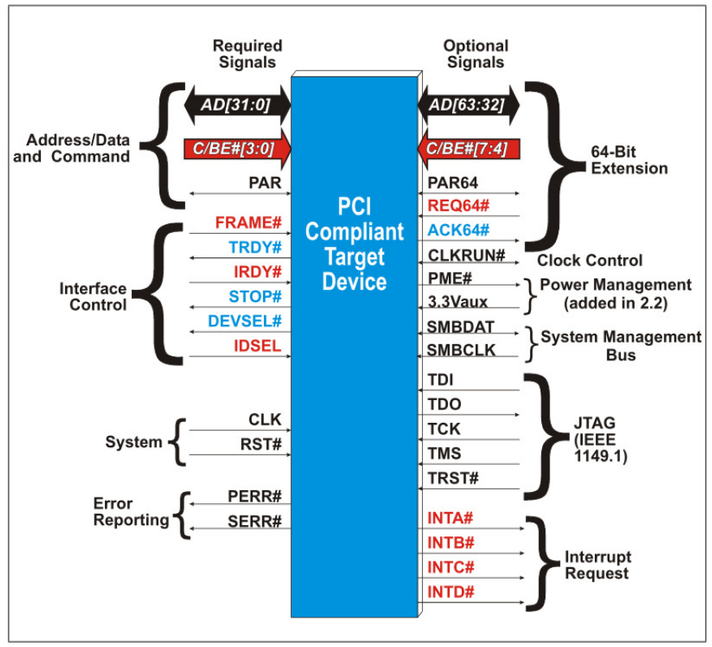


Figure 4-2: PCI-Compliant Target Device Signals



Title: PMC host interface				
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PMC	REV. B	
			SHEET 10 OF 13	

IO block power supply, FPGA <> IO block connections

{12} LVTIO_OUT_P_1 — LVTIO_OUT_P_1
{12} LVTIO_OUT_N_1 — LVTIO_OUT_N_1
{12} #LVTIO_OE_1 — #LVTIO_OE_1
{12} LVTIO_IN_P_1 — LVTIO_IN_P_1
{12} LVTIO_IN_N_1 — LVTIO_IN_N_1
{12} LVTIO_TERM_EN_1 — LVTIO_TERM_EN_1
{12} LVTIO_DIR_LED_1 — LVTIO_DIR_LED_1
{12} LVTIO_ACT_LED_1 — LVTIO_ACT_LED_1

{12} LVTIO_OUT_P_2 — LVTIO_OUT_P_2
{12} LVTIO_OUT_N_2 — LVTIO_OUT_N_2
{12} #LVTIO_OE_2 — #LVTIO_OE_2
{12} LVTIO_IN_P_2 — LVTIO_IN_P_2
{12} LVTIO_IN_N_2 — LVTIO_IN_N_2
{12} LVTIO_TERM_EN_2 — LVTIO_TERM_EN_2
{12} LVTIO_DIR_LED_2 — LVTIO_DIR_LED_2
{12} LVTIO_ACT_LED_2 — LVTIO_ACT_LED_2

{12} LVTIO_OUT_P_3 — LVTIO_OUT_P_3
{12} LVTIO_OUT_N_3 — LVTIO_OUT_N_3
{12} #LVTIO_OE_3 — #LVTIO_OE_3
{12} LVTIO_IN_P_3 — LVTIO_IN_P_3
{12} LVTIO_IN_N_3 — LVTIO_IN_N_3
{12} LVTIO_TERM_EN_3 — LVTIO_TERM_EN_3
{12} LVTIO_DIR_LED_3 — LVTIO_DIR_LED_3
{12} LVTIO_ACT_LED_3 — LVTIO_ACT_LED_3

{13} LVTIO_OUT_P_4 — LVTIO_OUT_P_4
{13} LVTIO_OUT_N_4 — LVTIO_OUT_N_4
{13} #LVTIO_OE_4 — #LVTIO_OE_4
{13} LVTIO_IN_P_4 — LVTIO_IN_P_4
{13} LVTIO_IN_N_4 — LVTIO_IN_N_4
{13} LVTIO_TERM_EN_4 — LVTIO_TERM_EN_4
{12} LVTIO_DIR_LED_4 — LVTIO_DIR_LED_4
{12} LVTIO_ACT_LED_4 — LVTIO_ACT_LED_4

{13} LVTIO_OUT_P_5 — LVTIO_OUT_P_5
{13} LVTIO_OUT_N_5 — LVTIO_OUT_N_5
{13} #LVTIO_OE_5 — #LVTIO_OE_5
{13} LVTIO_IN_P_5 — LVTIO_IN_P_5
{13} LVTIO_IN_N_5 — LVTIO_IN_N_5
{13} LVTIO_TERM_EN_5 — LVTIO_TERM_EN_5
{7} LVTIO_DIR_LED_5 — LVTIO_DIR_LED_5
{7} LVTIO_ACT_LED_5 — LVTIO_ACT_LED_5

LOG1F

BANK 5A
LOWER LEFT
3.3V

LVTTL IO control signals

#LVTIO_OE_1	N5	DQ1R_1
LVTIO_TERM_EN_1	P1	DQ1R_2
LVTIO_ACT_LED_1	P3	DQ1R_3
LVTIO_DIR_LED_1	R2	DQ1R_4
#LVTIO_OE_2	R3	DQ1R_5
LVTIO_TERM_EN_2	R6	DQ1R_6
LVTIO_ACT_LED_2	T1	DQ1R_7
LVTIO_DIR_LED_2	T2	DQ1R_8
#LVTIO_OE_3	T3	DQ1R_9
LVTIO_TERM_EN_3	T6	DQ1R_10
LVTIO_ACT_LED_3	U1	DQ1R_12
LVTIO_DIR_LED_3	T7	DQ1R_11
#LVTIO_OE_4	U5	DQ1R_13
LVTIO_TERM_EN_4	V1	DQ1R_14
LVTIO_ACT_LED_4	V4	DQ1R_15
LVTIO_DIR_LED_4	V5	DQ1R_16
#LVTIO_OE_5	W1	DQ1R_17
LVTIO_TERM_EN_5	W2	DQ1R_18
LVTIO_ACT_LED_5	N6	IO_1F
LVTIO_DIR_LED_5	P4	IO_2F
#LVTTL_IN_CLK_EN	P6	IO_3F
	R5	IO_4F
	T4	IO_5F
	U6	IO_6F
	V2	IO_7F
	U3	DQSN1R
	V3	DQS1R
	U7	IO_VREFB5AN0

{13} #LVTTL_IN_CLK_EN

5AGXMA3D4F27I3N

LOG1I

BANK 7C
TOP LEFT
2.5V

LVTTL IO data inputs

LVTIO_IN_N_1	A6	RX_T19N_DQSN1T
LVTIO_IN_P_1	A5	RX_T19P_DQS1T
LVTIO_IN_N_2	C6	RX_T21N_DQ1T
LVTIO_IN_P_2	B6	RX_T21P_DQ1T
LVTIO_IN_N_3	E6	RX_T15N_DQ1T
LVTIO_IN_P_3	D6	RX_T15P_DQ1T
LVTIO_IN_N_4	F7	RX_T17N_DQ1T
LVTIO_IN_P_4	E7	RX_T17P_DQ1T
LVTIO_IN_N_5	H9	RX_T23N_DQ1T
LVTIO_IN_P_5	G9	RX_T23P_DQ1T
	D8	RX_T24N_DQ1T
	C8	RX_T24P_DQ1T
	E9	RX_T26N_DQ1T
	D9	RX_T26P_DQ1T
	H10	RX_T28N_DQ1T
	G10	RX_T28P_DQ1T

LVTTL IO data outputs

LVTIO_OUT_N_1	A9	TX_T25N
LVTIO_OUT_P_1	A8	TX_T25P_DQ1T
LVTIO_OUT_N_2	C7	TX_T22N
LVTIO_OUT_P_2	B7	TX_T22P_DQ1T
LVTIO_OUT_N_3	D5	TX_T18N
LVTIO_OUT_P_3	C5	TX_T18P_DQ1T
LVTIO_OUT_N_4	G8	TX_T20N
LVTIO_OUT_P_4	F8	TX_T20P_DQ1T
LVTIO_OUT_N_5	J8	TX_T16N
LVTIO_OUT_P_5	J9	TX_T16P_DQ1T
	K10	TX_T27N
	J10	TX_T27P_DQ1T
	C9	TX_T29N
	B9	TX_T29P_DQ1T
	E10	DQ1T
	F10	IO_VREFB7CN0

5AGXMA3D4F27I3N

Power supply for output drivers

V_MAIN
100K R130
100n C329
GND
PRUN_3V3_IO
10K R133
PGOOD_3V3_IO
red D17
LR QH9F
GND

POWIO33A

H5	RUN/SS	AUX	F5
		BIAS	G5
H6	PGOOD	SYNC	G6
		ADJ	H7
F7	SHARE	R_T	G7

10K R132
154K R131
49K9 R129
GND
LTM8023EV

POWIO33B

V_MAIN
C331 100n
C330 10u
GND GND

G1	V_IN1	V_OUT1	A1
G2	V_IN2	V_OUT2	A2
G3	V_IN3	V_OUT3	A3
H1	V_IN4	V_OUT4	A4
H2	V_IN5	V_OUT5	B1
H3	V_IN6	V_OUT6	B2
		V_OUT7	B3
		V_OUT8	B4
		V_OUT9	C1
		V_OUT10	C2
		V_OUT11	C3
		V_OUT12	C4

LTM8023EV

ODRV
TP18
C332 22u
GND
JODRV_V33
JMP_V2
V33_ODRV
C333 100u
C334 100u
GND GND

POWIO33C

A5	GND1	GND24	F6
A6	GND2	GND23	E7
A7	GND3	GND22	E6
B5	GND4	GND21	E5
B6	GND5	GND20	E4
B7	GND6	GND19	E3
C5	GND7	GND18	E2
C6	GND8	GND17	E1
C7	GND9	GND16	D7
D1	GND10	GND15	D6
D2	GND11	GND14	D5
D3	GND12	GND13	D4

GND GND
LTM8023EV

ROOM: IO_POWER

LOG1K

BANK 8A
TOP RIGHT
2.5V

A23	RX_T86N_CLK21N	
B22	RX_T86P_CLK21P	
A21	TX_T82P	
D21	TX_T89P	
E21	TX_T89N_RZO_6	
G21	TX_T85P_CLKO0,CLKOP	
A20	RX_T81P_CLK23P	
C19	RX_T79P	
H19	TX_T87P	
D20	RX_T84N_CLKOUT3	
C22	RX_T88N_CLK20N	
C23	RX_T88P_CLK20P	
B19	RX_T81N_CLK23N	
F19	TX_T80N	
E19	TX_T80P	
J19	TX_T87N	
B21	RX_T83P_CLK22P	
D19	RX_T79N	
H21	TX_T85N_CLKO1,CLKON	
A22	TX_T82N	
C21	RX_T83N_CLK22N	
C20	RX_T84P_CLKOUT2	
F20	IO_0K	
G20	IO_VREFB8AN0	

5AGXMA3D4F27I3N

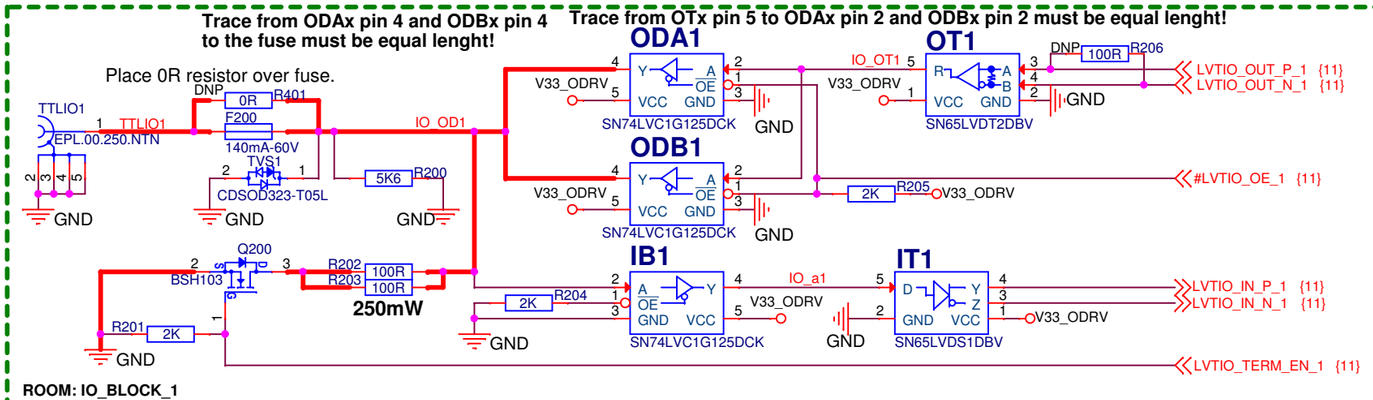
Place resistor footprint over capacitor (optional AC-coupling)
Only resistors will be placed!

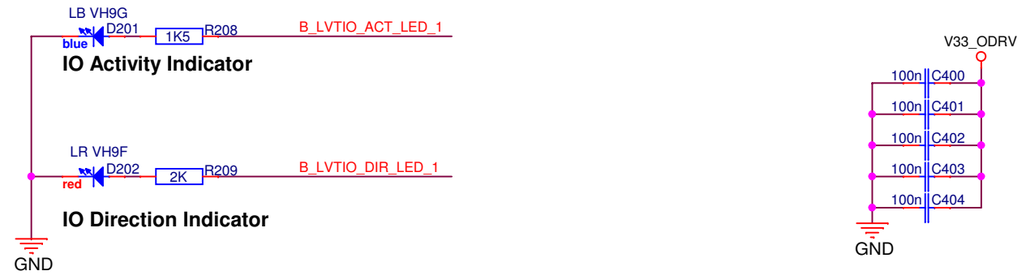
OSC
{8} OSC_RFCK_N_1
{8} OSC_RFCK_P_1
0R R392
100n C358
100n C357
0R R393
OSC_RFCK_C_N1
OSC_RFCK_C_P1

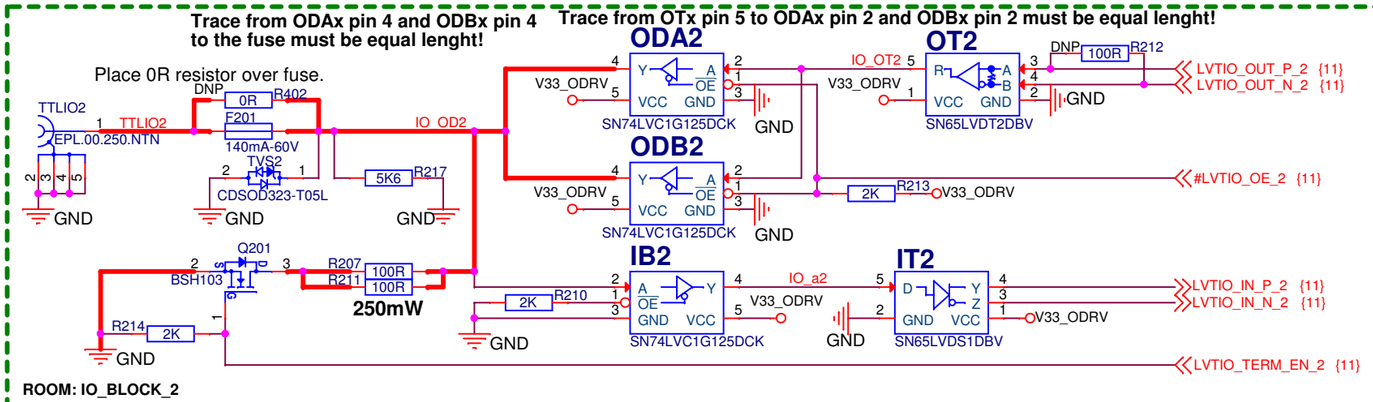
* - IO overvoltage protection bias circuit is based OHWR FMC-DIO-5CHTTLA

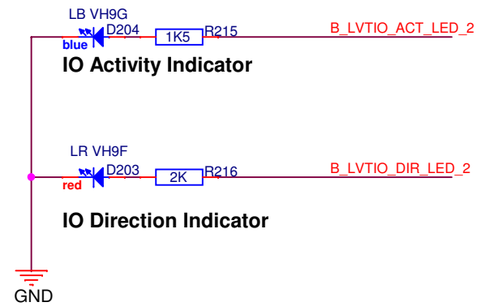
Title	IO block power supply, FPGA <> IO block connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
		SHEET 11 OF 13	

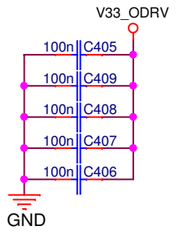
LVTTL IO blocks 1-3

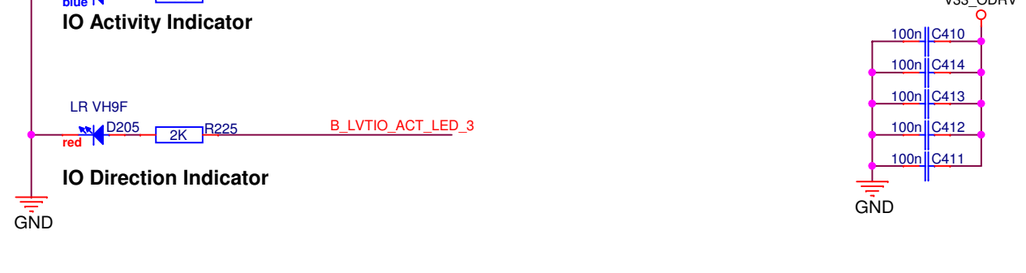




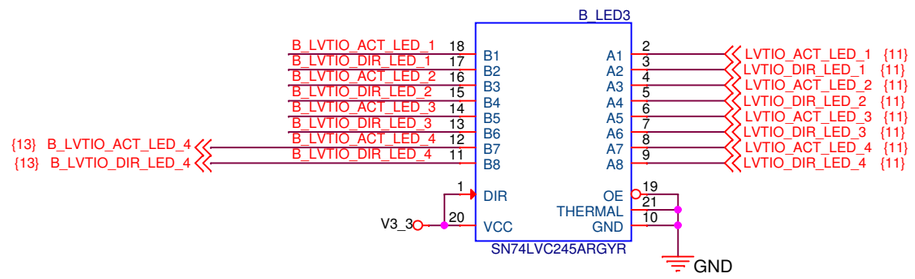






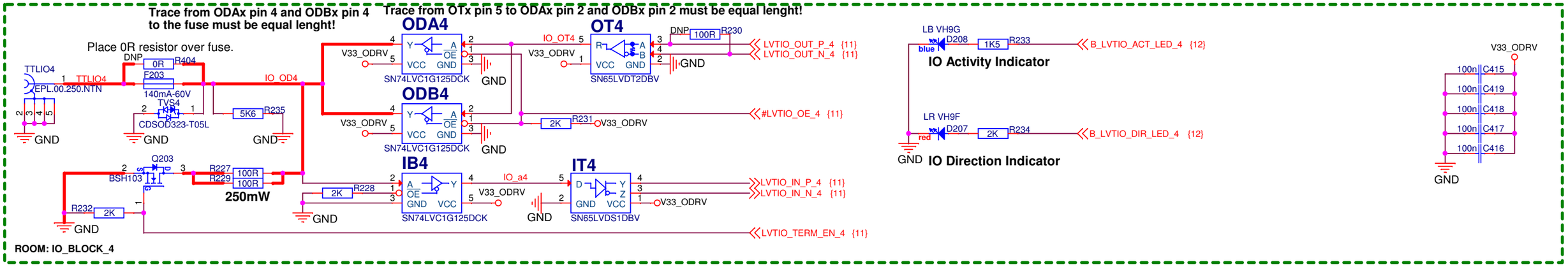


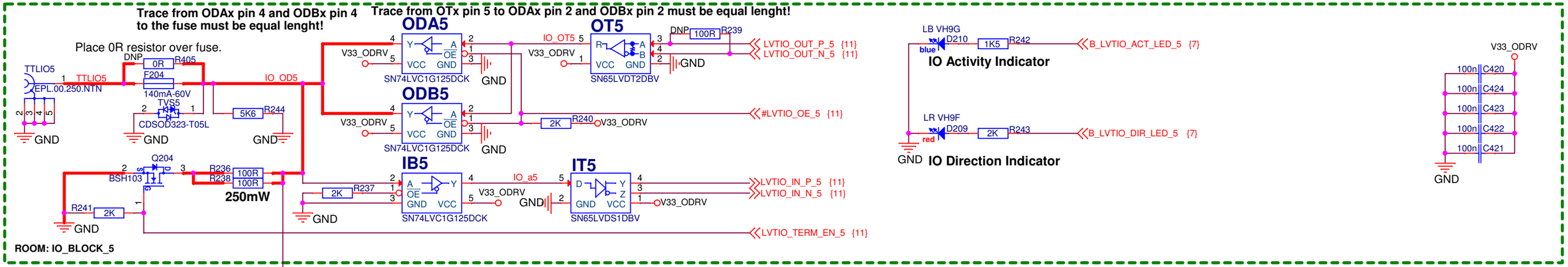
— Z = 50R !

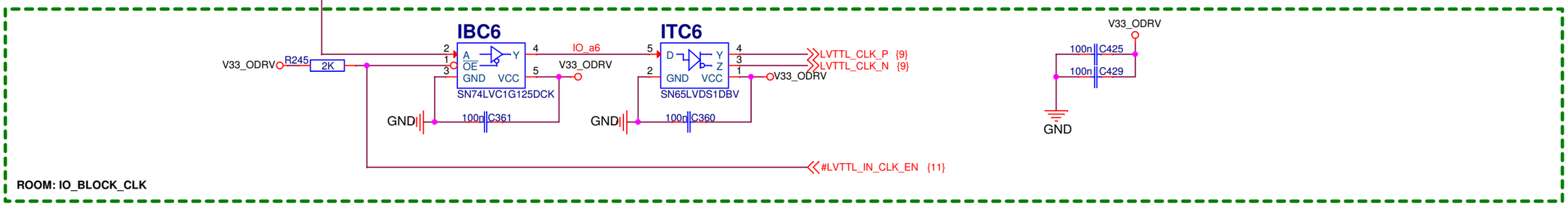


Title	LVTTL IO blocks 1-3		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
		SHEET 12 OF 13	

LVTTL IO blocks 4-5, IO CLOCK input







Z = 50R !

Title	LVTTL IO blocks 4-5, IO CLOCK input		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. B
		SHEET 13 OF 13	