FAIR Timing Receiver (FTRN) PMC form factor - CSL_FTRN_PMC

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Value	Capatitors used
12p	0402, 50V, C0G, 1%
22p	0402, 50V, C0G, 1%
10n	0402, 25V, X7R, 10%
100n	0402, 25V, X7R, 10%
1u	0603, 16V, X7R, 10%
2.2u	1210, 100V, X7R, 10%
10u	1210, 25V, X7R, 10%
22u	1210, 10V, X7R, 10%
100u	1210, 10V, X5R, 20%

All resistors are SMD 0402, 63mW, 1% except where marked differently.

Components marked DNP (Do Not Place) are foreseen for testing purposes.

TOP layer

FM1 FIDUCIAL FM2 FIDUCIAL FM3 FIDUCIAL

BOTTOM layer

FM4 FIDUCIAL FM5 FIDUCIAL FM6 FIDUCIAL

DATE	REVISION DESCRIPTION	DRAWN	REV
04.12.2014	Initial version	dslavinec	A
21.4.2015	Added fixes found during HDL synthesis check and changes during PCB layout	dslavinec, bpecnik	A
21.5.2015	PCB layout ready for review	dslavinec, bpecnik	A

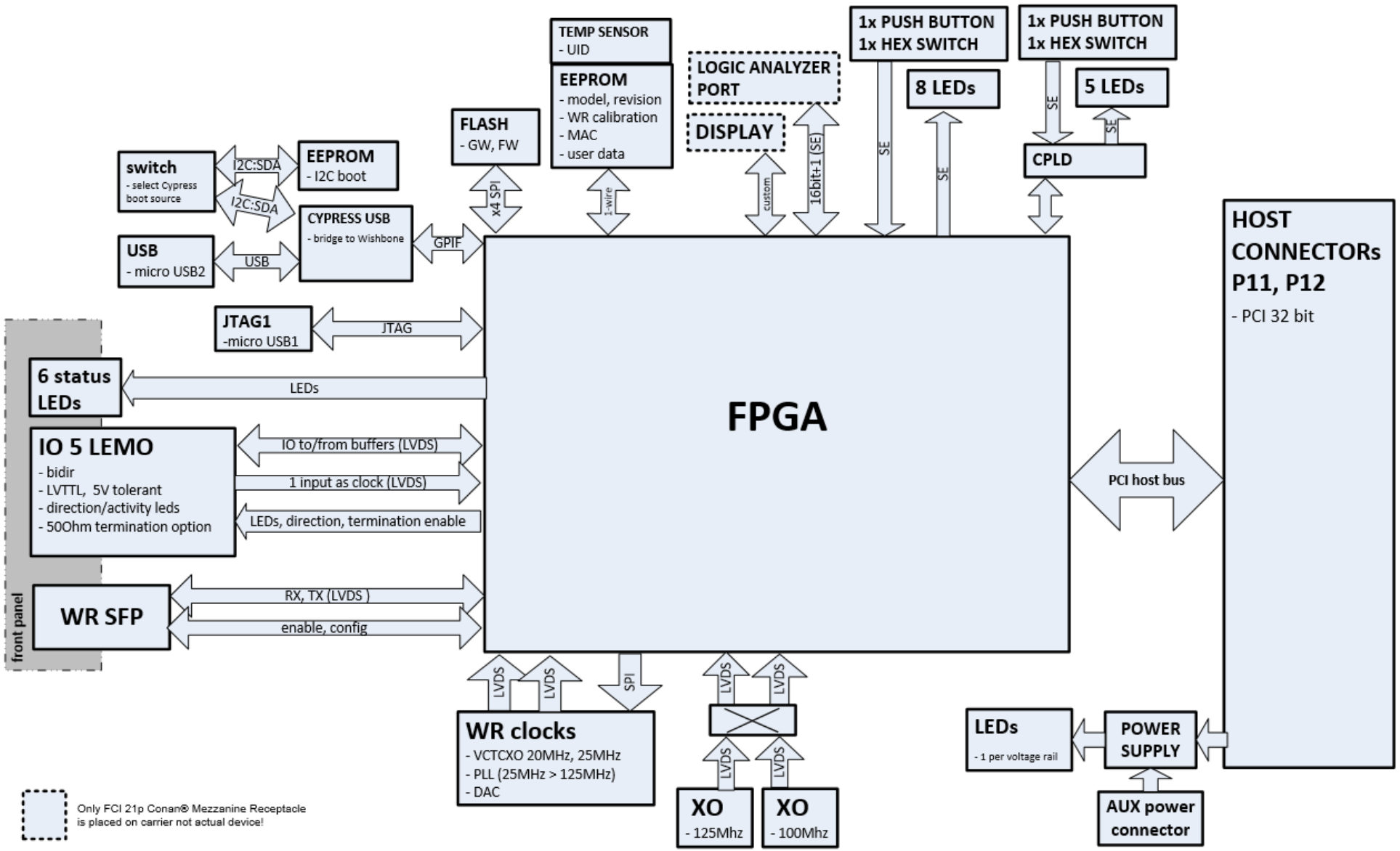
DRAWN	Dušan Slavinec		04.12.2014
CHECKED	-		
APPROVED	-		

Title: FAIR Timing Receiver (FTRN) PMC form factor - CSL_FTRN_PMC

Size: A3 | Type: SE | DWG.NO.: CSL_FTRN_PMC | REV.: A

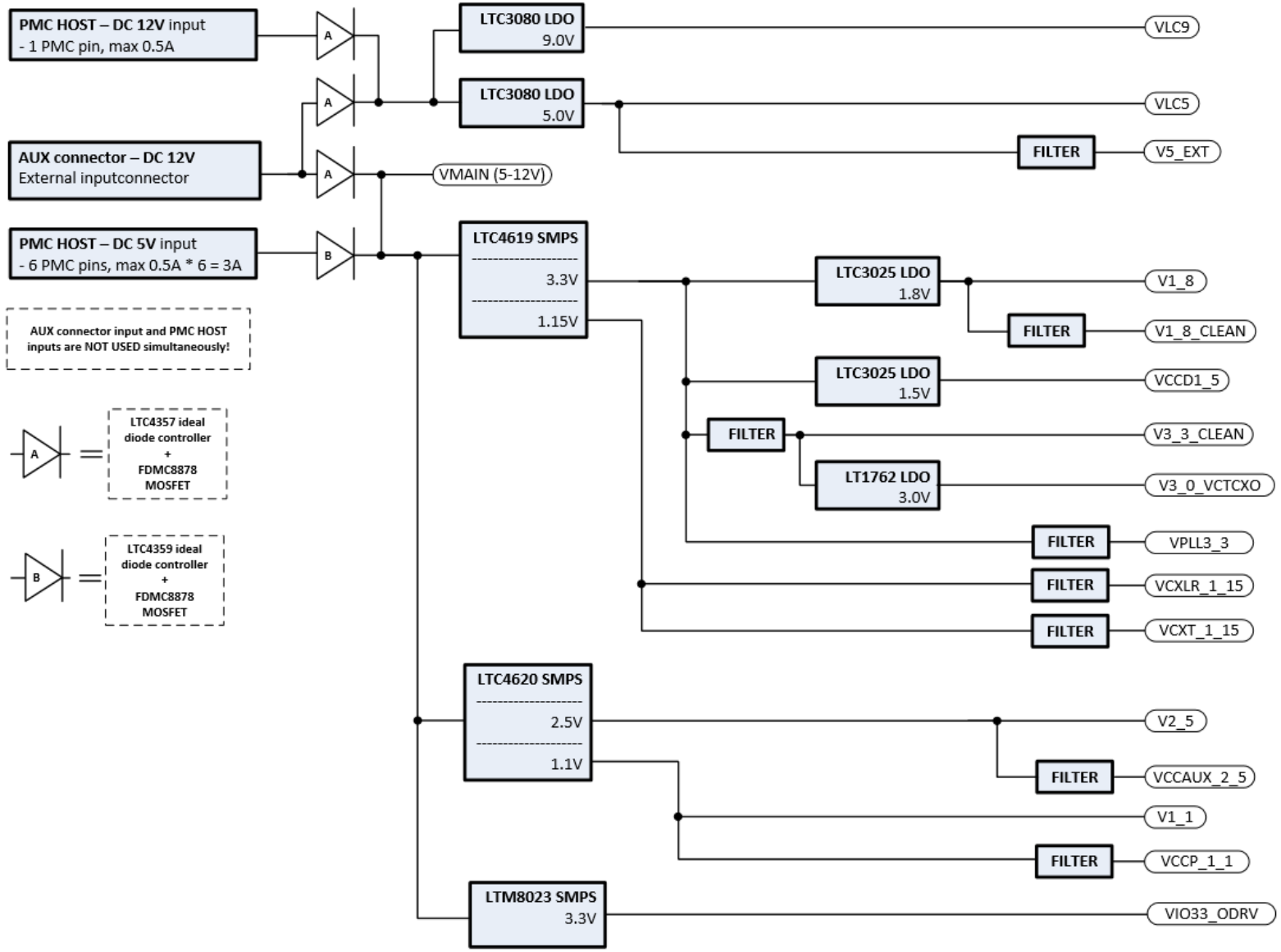
SHEET 1 OF 13

Block Diagram



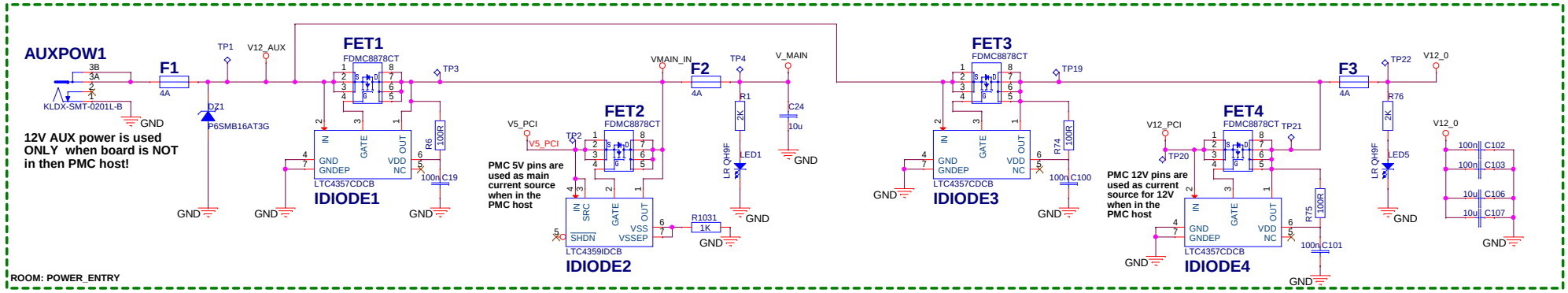
Title: Block Diagram			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PMC	REV. A
			SHEET 2 OF 13

Power tree block scheme

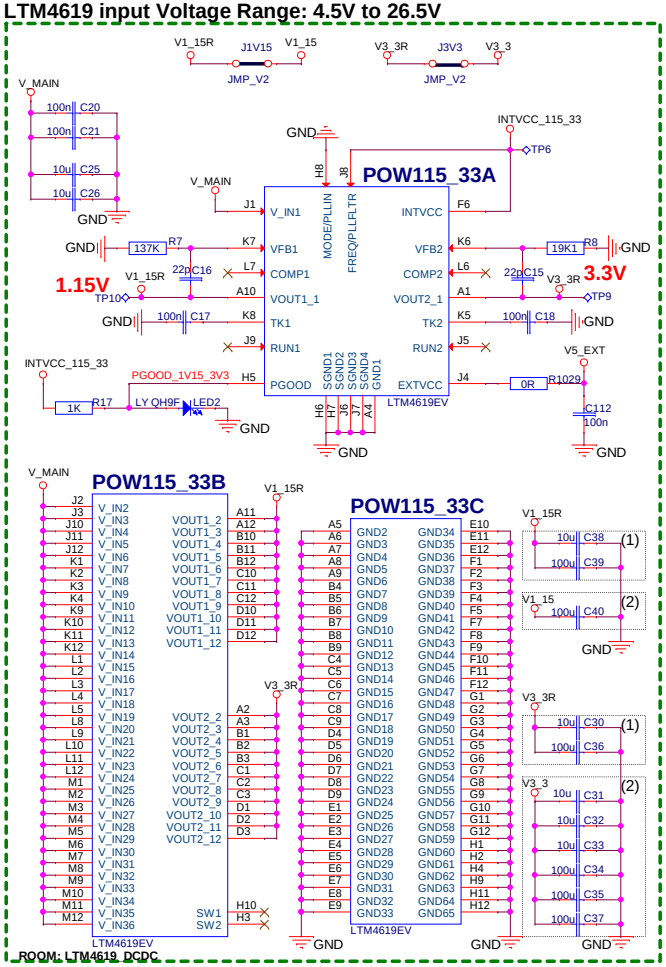


Title	Power tree block scheme		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. A
			SHEET 3 OF 13

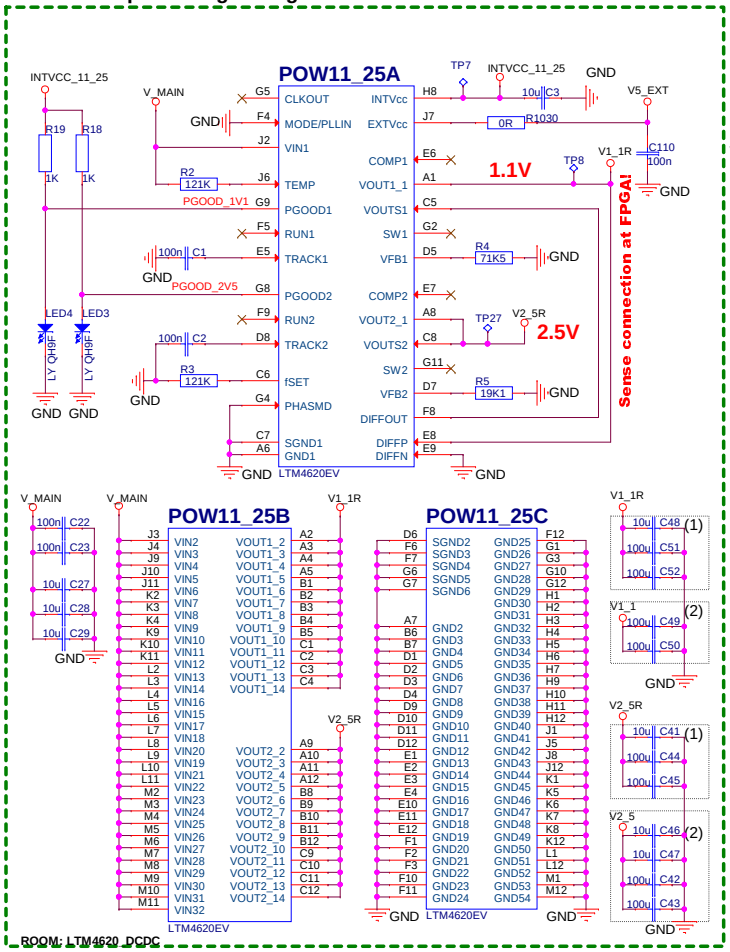
Power entry and main DCDC power regulators

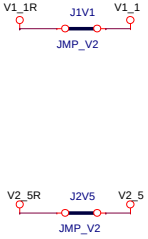


LTM4619 input Voltage Range: 4.5V to 26.5V

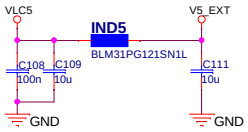


LTM4620 input Voltage Range: 4.5V to 16V





5V power for LTM4619 and LTM4620 EXTVCC

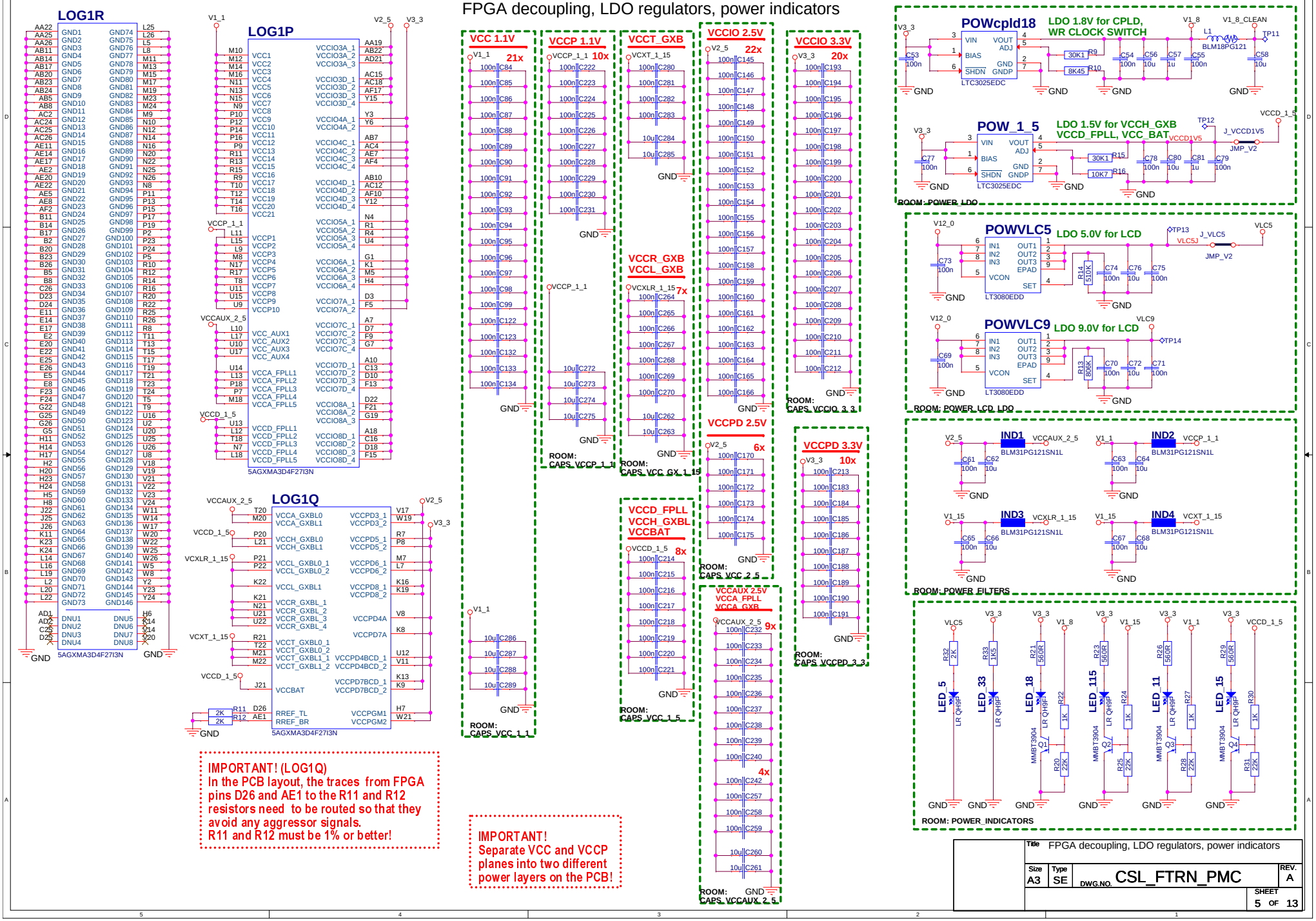


(1) - place capacitors on the regulator outputs

(2) - place capacitors away from the regulator outputs

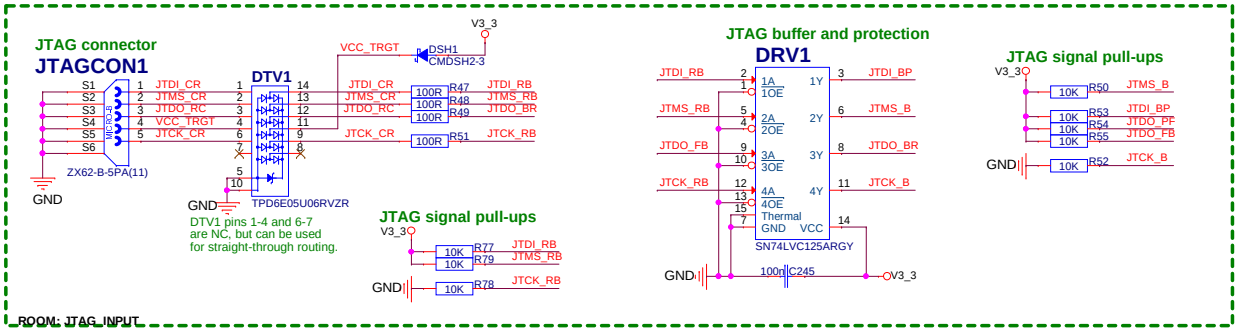
Title: Power entry and main DCDC power regulators			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PMC	REV. A
			SHEET 4 OF 13

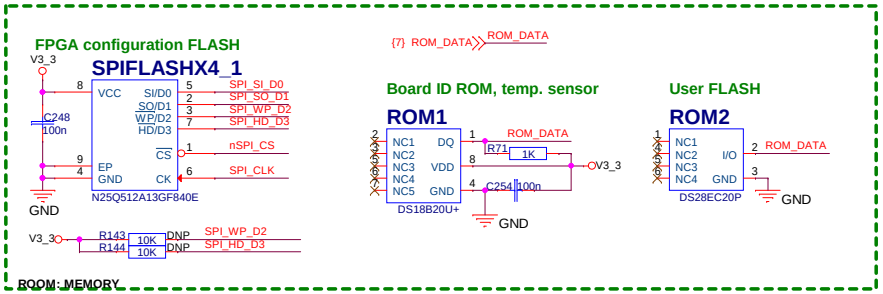
FPGA decoupling, LDO regulators, power indicators

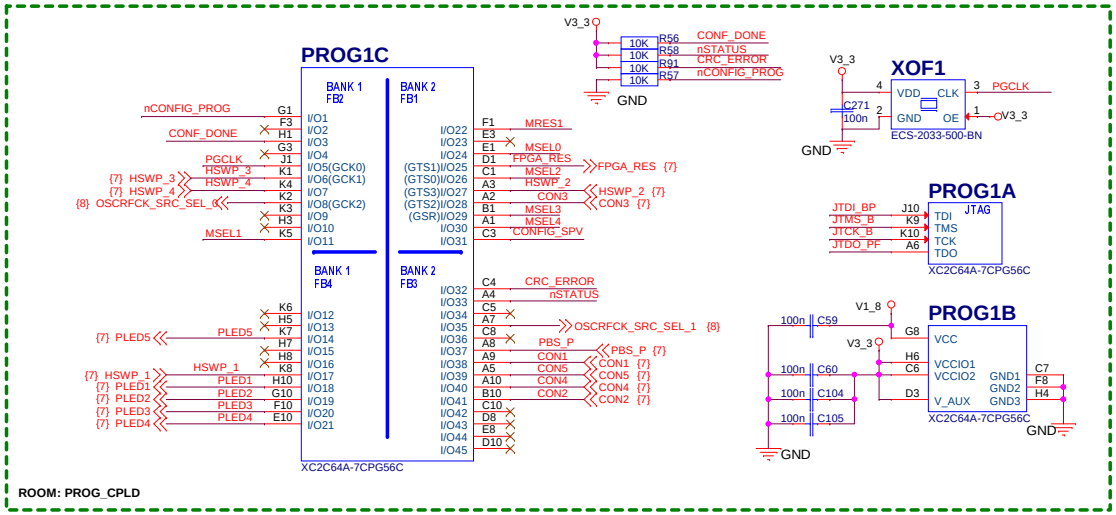


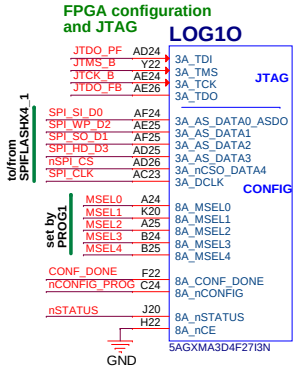
FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash

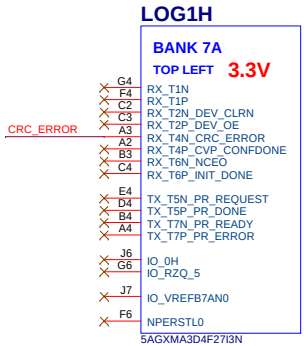
USB connector JTAG signals flow : C (connector) > R (resistor) > B (buffer) > P (PROG - CPLD) > F (FPGA) > B > C

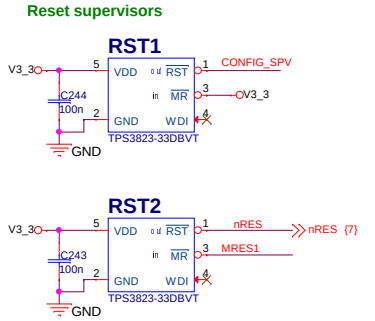






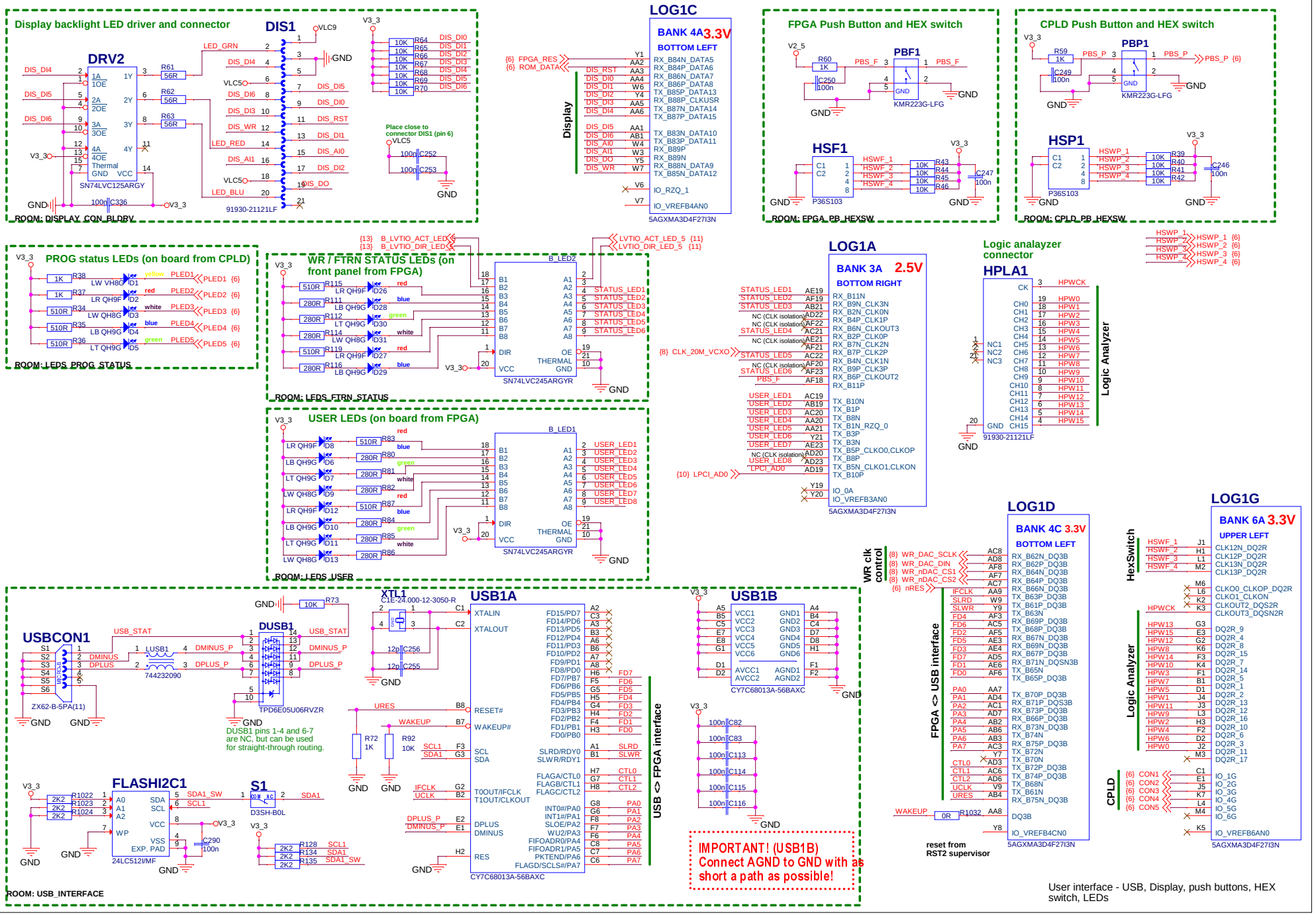




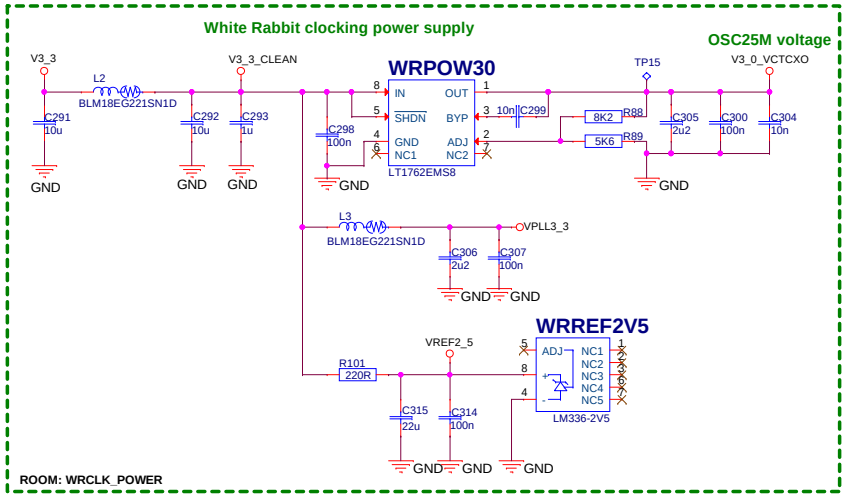


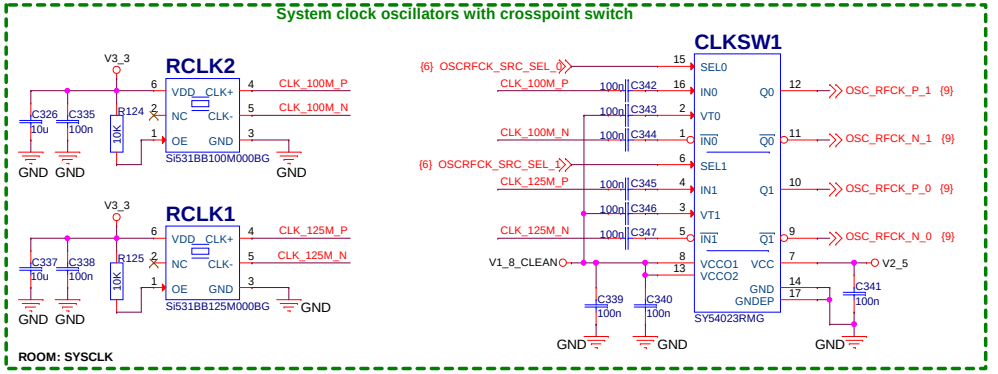
Title	FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. A
		SHEET 6 OF 13	

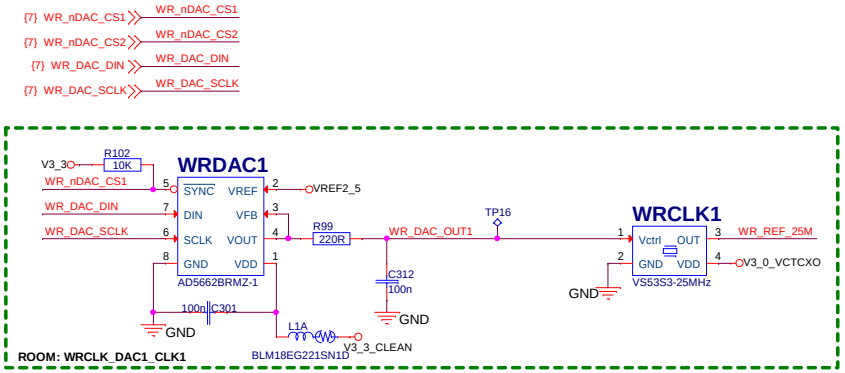
User interface - USB, Display, push buttons, HEX switch, LEDs

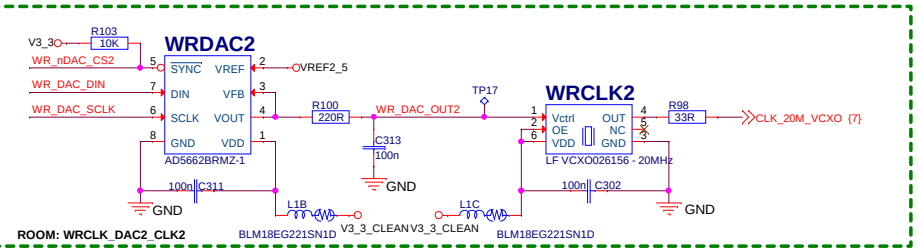


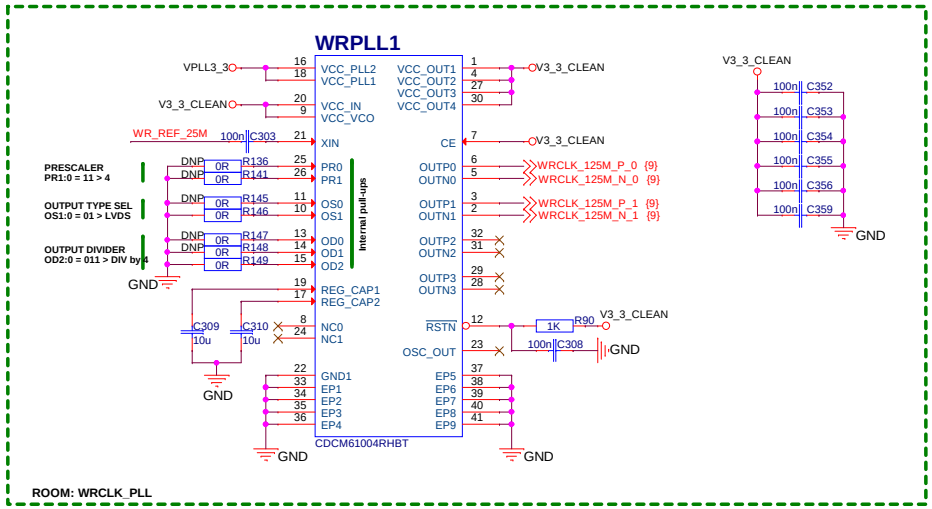
Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch





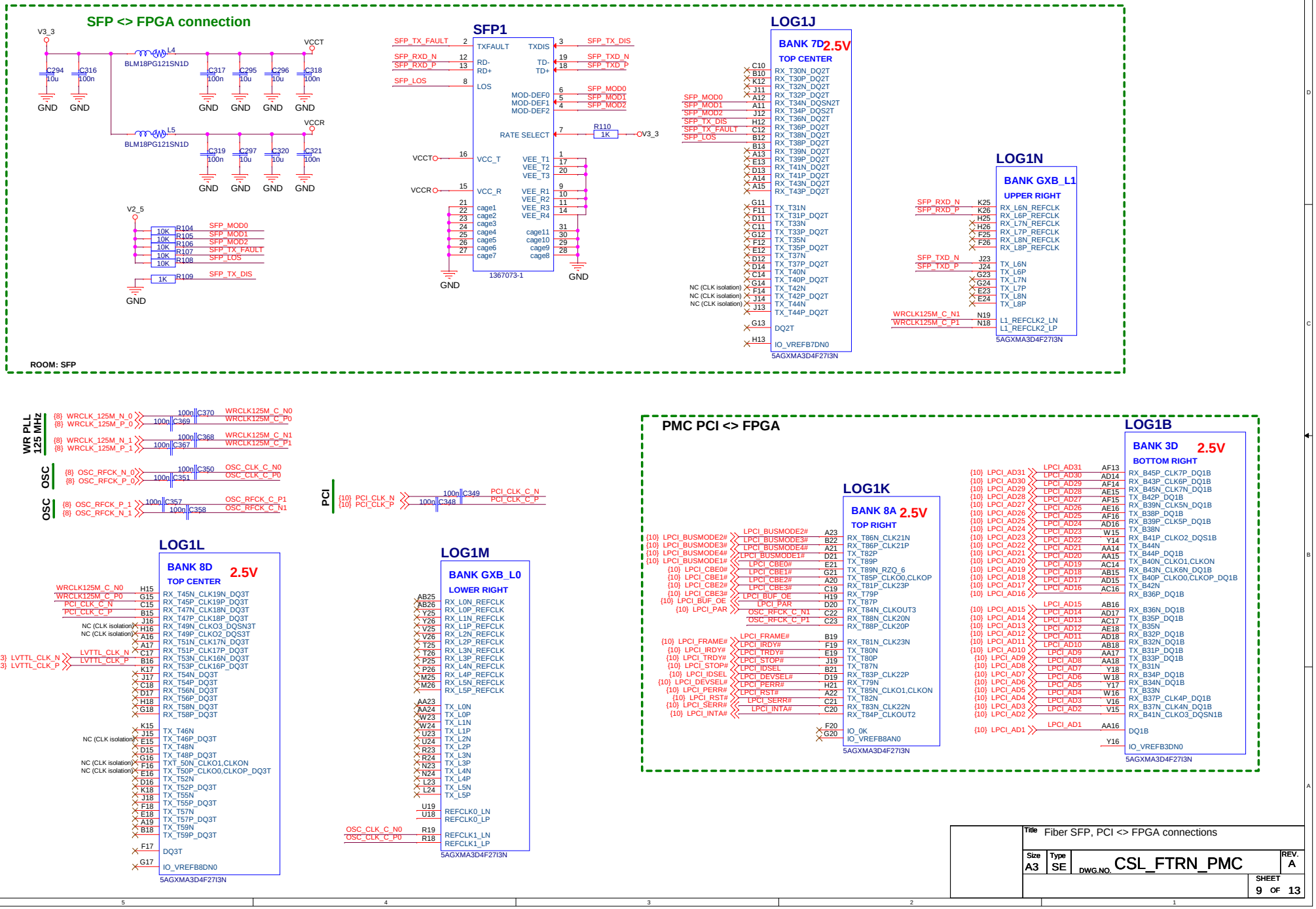




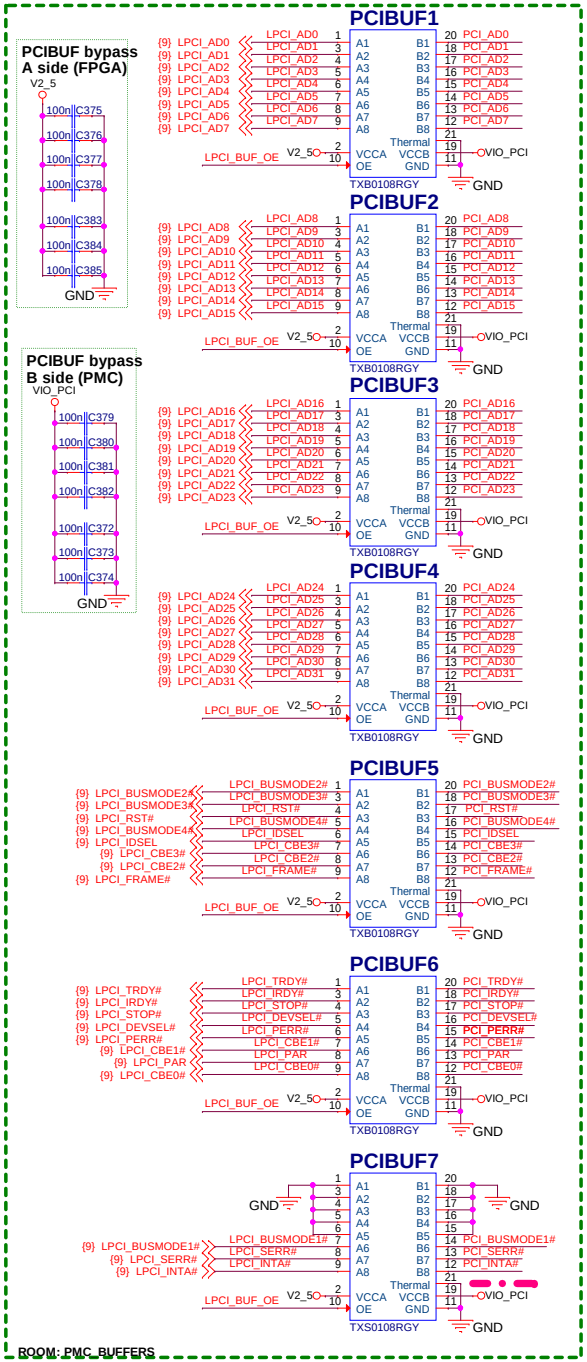


Title	Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. A
		SHEET 8 OF 13	

Fiber SFP, PCI <> FPGA connections



PMC host interface



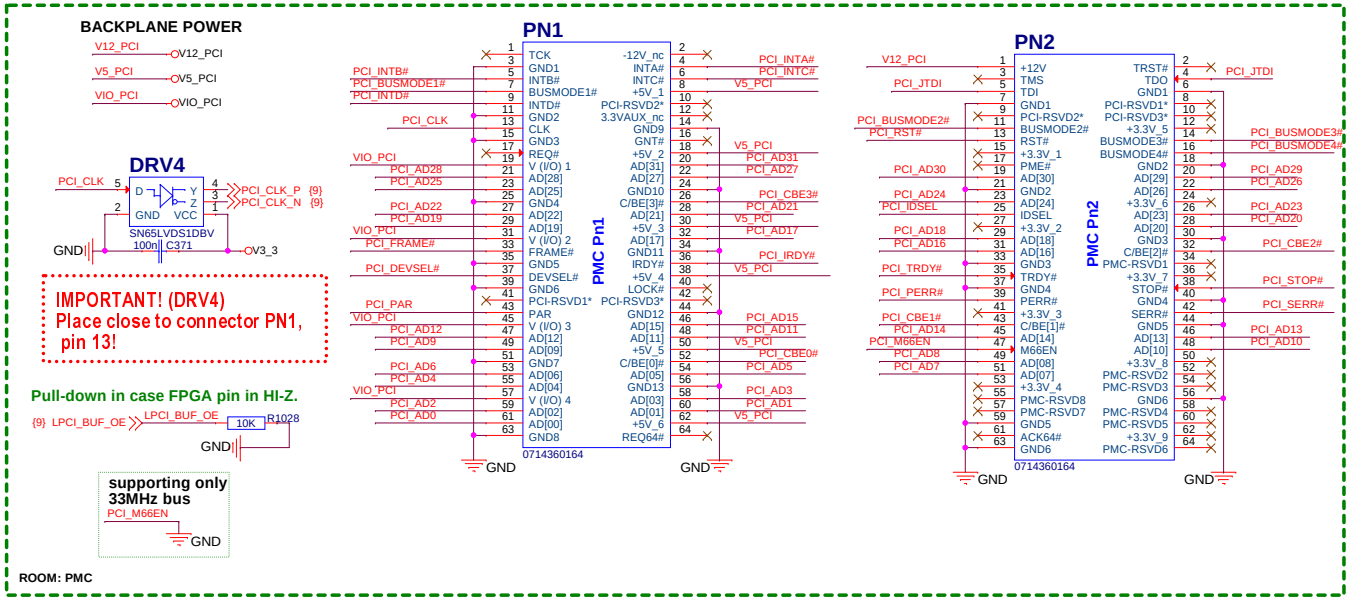
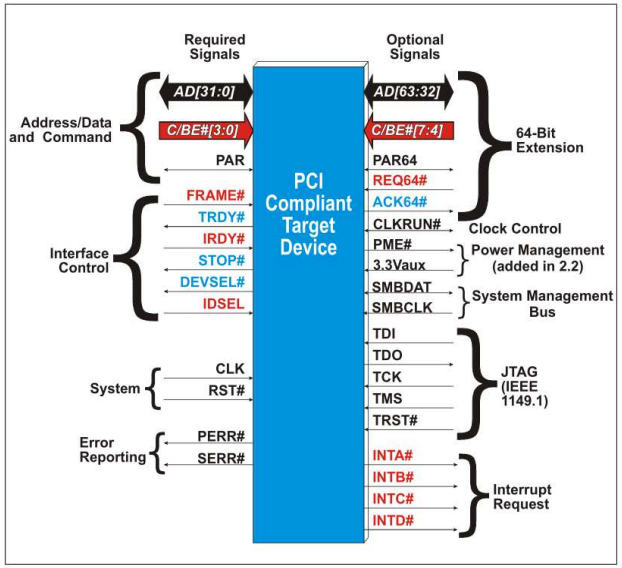


Figure 4-2: PCI-Compliant Target Device Signals



Title: PMC host interface				
Size: A3	Type: SE	DWG.NO.: CSL_FTRN_PMC		REV.: A
				SHEET: 10 OF 13

IO block power supply, FPGA <> IO block connections

{12} LVTIO_OUT_P_1 — LVTIO_OUT_P_1
{12} LVTIO_OUT_N_1 — LVTIO_OUT_N_1
{12} #LVTIO_OE_1 — #LVTIO_OE_1
{12} LVTIO_IN_P_1 — LVTIO_IN_P_1
{12} LVTIO_IN_N_1 — LVTIO_IN_N_1
{12} LVTIO_TERM_EN_1 — LVTIO_TERM_EN_1
{12} LVTIO_DIR_LED_1 — LVTIO_DIR_LED_1
{12} LVTIO_ACT_LED_1 — LVTIO_ACT_LED_1

{12} LVTIO_OUT_P_2 — LVTIO_OUT_P_2
{12} LVTIO_OUT_N_2 — LVTIO_OUT_N_2
{12} #LVTIO_OE_2 — #LVTIO_OE_2
{12} LVTIO_IN_P_2 — LVTIO_IN_P_2
{12} LVTIO_IN_N_2 — LVTIO_IN_N_2
{12} LVTIO_TERM_EN_2 — LVTIO_TERM_EN_2
{12} LVTIO_DIR_LED_2 — LVTIO_DIR_LED_2
{12} LVTIO_ACT_LED_2 — LVTIO_ACT_LED_2

{12} LVTIO_OUT_P_3 — LVTIO_OUT_P_3
{12} LVTIO_OUT_N_3 — LVTIO_OUT_N_3
{12} #LVTIO_OE_3 — #LVTIO_OE_3
{12} LVTIO_IN_P_3 — LVTIO_IN_P_3
{12} LVTIO_IN_N_3 — LVTIO_IN_N_3
{12} LVTIO_TERM_EN_3 — LVTIO_TERM_EN_3
{12} LVTIO_DIR_LED_3 — LVTIO_DIR_LED_3
{12} LVTIO_ACT_LED_3 — LVTIO_ACT_LED_3

{13} LVTIO_OUT_P_4 — LVTIO_OUT_P_4
{13} LVTIO_OUT_N_4 — LVTIO_OUT_N_4
{13} #LVTIO_OE_4 — #LVTIO_OE_4
{13} LVTIO_IN_P_4 — LVTIO_IN_P_4
{13} LVTIO_IN_N_4 — LVTIO_IN_N_4
{13} LVTIO_TERM_EN_4 — LVTIO_TERM_EN_4
{13} LVTIO_DIR_LED_4 — LVTIO_DIR_LED_4
{13} LVTIO_ACT_LED_4 — LVTIO_ACT_LED_4

{13} LVTIO_OUT_P_5 — LVTIO_OUT_P_5
{13} LVTIO_OUT_N_5 — LVTIO_OUT_N_5
{13} #LVTIO_OE_5 — #LVTIO_OE_5
{13} LVTIO_IN_P_5 — LVTIO_IN_P_5
{13} LVTIO_IN_N_5 — LVTIO_IN_N_5
{13} LVTIO_TERM_EN_5 — LVTIO_TERM_EN_5
{13} LVTIO_DIR_LED_5 — LVTIO_DIR_LED_5
{13} LVTIO_ACT_LED_5 — LVTIO_ACT_LED_5

LOG1F

BANK 5A
LOWER LEFT
3.3V

LVTTL IO control signals

{13} #LVTTL_IN_CLK_EN

#LVTIO_OE_1	N5	DQ1R_1
LVTIO_TERM_EN_1	P1	DQ1R_2
LVTIO_ACT_LED_1	P3	DQ1R_3
LVTIO_DIR_LED_1	R2	DQ1R_4
#LVTIO_OE_2	R3	DQ1R_5
LVTIO_TERM_EN_2	R6	DQ1R_6
LVTIO_ACT_LED_2	T1	DQ1R_7
LVTIO_DIR_LED_2	T2	DQ1R_8
#LVTIO_OE_3	T3	DQ1R_9
LVTIO_TERM_EN_3	T6	DQ1R_10
LVTIO_ACT_LED_3	U1	DQ1R_12
LVTIO_DIR_LED_3	T7	DQ1R_11
#LVTIO_OE_4	U5	DQ1R_13
LVTIO_TERM_EN_4	V1	DQ1R_14
LVTIO_ACT_LED_4	V4	DQ1R_15
LVTIO_DIR_LED_4	V5	DQ1R_16
#LVTIO_OE_5	W1	DQ1R_17
LVTIO_TERM_EN_5	W2	DQ1R_18
LVTIO_ACT_LED_5	N6	IO_1F
LVTIO_DIR_LED_5	P4	IO_2F
#LVTTL_IN_CLK_EN	P6	IO_3F
	R5	IO_4F
	T4	IO_5F
	U6	IO_6F
	V2	IO_7F
	U3	DQSN1R
	V3	DQS1R
	U7	IO_VREFB5AN0

N1 CLK14N_DQ1R
M1 CLK14P_DQ1R
N3 CLK15N_DQ1R
N2 CLK15P_DQ1R

5AGXMA3D4F27I3N

LOG1I

BANK 7C
TOP LEFT
2.5V

LVTTL IO data inputs

LVTIO_IN_N_1	A6	RX_T19N_DQSN1T
LVTIO_IN_P_1	A5	RX_T19P_DQS1T
LVTIO_IN_N_2	C6	RX_T21N_DQ1T
LVTIO_IN_P_2	B6	RX_T21P_DQ1T
LVTIO_IN_N_3	E6	RX_T15N_DQ1T
LVTIO_IN_P_3	D6	RX_T15P_DQ1T
LVTIO_IN_N_4	F7	RX_T17N_DQ1T
LVTIO_IN_P_4	E7	RX_T17P_DQ1T
LVTIO_IN_N_5	H9	RX_T23N_DQ1T
LVTIO_IN_P_5	G9	RX_T23P_DQ1T
	D8	RX_T24N_DQ1T
	C8	RX_T24P_DQ1T
	E9	RX_T26N_DQ1T
	D9	RX_T26P_DQ1T
	H10	RX_T28N_DQ1T
	G10	RX_T28P_DQ1T

LVTTL IO data outputs

LVTIO_OUT_N_1	A9	TX_T25N
LVTIO_OUT_P_1	A8	TX_T25P_DQ1T
LVTIO_OUT_N_2	C7	TX_T22N
LVTIO_OUT_P_2	B7	TX_T22P_DQ1T
LVTIO_OUT_N_3	D5	TX_T18N
LVTIO_OUT_P_3	C5	TX_T18P_DQ1T
LVTIO_OUT_N_4	G8	TX_T20N
LVTIO_OUT_P_4	F8	TX_T20P_DQ1T
LVTIO_OUT_N_5	J8	TX_T16N
LVTIO_OUT_P_5	J9	TX_T16P_DQ1T
	K10	TX_T27N
	J10	TX_T27P_DQ1T
	C9	TX_T29N
	B9	TX_T29P_DQ1T
	E10	DQ1T
	F10	IO_VREFB7CN0

5AGXMA3D4F27I3N

LOG1E

BANK 4D
BOTTOM CENTER
3.3V

AB13	RX_B47N_DQ2B	
AC13	RX_B47P_DQ2B	
AD13	RX_B49N_DQ2B	
AE13	RX_B49P_DQ2B	
AD12	RX_B51N_DQ2B	
AE12	RX_B51P_DQ2B	
AF12	RX_B52N_DQ2B	
AF11	RX_B52P_DQ2B	
AC10	RX_B54N_DQ2B	
AD10	RX_B54P_DQ2B	
AE10	RX_B56N_DQSN2B	
AF9	RX_B56P_DQS2B	
V10	RX_B58N_DQ2B	
W10	RX_B58P_DQ2B	
AB9	RX_B60N_DQ2B	
AC9	RX_B60P_DQ2B	
V13	TX_B46N	
W13	TX_B46P_DQ2B	
Y13	TX_B48N	
AA13	TX_B48P_DQ2B	
V12	TX_B50N	
W12	TX_B50P_DQ2B	
AC11	TX_B53N	
AD11	TX_B53P_DQ2B	
Y11	TX_B55N	
AA11	TX_B55P_DQ2B	
AD9	TX_B57N	
AE9	TX_B57P_DQ2B	
Y10	TX_B59N	
AA10	TX_B59P_DQ2B	
AB12	DQ2B	
AA12	IO_VREFB4DN0	

5AGXMA3D4F27I3N

Power supply for output drivers

V_MAIN
100K R130
100n C329
GND
PRUN_3V3_IO
H5
POWIO33A
RUN/SS
AUX
F5
BIAS
G5
PGOOD_3V3_IO
H6
PGOOD
SYNC
G6
10K R132
ADJ
H7
154K R131
SHARE
R_T
G7
49K9 R129
F7
10K R133
red D17
LR QH9F
LTM8023EV
GND

POWIO33B
V_MAIN
G1 G2 G3 H1 H2 H3
V_IN1 V_IN2 V_IN3 V_IN4 V_IN5 V_IN6
V_OUT1 V_OUT2 V_OUT3 V_OUT4 V_OUT5 V_OUT6 V_OUT7 V_OUT8 V_OUT9 V_OUT10 V_OUT11 V_OUT12
A1 A2 A3 A4 B1 B2 B3 B4 C1 C2 C3 C4
LTM8023EV
C331 100n
C330 10u
TP18
ODRV
JV33_ODRV
JMP_V2
V33_ODRV
C332 22u
C333 100u
C334 100u
GND

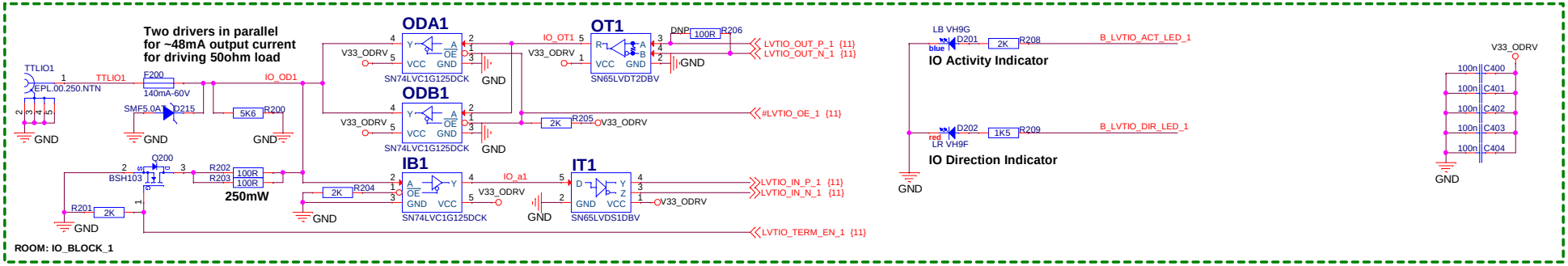
POWIO33C
A5 A6 A7 B5 B6 B7 C5 C6 C7 D1 D2 D3
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12
GND24 GND23 GND22 GND21 GND20 GND19 GND18 GND17 GND16 GND15 GND14 GND13
F6 E7 E6 E5 E4 E3 E2 E1 D7 D6 D5 D4
LTM8023EV
GND

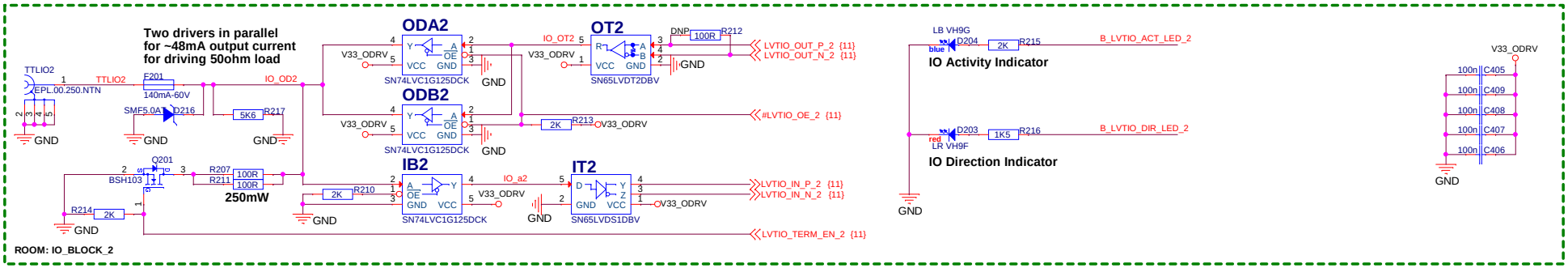
ROOM: IO_POWER

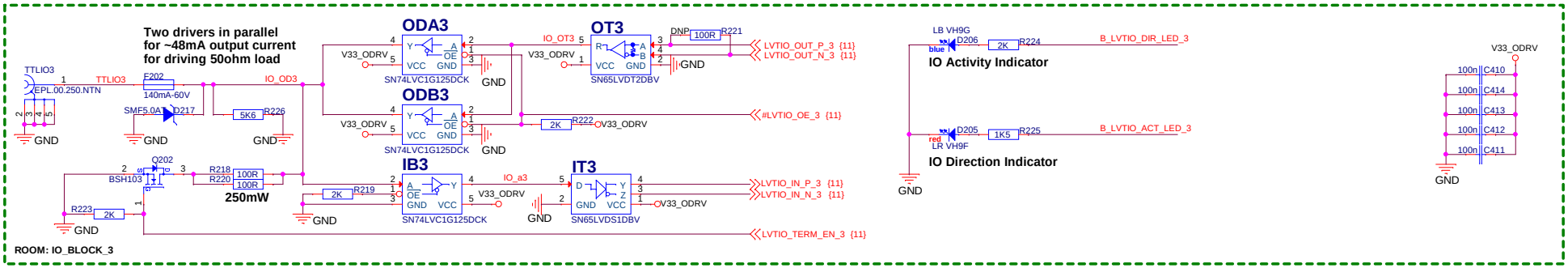
* - IO overvoltage protection bias circuit is based OHWR FMC-DIO-5CHTTLA

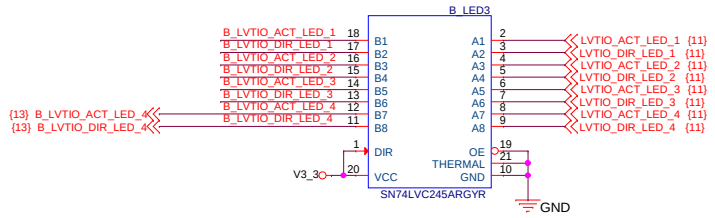
Title	IO block power supply, FPGA <> IO block connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. A
		SHEET 11 OF 13	

LVTTL IO blocks 1-3



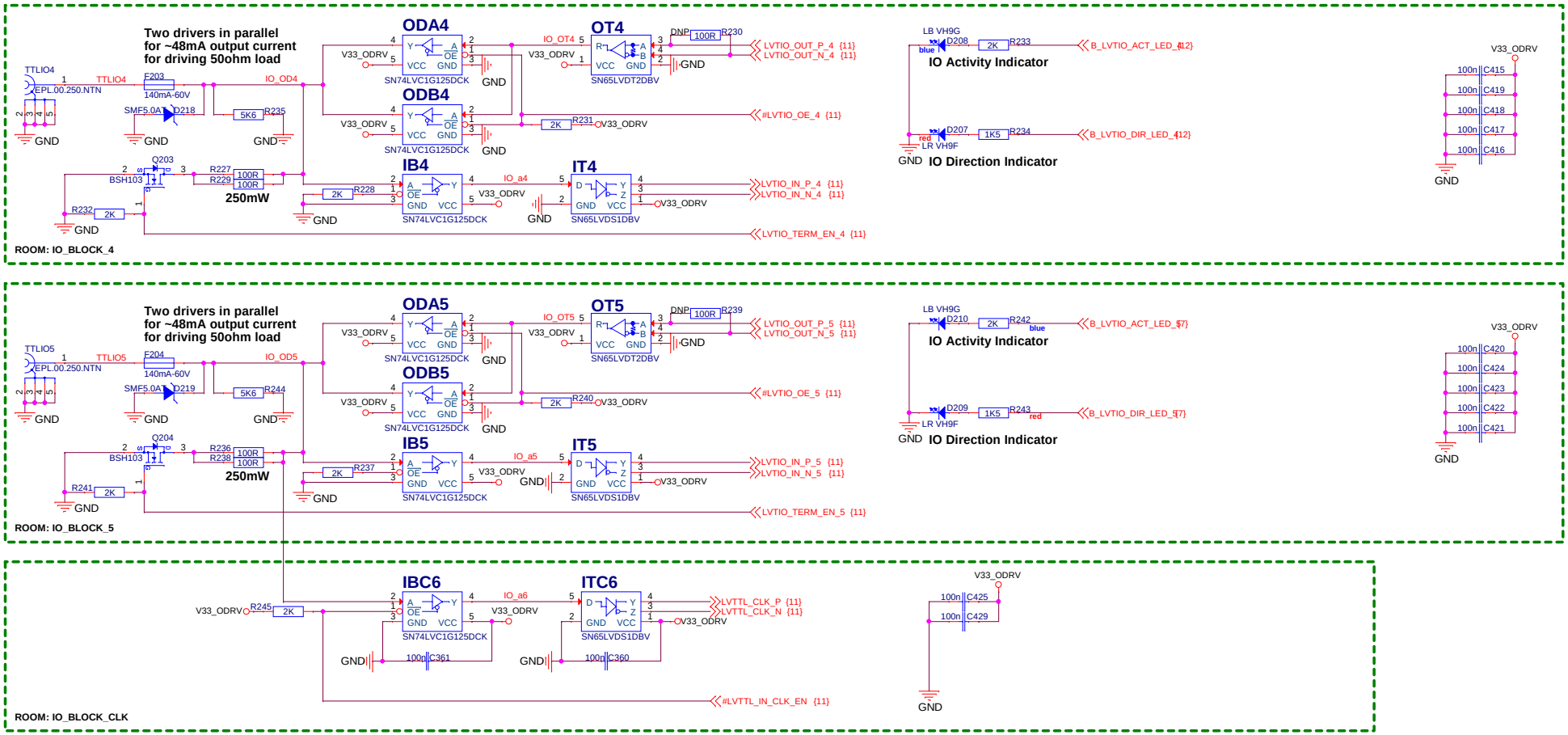






Title	LVTTL IO blocks 1-3		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. A
		SHEET 12 OF 13	

LVTTL IO blocks 4-5, IO CLOCK input



Title	LVTTL IO blocks 4-5, IO CLOCK input		
Size A3	Type SE	DWG.NO. CSL_FTRN_PMC	REV. A
			SHEET 13 OF 13