FAIR Timing Receiver (FTRN) PCIe form factor - CSL_FTRN_PCIe

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DATE	REVISION DESCRIPTION	DRAWN	REV
11.09.2019	Initial version	dslavinec, mlevicnik	A
08.10.2019	Resistors package changed from 0402 to 0805 (R1035, R1036, R1037)	AJuvancic	A
18.10.2019	Capacitors (C436~C443) moved from FPGA side to PCIe connector side	AJuvancic	A
26.11.2019	Resistors (R21,R23,R26,R29) value changed from 10K to 1K5	AJuvancic	A
26.11.2019	Capacitors (C357,C358,C370) Mounted status changed to DNP	AJuvancic	A
26.11.2019	Capacitors PART_NUMBER changed (ND6-100N -> ND6-100N, NB7-1U -> NB7-1U-25V)	AJuvancic	A
23.04.2020	Solder jumpers (J1V1, J1V15, J3V3, J2V5, JVLC5, JVCCD_1_5, JODRV_33V) replaced with 0R resistors. Capacitors package changed from 1210 to 0805 (C326, C337)	AJuvancic	B
06.05.2020	Jumper SJMP2 replaced with two 0805 resistors (SJMP2 and SJMP2/2)	AJuvancic	B
08.05.2020	Jumper SJMP2 Mounted status moved from DNP to mounted	AJuvancic	B
12.05.2020	Solder jumpers Mounted status moved from DNP to mounted (J1V1, J1V15, J3V3, J2V5, JVLC5, JVCCD_1_5, JODRV_33V)	AJuvancic	B

Value	Capatitors used
12p	0402, 50V, C0G, 1%
22p	0402, 50V, C0G, 1%
10n	0402, 25V, X7R, 10%
100n	0402, 25V, X7R, 10%
1u	0603, 16V, X7R, 10%
2.2u	1210, 100V, X7R, 10%
10u	1210, 25V, X7R, 10%
22u	1210, 10V, X7R, 10%
100u	1210, 10V, X5R, 20%

All resistors are SMD 0402, 63mW, 1% except where marked differently.

Components marked DNP (Do Not Place) are foreseen for testing purposes.

TOP layer

FM1 FIDUCIAL FM2 FIDUCIAL FM3 FIDUCIAL

BOTTOM layer

FM4 FIDUCIAL FM5 FIDUCIAL FM6 FIDUCIAL

DRAWN	Dušan Slavinec, Marko Levicnik		11.09.2019
CHECKED	Marko Levicnik		
APPROVED	Gregor Cuk		

Title: FAIR Timing Receiver (FTRN) PCIe form factor - CSL_FTRN_PCIe

Size: A3 | Type: SE | DWG.NO. CSL_FTRN_PCIe | REV. B

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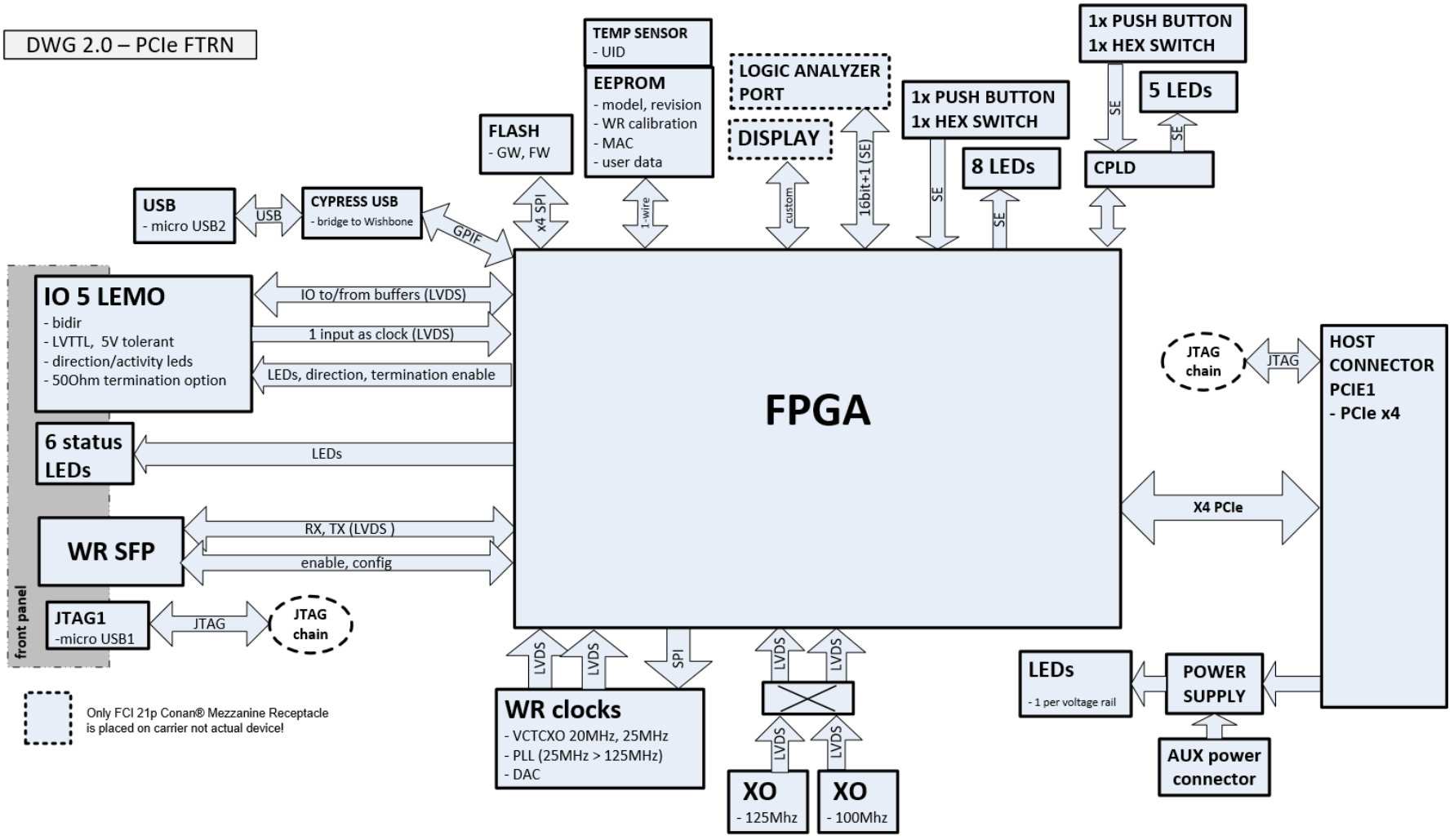
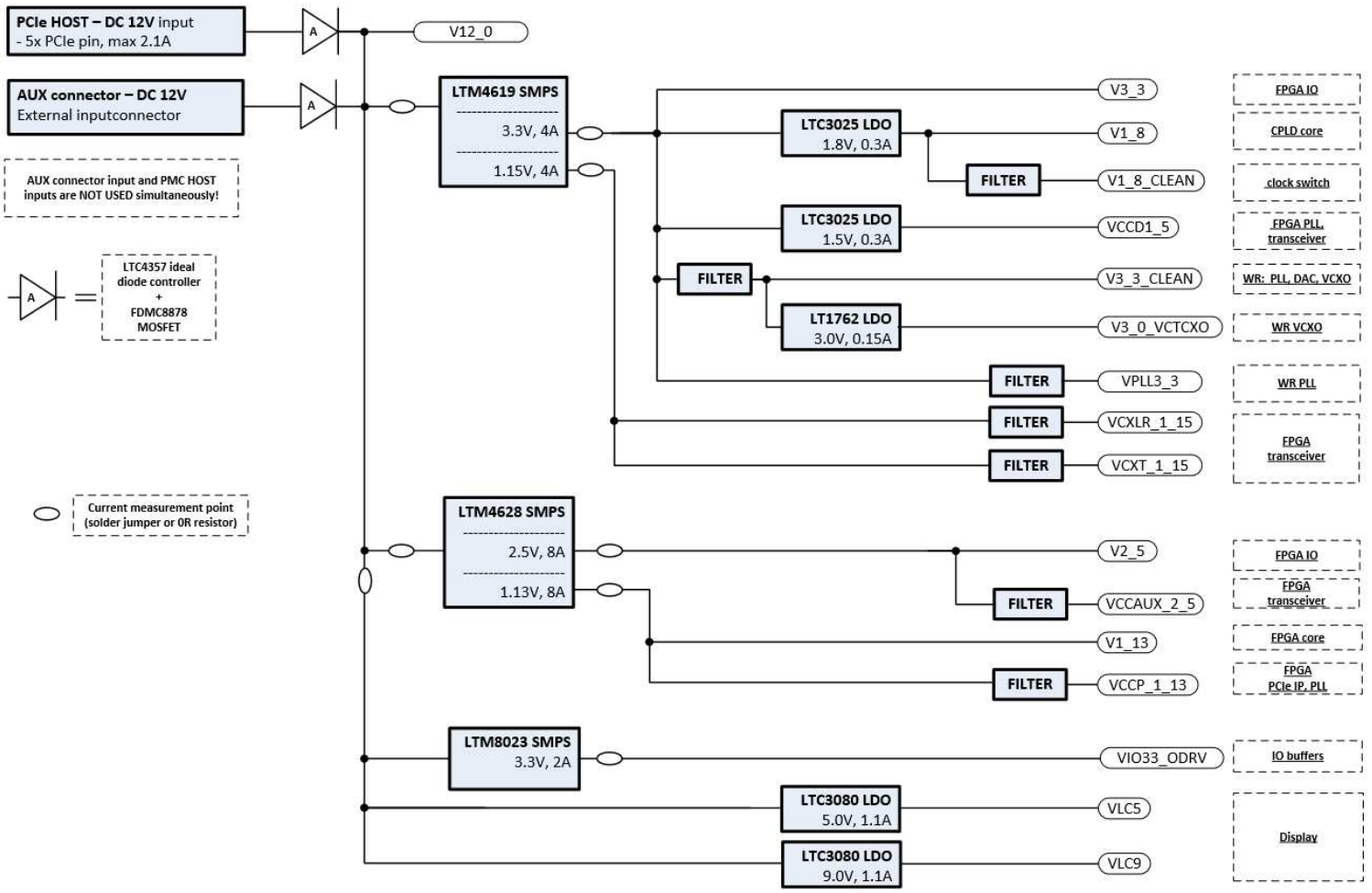
Block Diagram



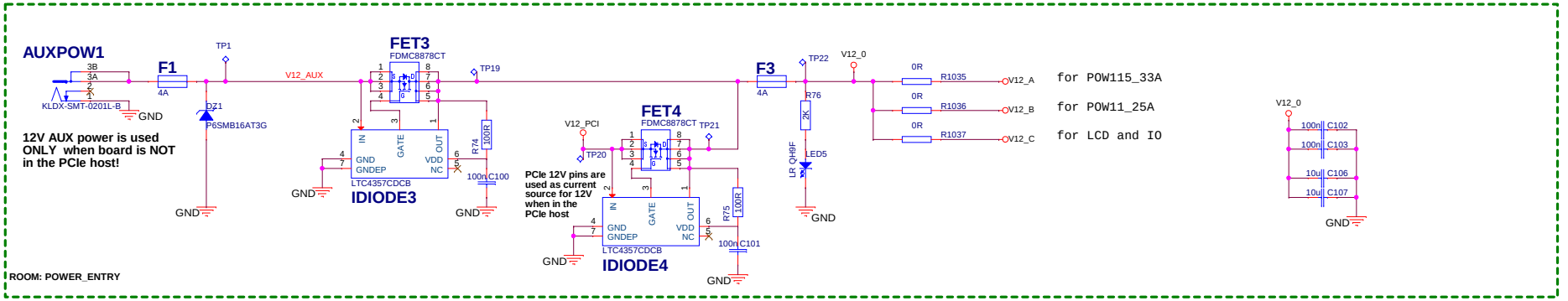
Title: Block Diagram			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PCIe	REV. A
			SHEET 2 OF 13

Power tree block scheme

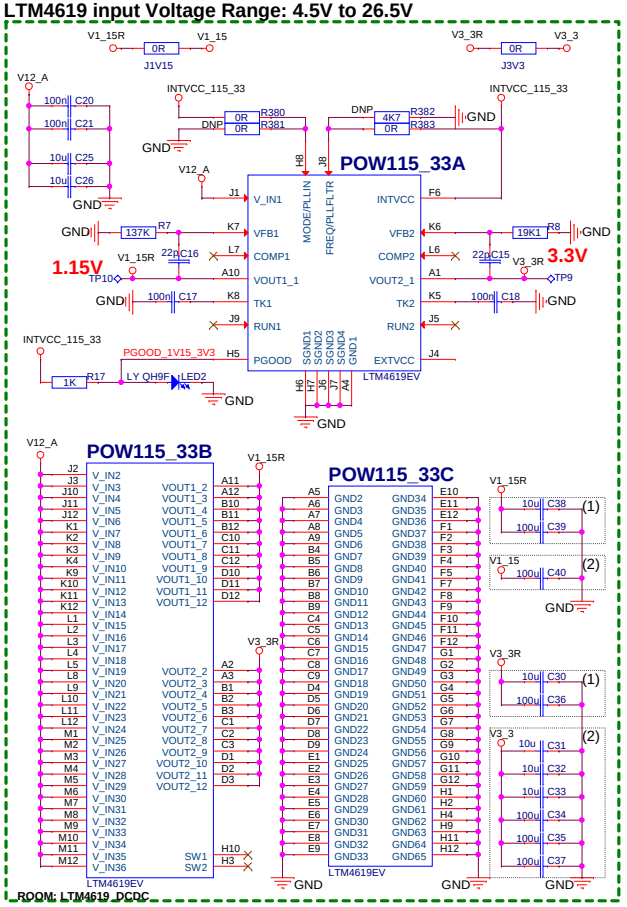


Title: Power tree block scheme			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PCIe	REV. A
			SHEET 3 OF 13

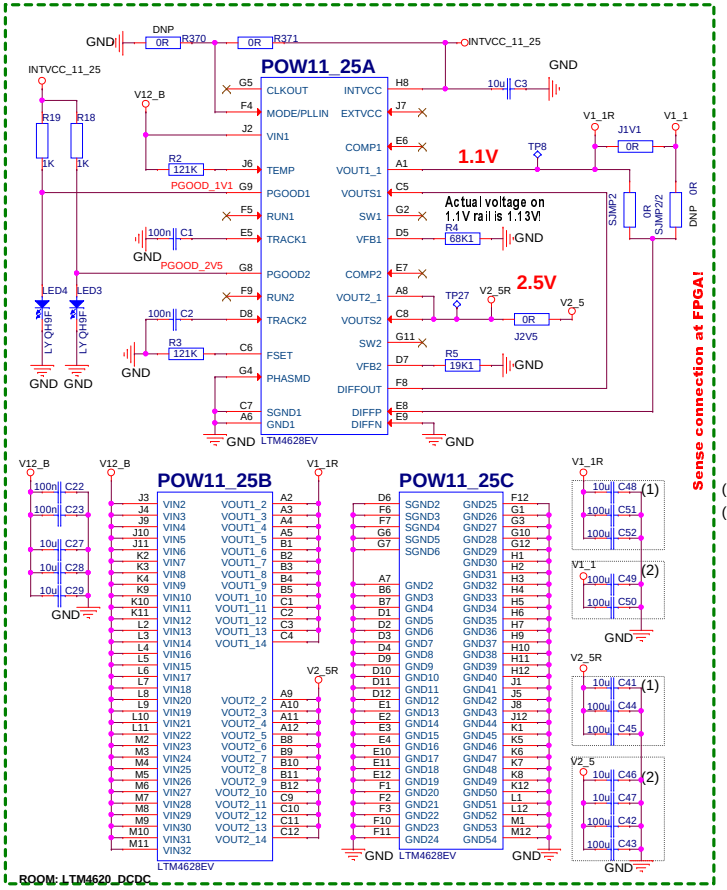
Power entry and main DCDC power regulators



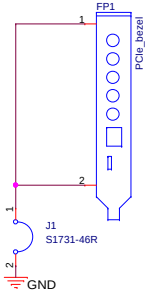
LTM4619 input Voltage Range: 4.5V to 26.5V



LTM4628 input Voltage Range: 4.5V to 16V



Optional PCIe bezel connection to GND

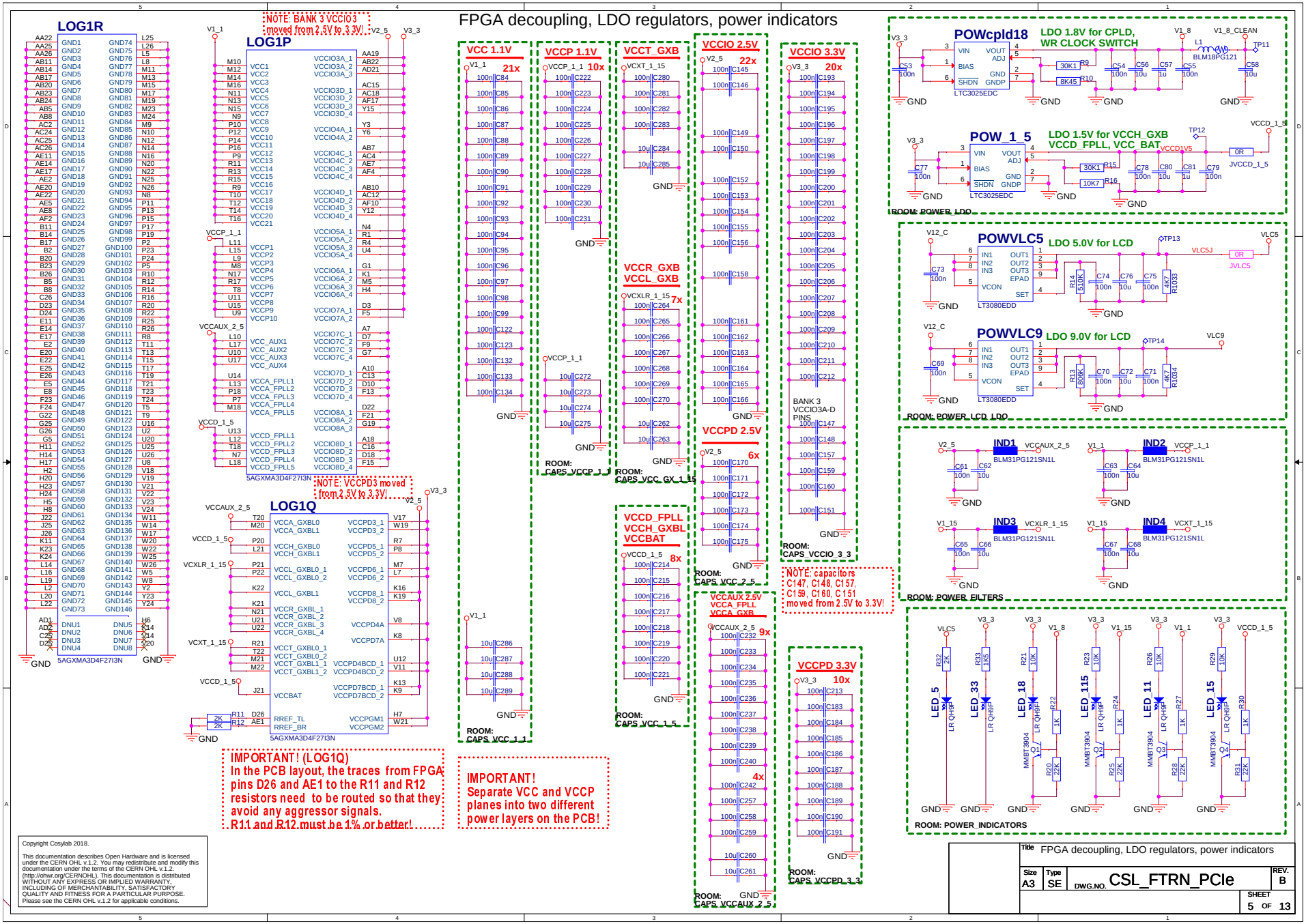


(1) - place capacitors at the regulator outputs

(2) - place capacitors away from the regulator outputs

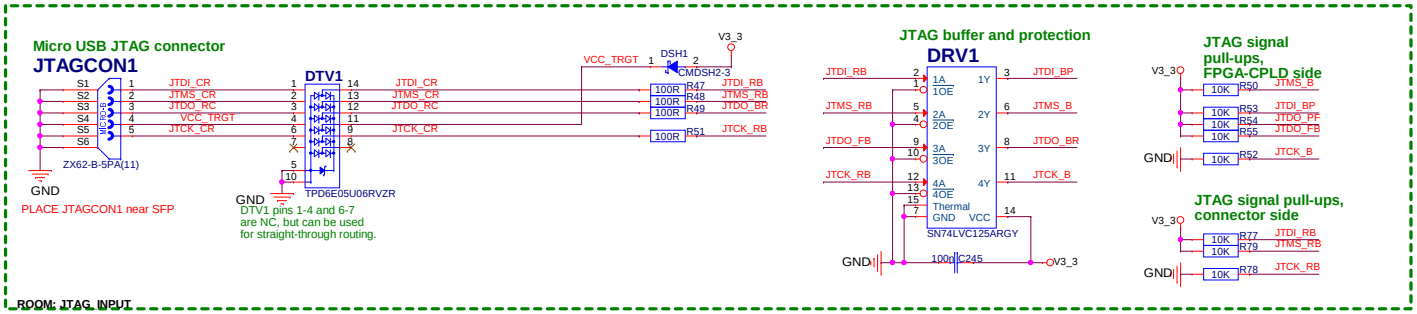
Title: Power entry and main DCDC power regulators				
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PCIe		REV. B
				SHEET 4 OF 13

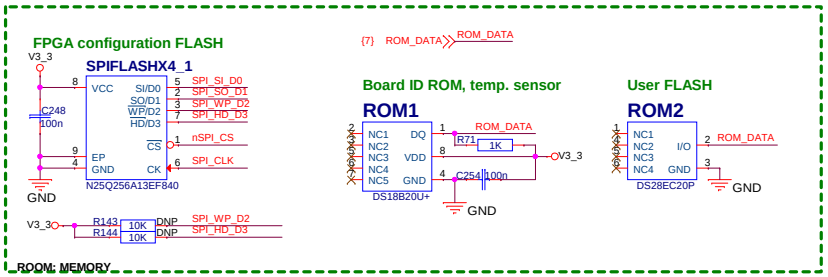
FPGA decoupling, LDO regulators, power indicators

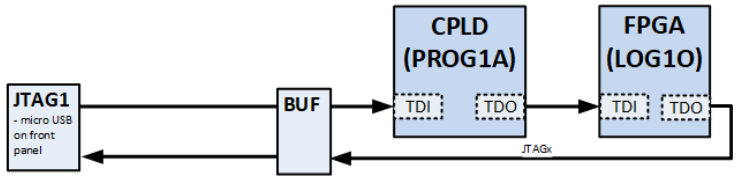


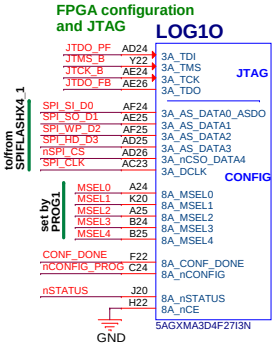
Title	FPGA decoupling, LDO regulators, power indicators		
Size A3	Type SE	DWG.NO. CSL_FTRN_PCIe	REV. B
			SHEET 5 OF 13

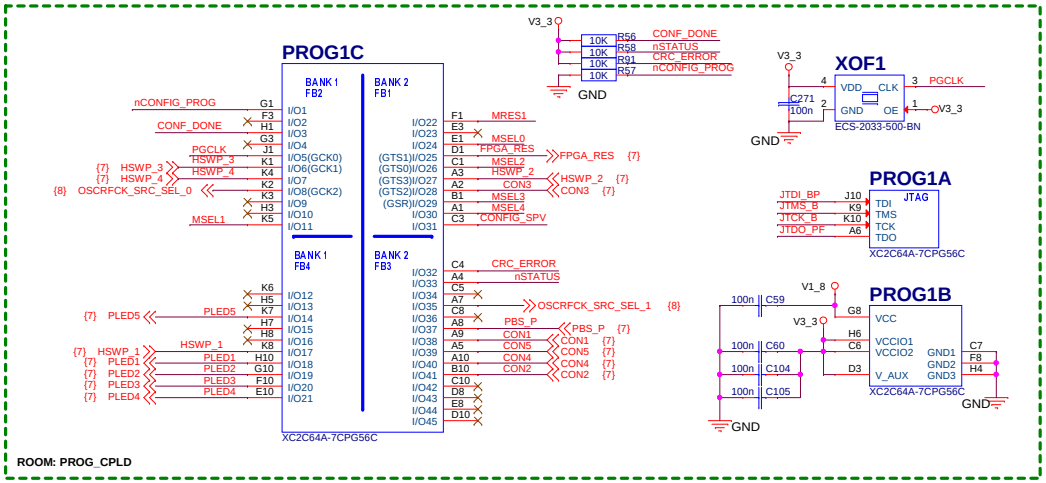
FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash

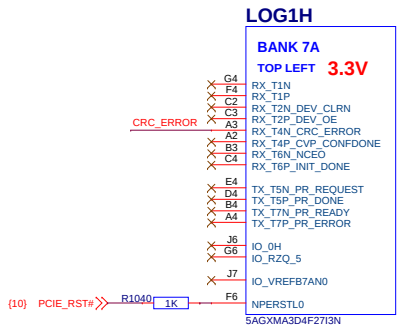


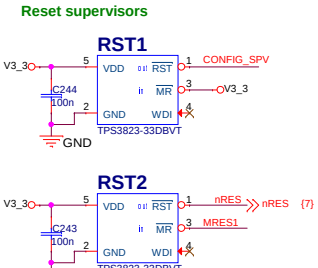






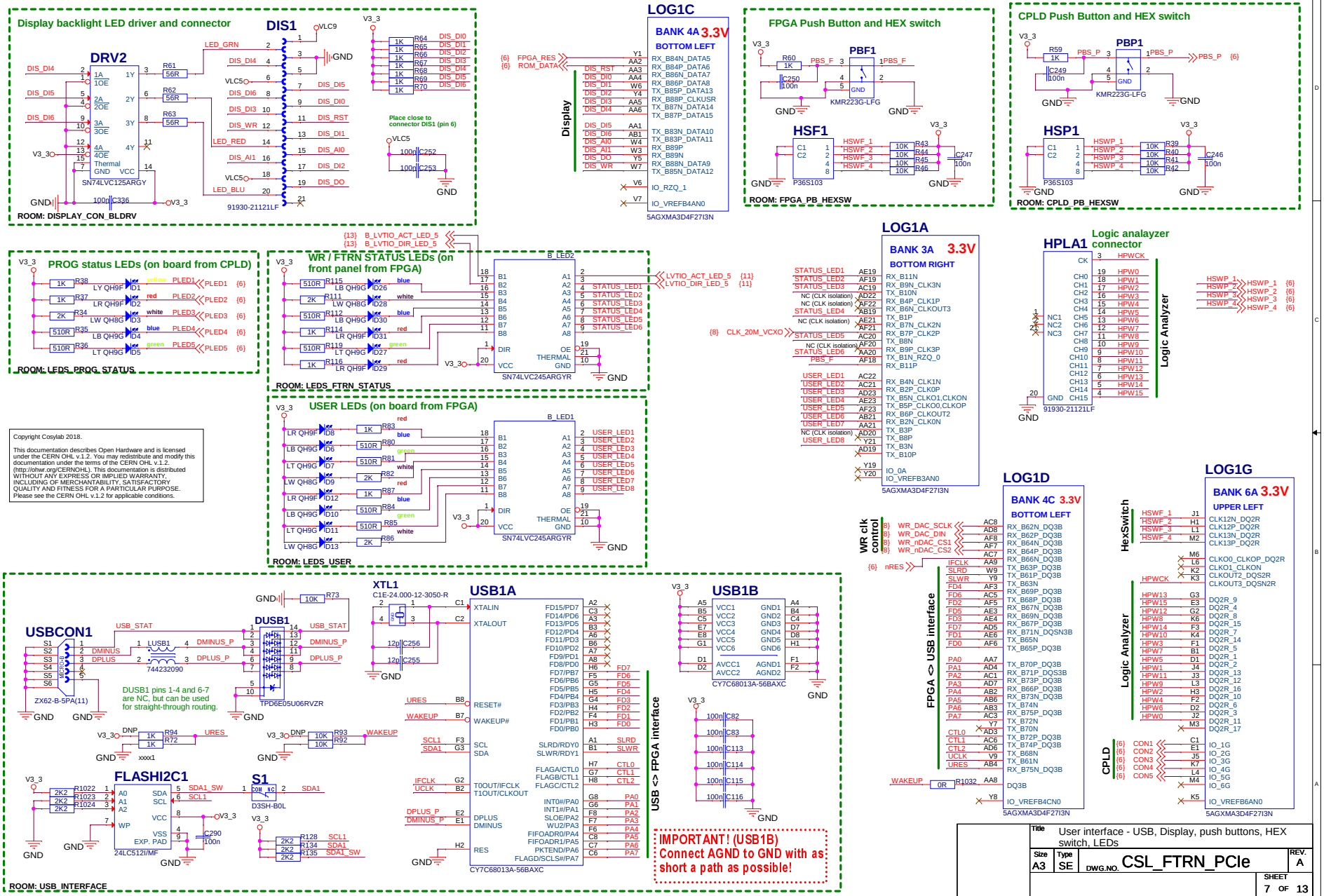






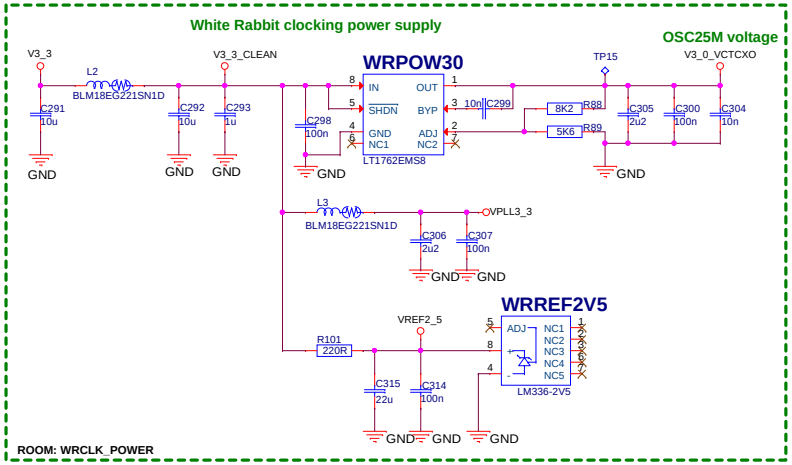
Title	FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash		
Size A3	Type SE	DWG.NO. CSL_FTRN_PCIe	REV. A
			SHEET 6 OF 13

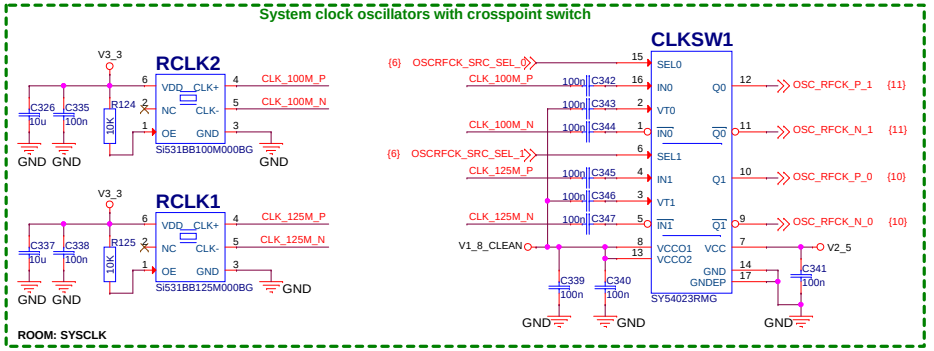
User interface - USB, Display, push buttons, HEX switch, LEDs

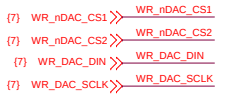


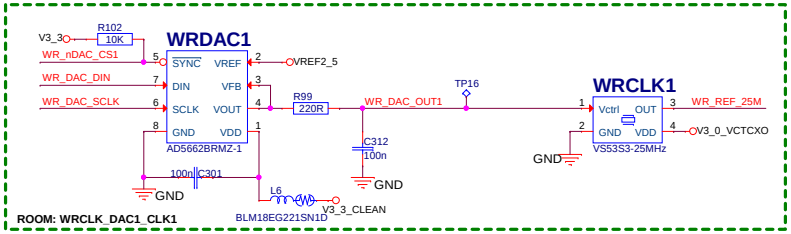
Title	User interface - USB, Display, push buttons, HEX switch, LEDs
Size	A3
Type	SE
DWG.NO.	CSL_FTRN_PCIe
REV.	A
SHEET	7 OF 13

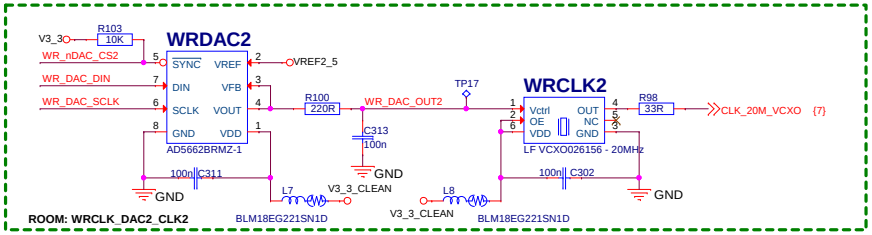
Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch

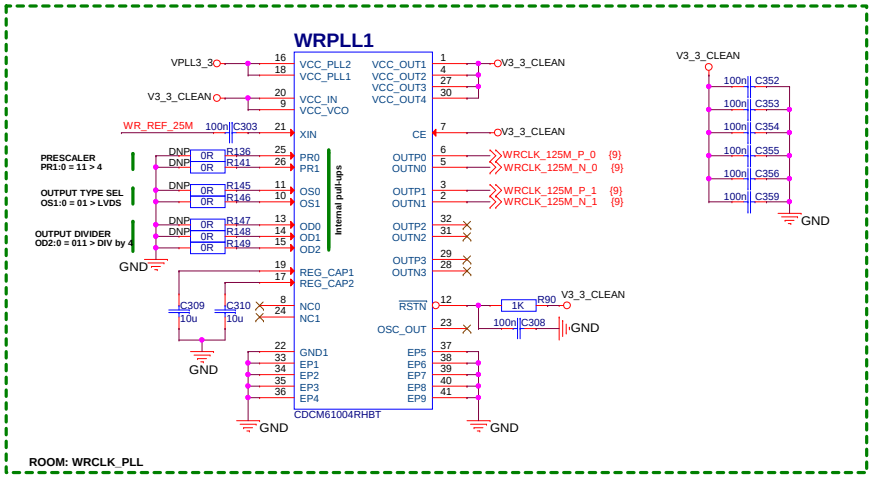






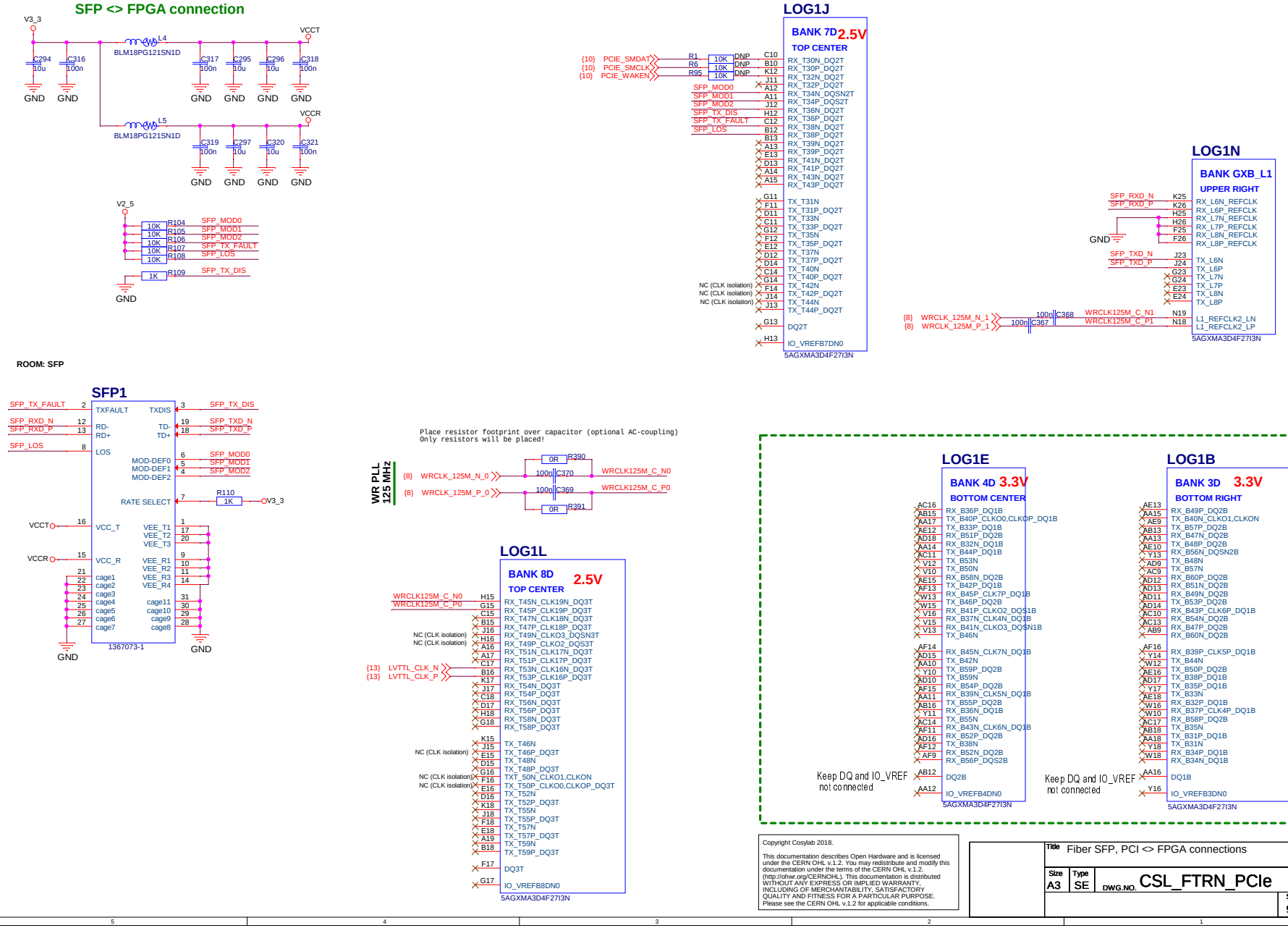






Title	Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch		
Size A3	Type SE	DWG.NO. CSL_FTRN_PCIe	REV. B
			SHEET 8 OF 13

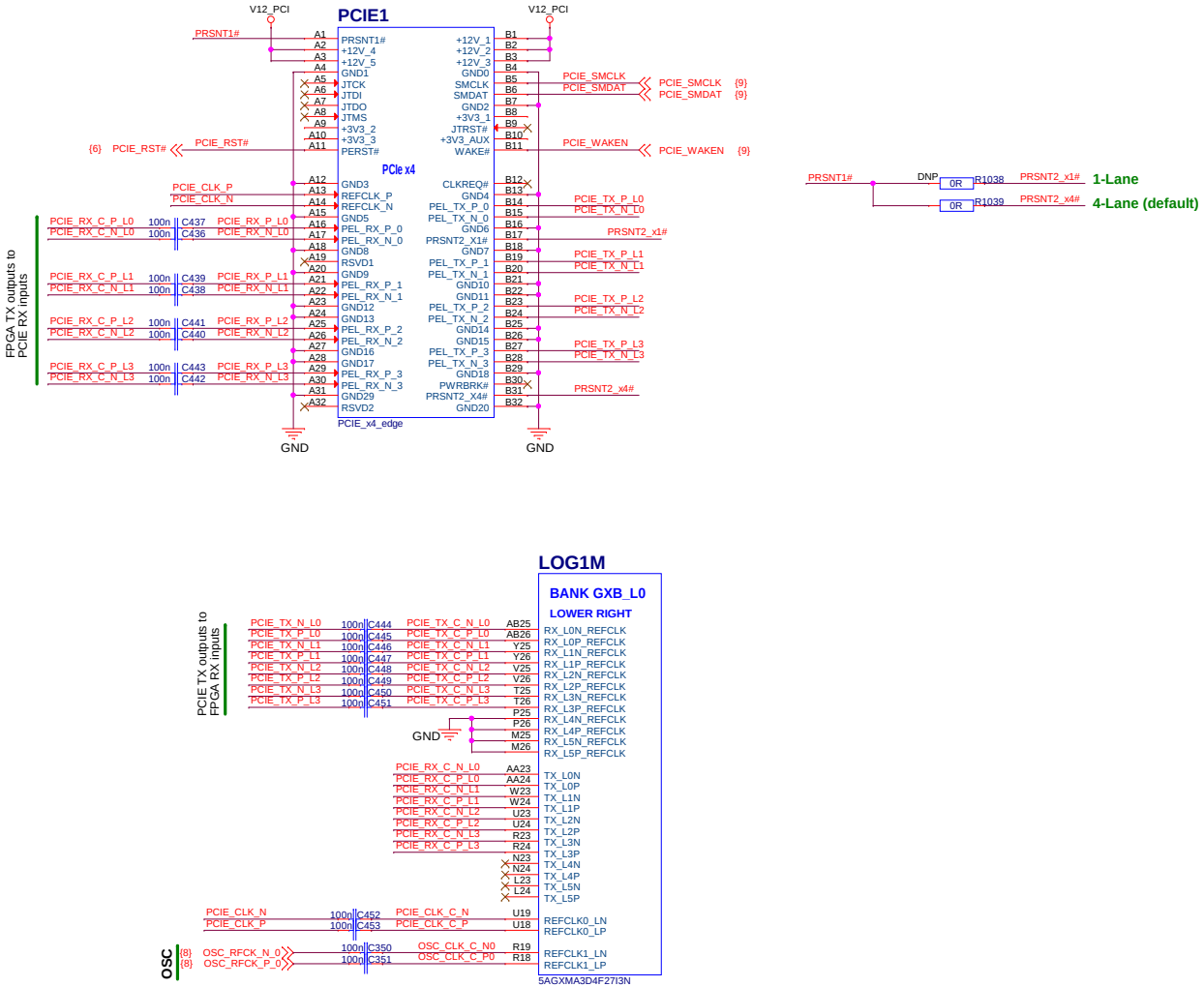
Fiber SFP, PCI <> FPGA connections



Title	Fiber SFP, PCI <> FPGA connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_PCIe	REV. A
			SHEET 9 OF 13

PCIe host interface

PCIe x4 PCB edge connector

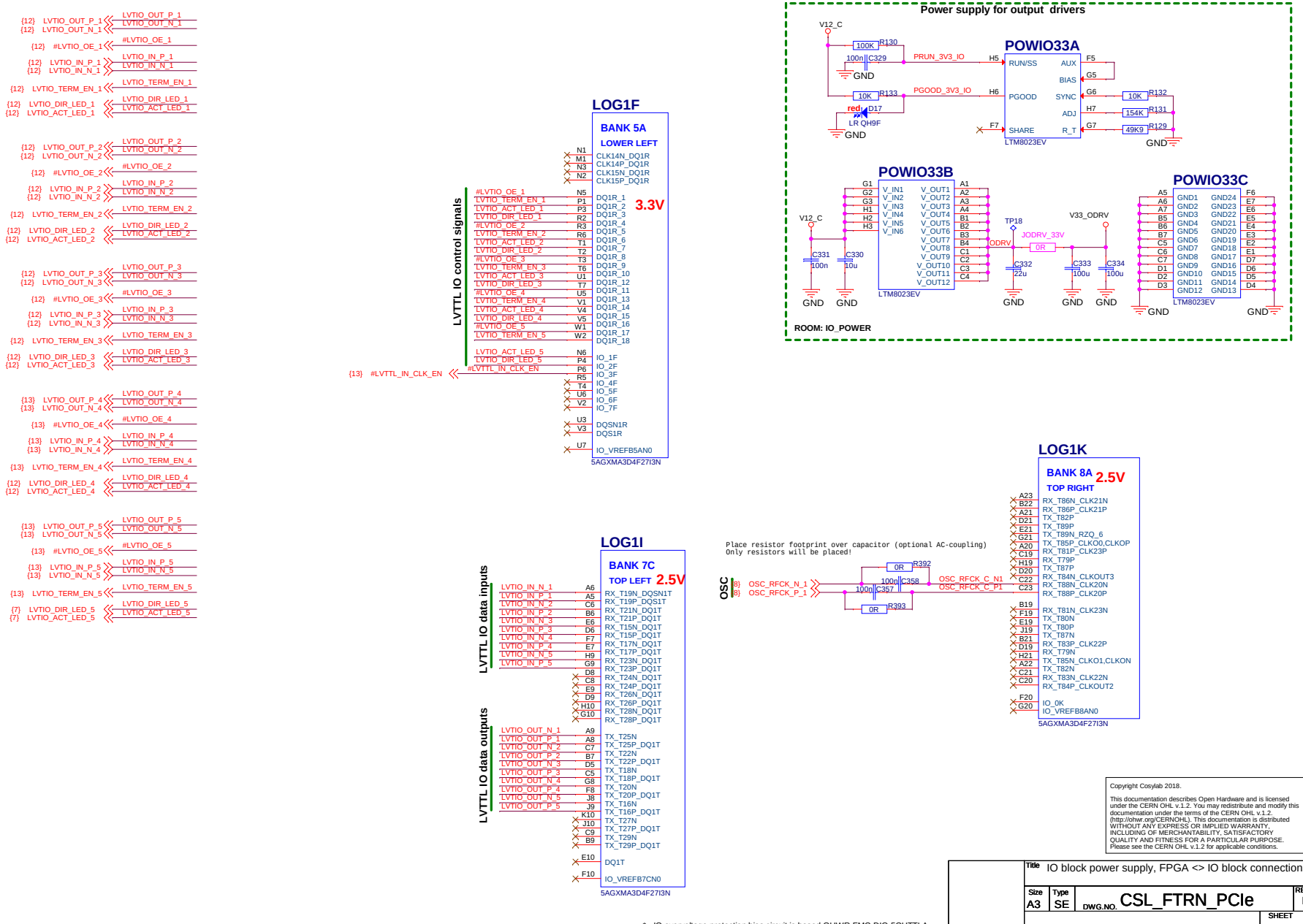


https://en.wikipedia.org/wiki/PCI_Express#Pinout

Pin	Side B	Side A	Description
1	+12 V	PRSNT1#	Must connect to farthest PRSNT2# pin
2	+12 V	+12 V	Main power pins
3	+12 V	+12 V	
4	Ground	Ground	
5	SMCLK	TCK	SMBus and JTAG port pins
6	SMDAT	TDI	
7	Ground	TDO	
8	+3.3 V	TMS	
9	TRST#	+3.3 V	
10	+3.3 V aux	+3.3 V	Standby power
11	WAKE#	PERST#	Link reactivation; fundamental reset
Key notch			
12	CLKREQ#[114]	Ground	Clock Request Signal
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK−	Lane 0 transmit data, + and −
15	HSOn(0)	Ground	
16	Ground	HSIp(0)	Lane 0 receive data, + and −
17	PRSNT2#	HSIn(0)	
18	Ground	Ground	
PCI Express ×1 cards end at pin 18			
19	HSOp(1)	Reserved	Lane 1 transmit data, + and −
20	HSOn(1)	Ground	
21	Ground	HSIp(1)	Lane 1 receive data, + and −
22	Ground	HSIn(1)	
23	HSOp(2)	Ground	Lane 2 transmit data, + and −
24	HSOn(2)	Ground	
25	Ground	HSIp(2)	Lane 2 receive data, + and −
26	Ground	HSIn(2)	
27	HSOp(3)	Ground	Lane 3 transmit data, + and −
28	HSOn(3)	Ground	
29	Ground	HSIp(3)	Lane 3 receive data, + and −
30	PWRBRK#[115]	HSIn(3)	
31	PRSNT2#	Ground	
32	Ground	Reserved	
PCI Express ×4 cards end at pin 32			

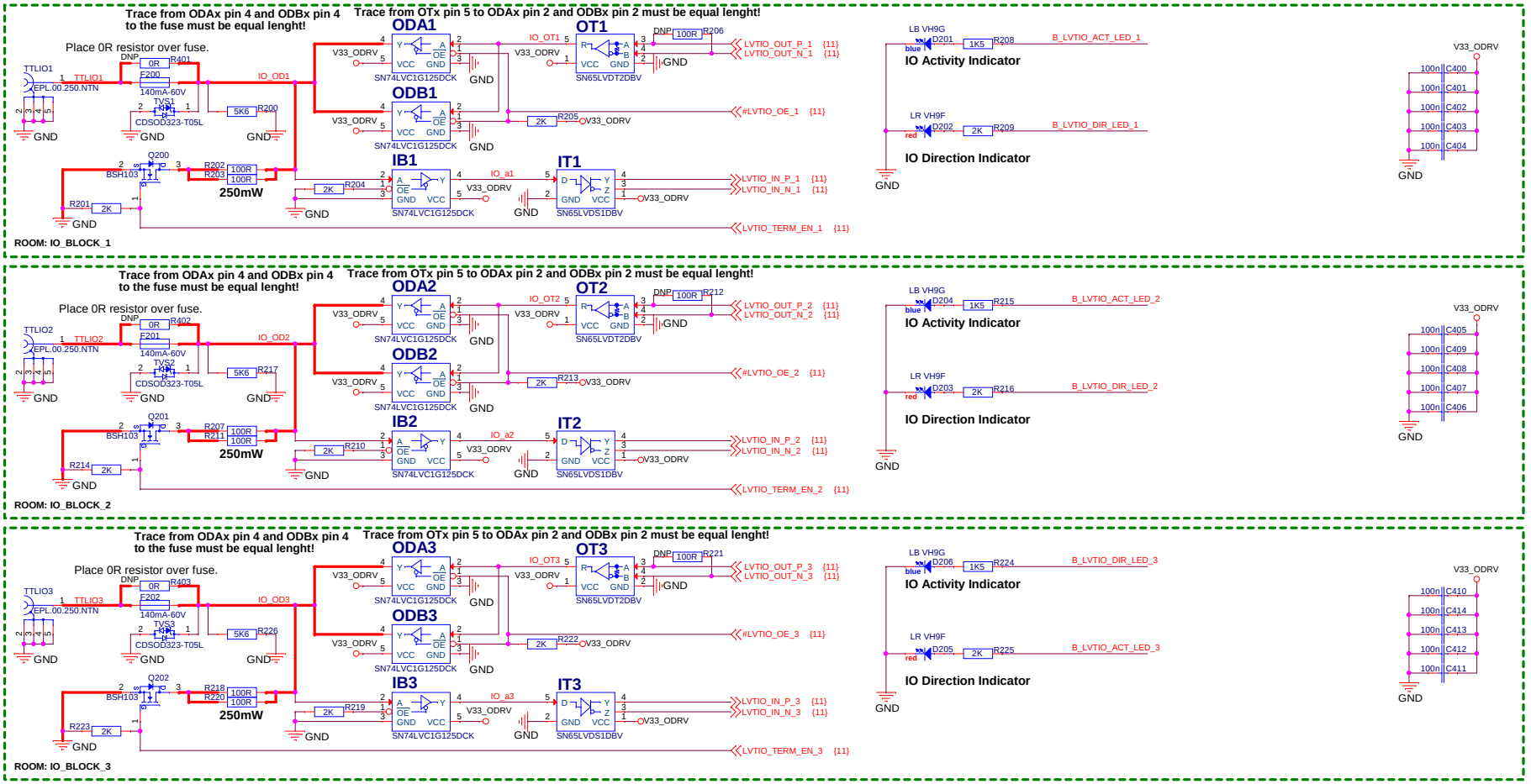
Title: PCIe host interface			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PCIe	REV. A
			SHEET 10 OF 13

IO block power supply, FPGA <> IO block connections



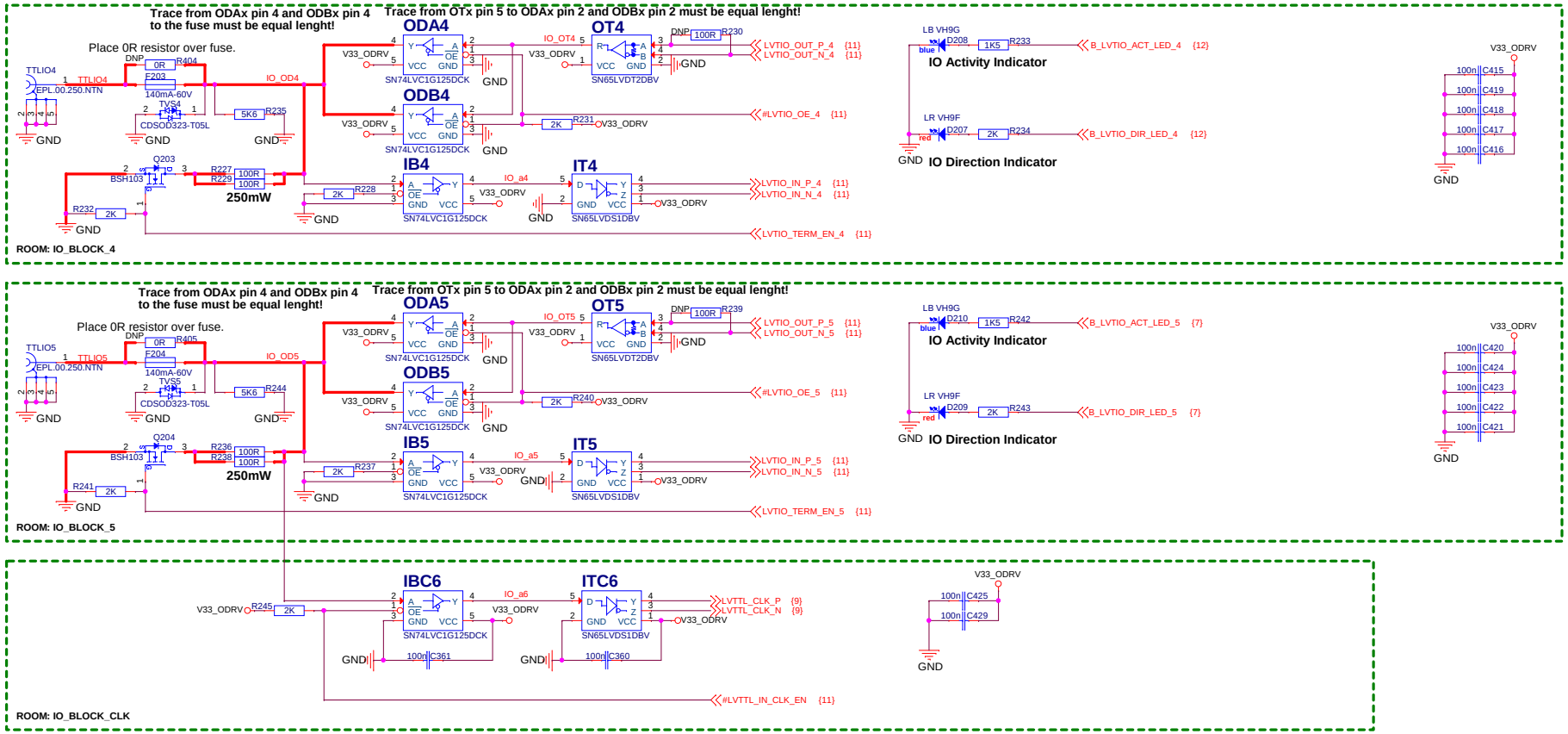
Title: IO block power supply, FPGA <> IO block connections			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_PCIe	REV. B
			SHEET 11 OF 13

LVTTL IO blocks 1-3



Title	LVTTL IO blocks 1-3		
Size A3	Type SE	DWG.NO. CSL_FTRN_PCIe	REV. A
			SHEET 12 OF 13

LVTTL IO blocks 4-5, IO CLOCK input



Title	LVTTL IO blocks 4-5, IO CLOCK input
Size	A3
Type	SE
DWG.NO.	CSL_FTRN_PCIe
REV.	A
SHEET	13 OF 13