

FAIR Timing Receiver (FTRN) PCIe form factor - CSL_FTRN_PCIe

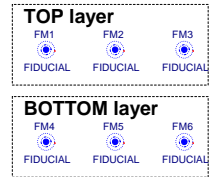
SHEET	TITLE
1	TITLE PAGE
2	Block diagram
3	Power Tree
4	POWER DC-DC
5	POWER LDOs, FPGA BYPASS
6	FPGA configuration
7	FPGA user interface
8	WR clocking, system CLOCKS
9	SFP to FPGA
10	PCIe host
11	IO to FPGA
12	IO blocks 1-3
13	IO blocks 4-5, IO clk

DATE	REVISION DESCRIPTION	DRAWN	REV
11.09.2019	Initial version	dslavinec, mlevicnik	A
08.10.2019	Resistors package changed from 0402 to 0805 (R1035, R1036, R1037)	AJuvancic	A
18.10.2019	Capacitors (C436-C443) moved from FPGA side to PCIe connector side	AJuvancic	A
26.11.2019	Resistors (R21,R23,R26,R29) value changed from 10K to 1K5	AJuvancic	A
26.11.2019	Capacitors (C357,C358,C370) Mounted status changed to DNP	AJuvancic	A
26.11.2019	Capacitors PART_NUMBER changed (ND6-100N -> ND6-100N, NB7-1U -> NB7-1U-25V)	AJuvancic	A
23.04.2020	Solder jumpers (J1V1, J1V15, J3V3, J2V5, JVLCS, JVCCD_1_5, JODRV_33V) replaced with 0R resistors. Capacitors package changed from 1210 to 0805 (C326, C337)	AJuvancic	B
06.05.2020	Jumper SJMP2 replaced with two 0805 resistors (SJMP2 and SJMP2/2)	AJuvancic	B
08.05.2020	Jumper SJMP2 Mounted status moved from DNP to mounted	AJuvancic	B
12.05.2020	Solder jumpers Mounted status moved from DNP to mounted (J1V1, J1V15, J3V3, J2V5, JVLCS, JVCCD_1_5, JODRV_33V)	AJuvancic	B

Value	Capacitors used
12p	0402, 50V, C0G, 1%
22p	0402, 50V, C0G, 1%
10n	0402, 25V, X7R, 10%
100n	0402, 25V, X7R, 10%
1u	0603, 16V, X7R, 10%
2.2u	1210, 100V, X7R, 10%
10u	1210, 25V, X7R, 10%
22u	1210, 10V, X7R, 10%
100u	1210, 10V, X5R, 20%

All resistors are SMD 0402, 63mW, 1% except where marked differently.

Components marked DNP (Do Not Place) are foreseen for testing purposes.

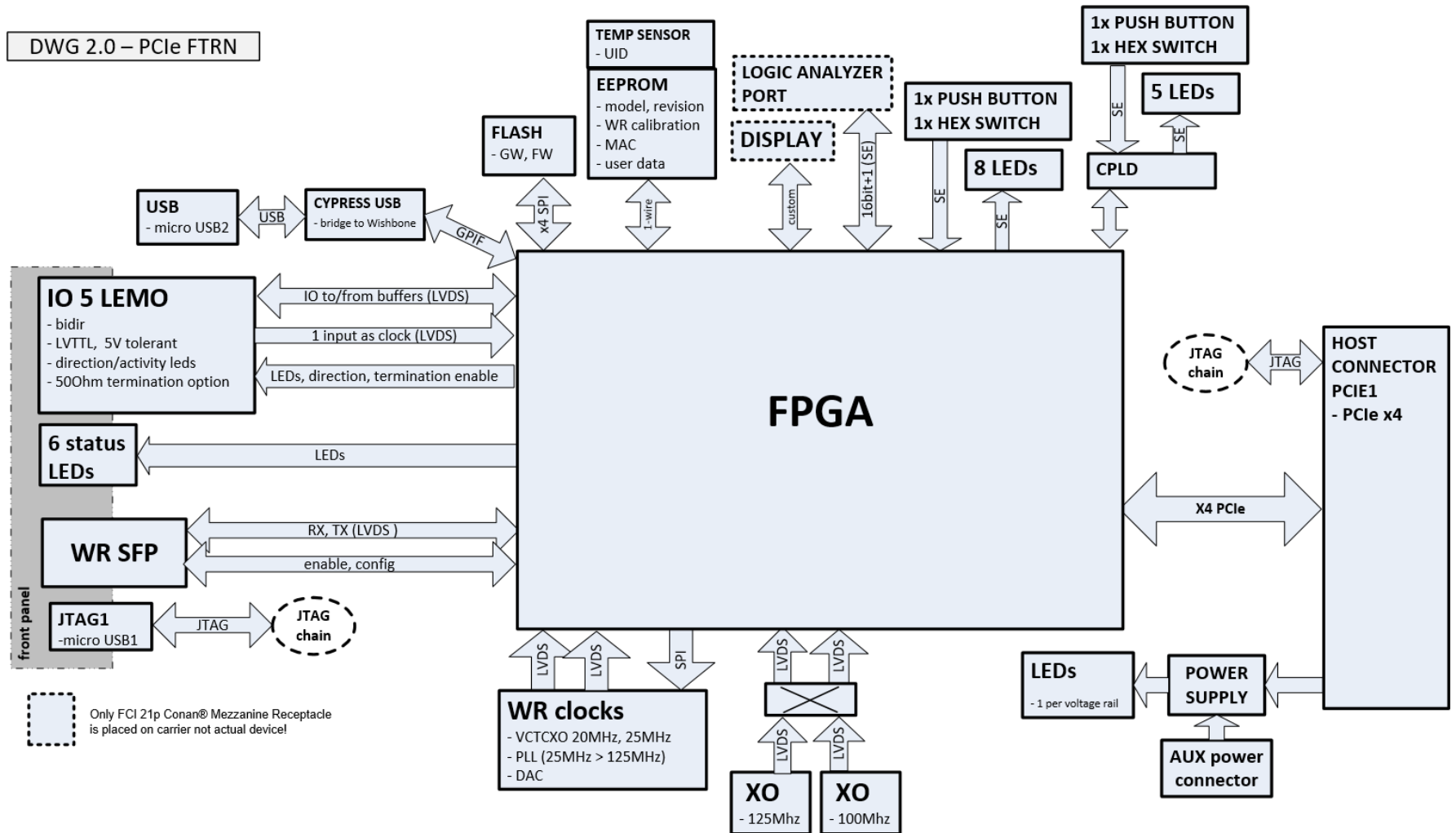


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DRAWN	Dušan Slavinec, Marko Levicnik		11.09.2019
CHECKED	Marko Levicnik		
APPROVED	Gregor Cuk		
		Title FAIR Timing Receiver (FTRN) PCIe form factor - CSL_FTRN_PCIe	
Size	A3	Type	SE
DWG.NO.	CSL_FTRN_PCIe		
			REV. B
			SHEET 1 OF 13

Block Diagram

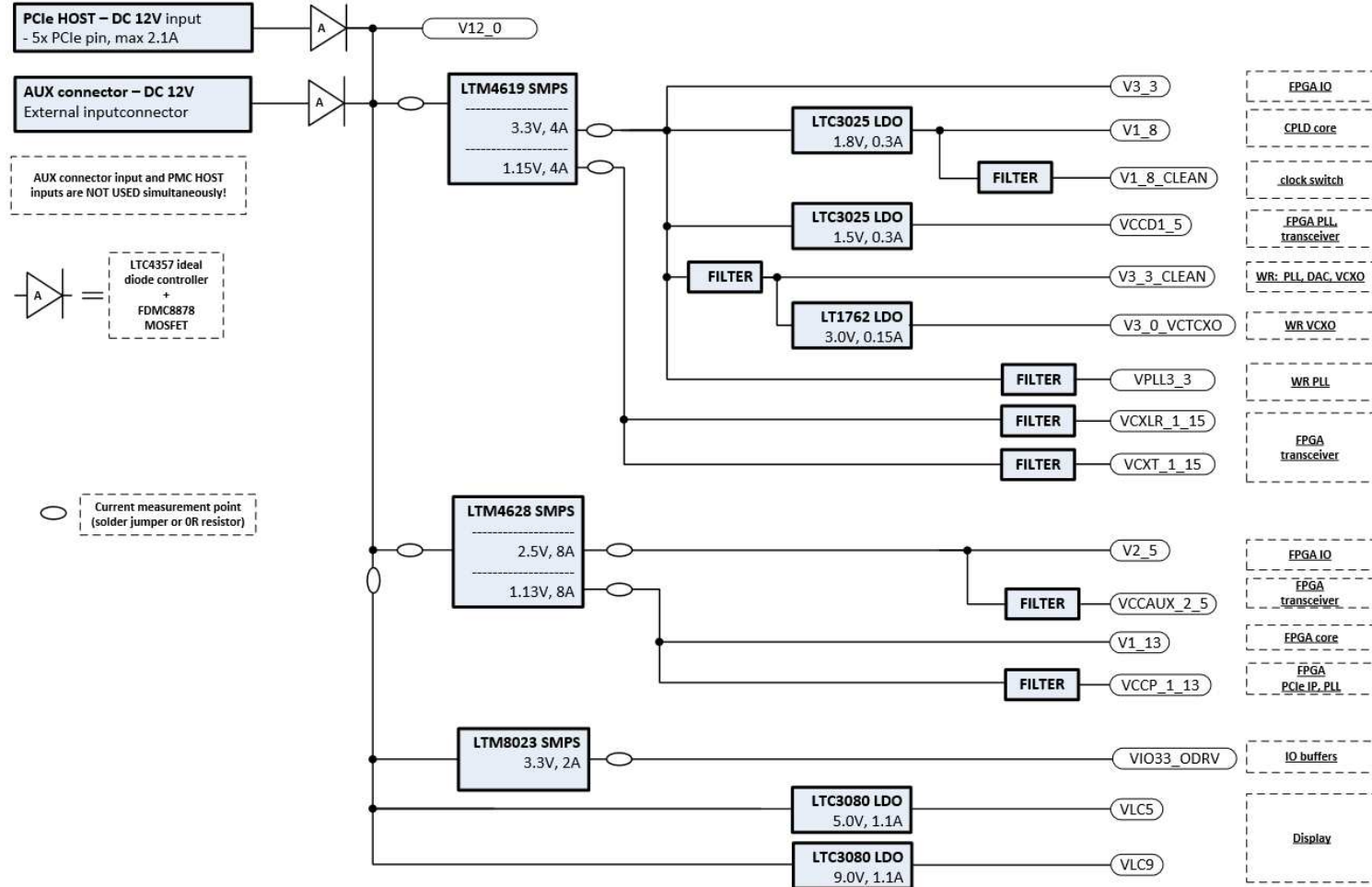


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Title Block Diagram			
Size A3	Type SE	DWG.NO. CSL_FTRN_PCle	REV. A
			SHEET 2 OF 13

Power tree block scheme

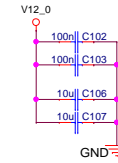
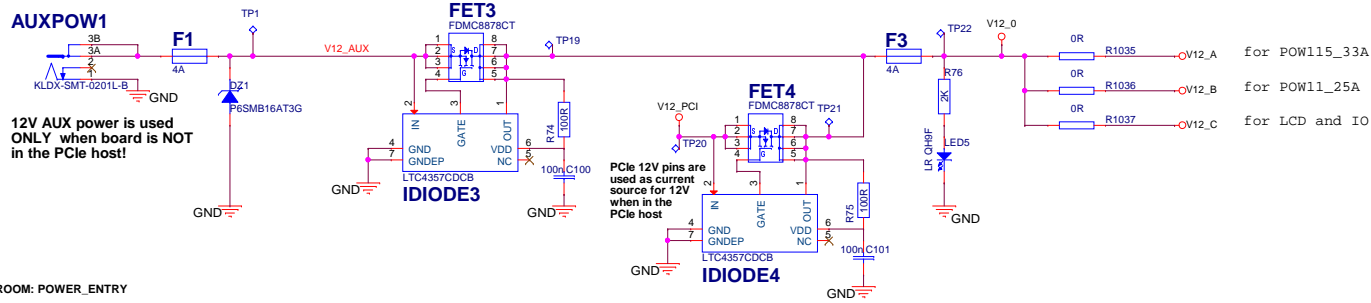


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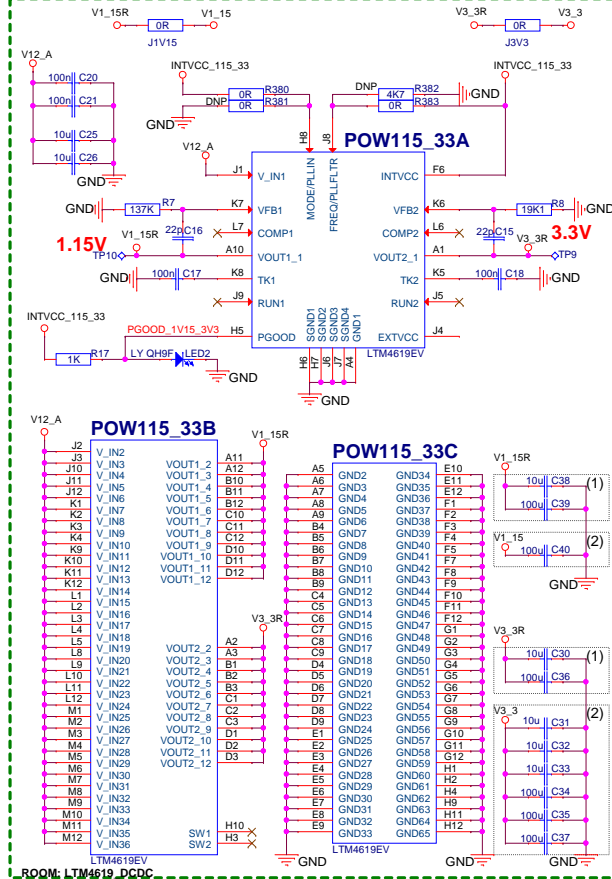
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Title				
Power tree block scheme				
Size	Type	DWG.NO.		REV.
A3	SE	CSL_FTRN_PcIe		A
SHEET				
3				OF 13

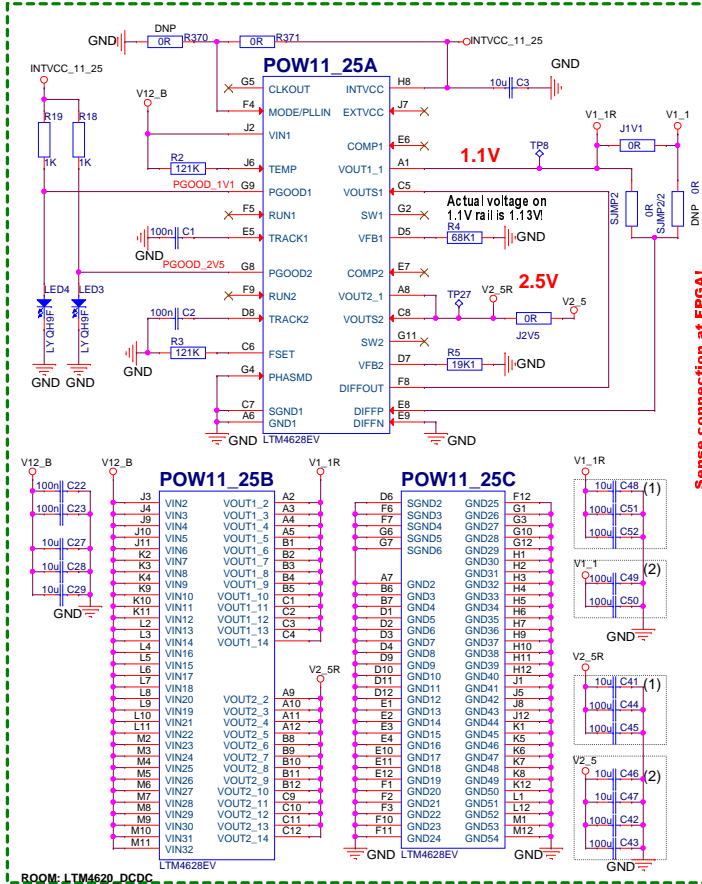
Power entry and main DCDC power regulators



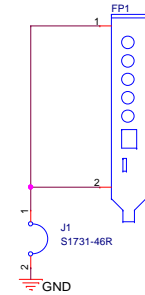
LTM4619 input Voltage Range: 4.5V to 26.5V



LTM4628 input Voltage Range: 4.5V to 16V



Optional PCIe bezel connection to GND



- (1) - place capacitors at the regulator outputs
- (2) - place capacitors away from the regulator outputs

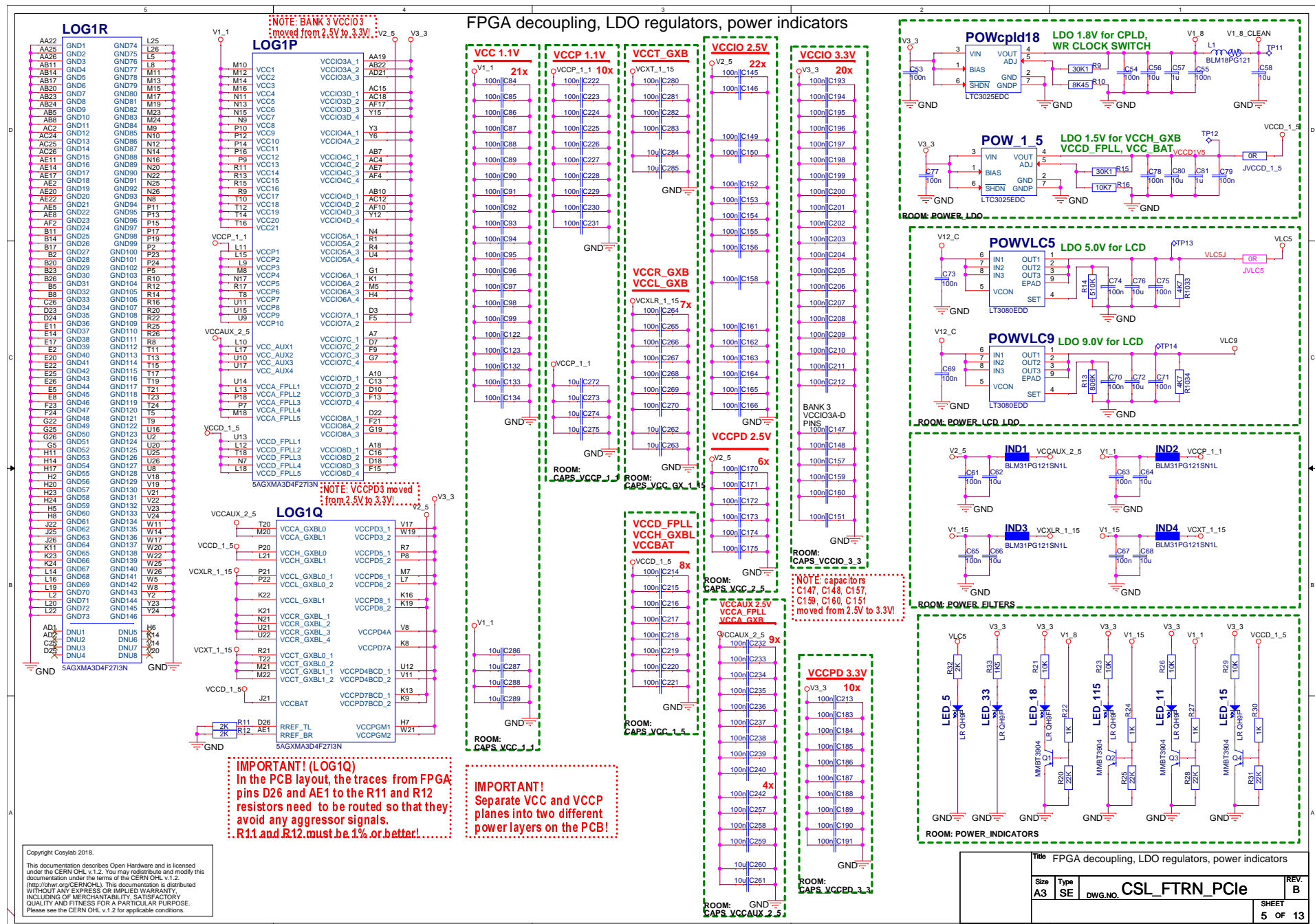
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Title Power entry and main DCDC power regulators

Size A3 Type SE DWG.No. CSL_FTRN_PcIe

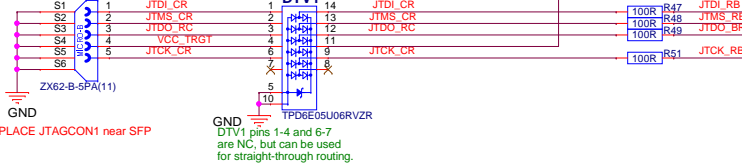
REV. B

SHEET 4 OF 13



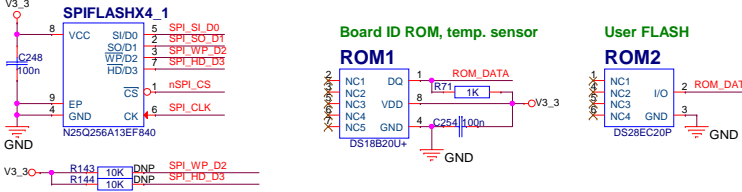
FPGA and CPLD JTAG, FPGA gateway FLASH, User Flash

Micro USB JTAG connector JTAGCON1

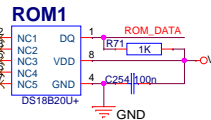


ROOM: JTAG INPUT

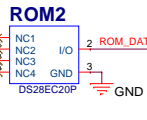
FPGA configuration FLASH



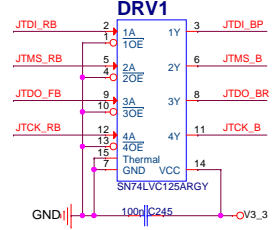
Board ID ROM, temp. sensor



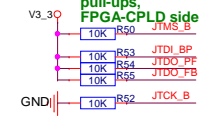
User FLASH



JTAG buffer and protection



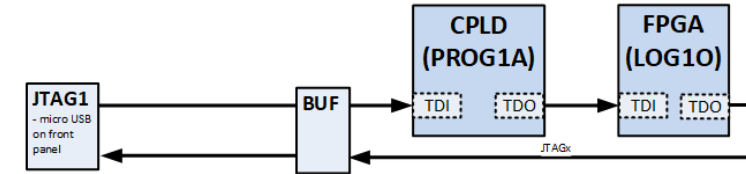
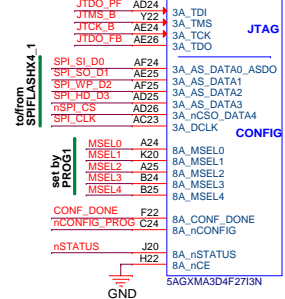
JTAG signal pull-ups, FPGA-CPLD side



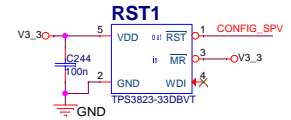
JTAG signal pull-ups, connector side



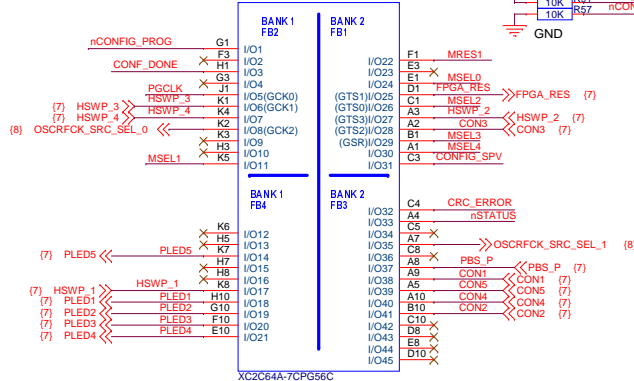
FPGA configuration and JTAG LOG10



Reset supervisors

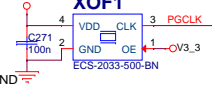


PROG1C

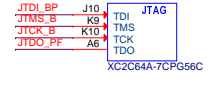


ROOM: PROG_CPLD

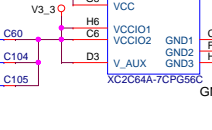
XOF1



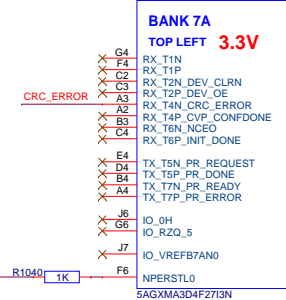
PROG1A



PROG1B



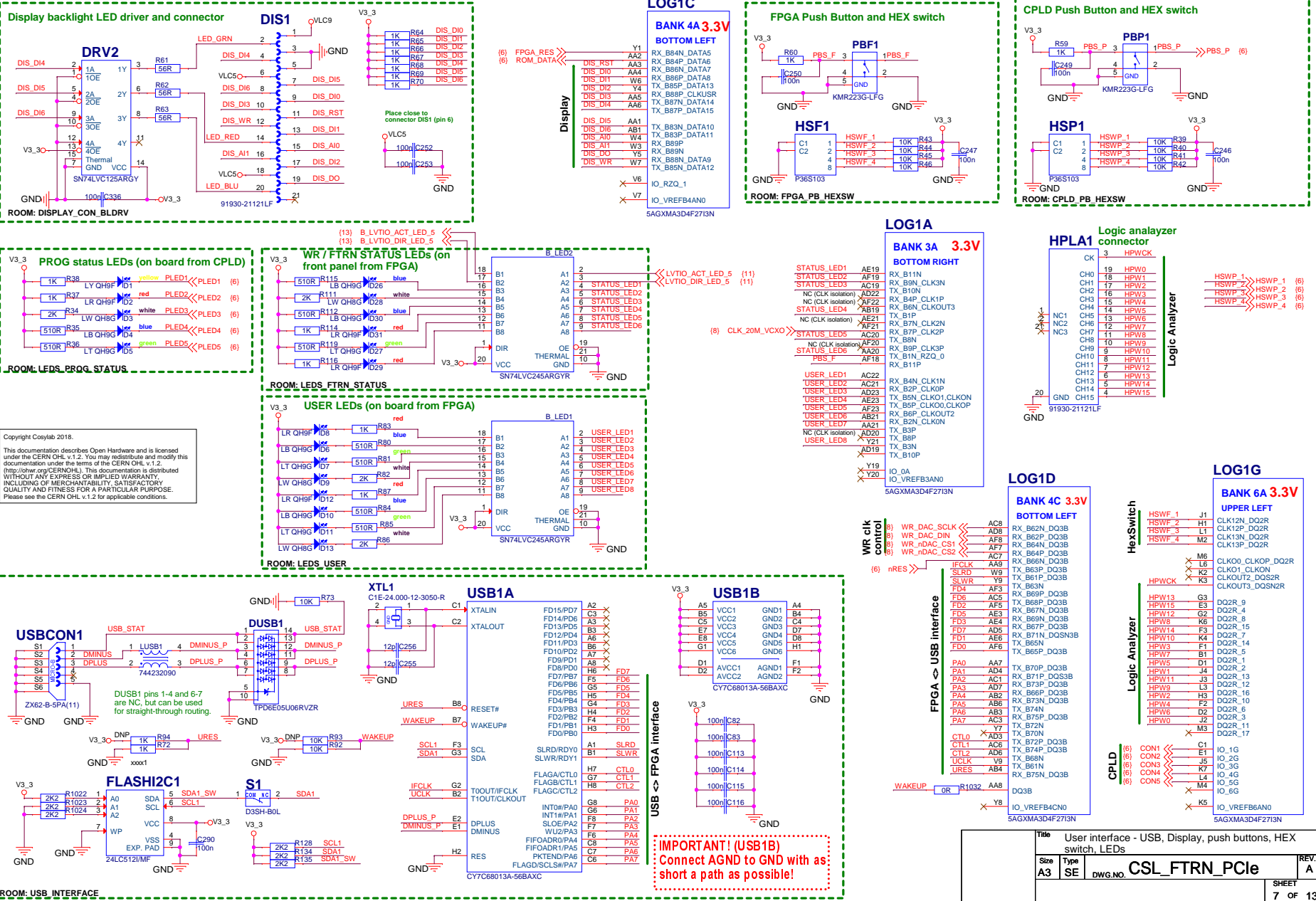
LOG1H

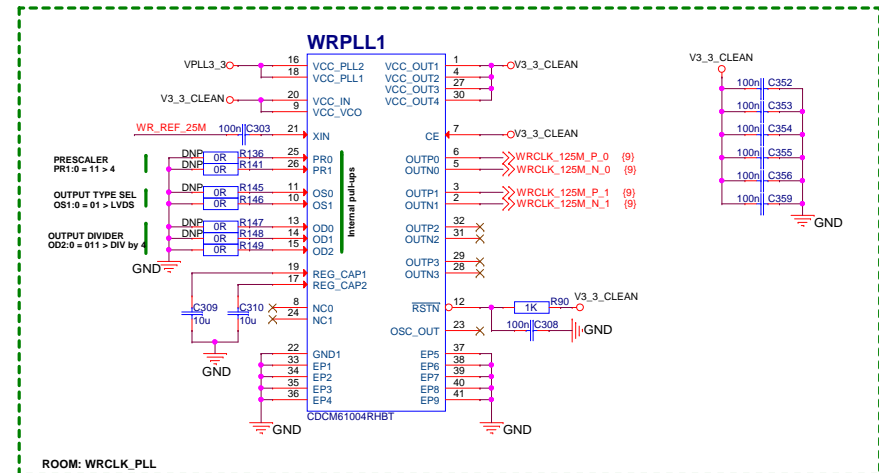
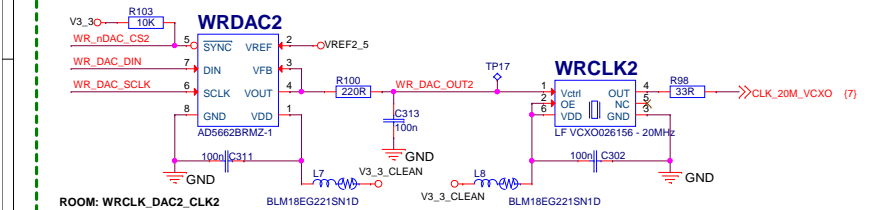
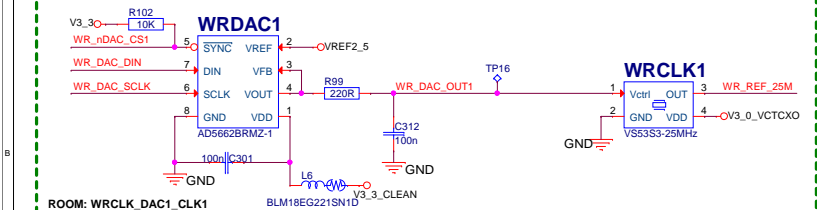
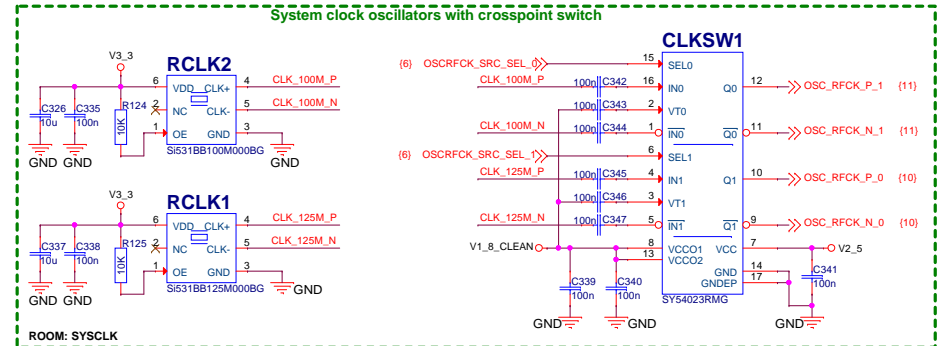
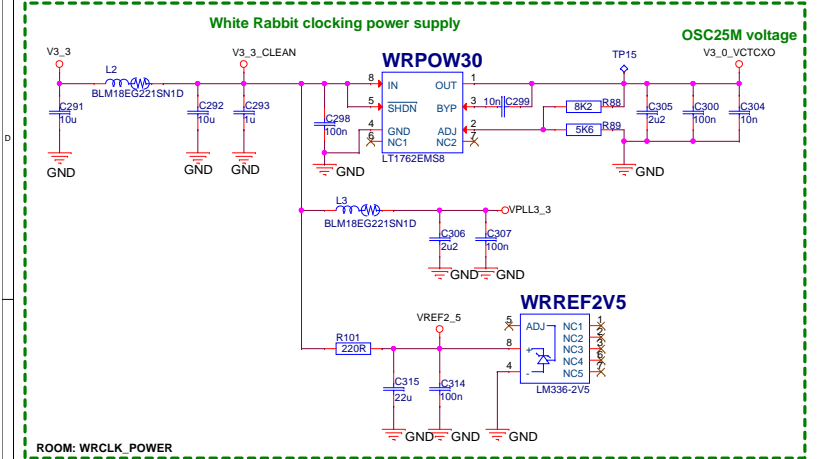


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Title		FPGA and CPLD JTAG, FPGA gateway FLASH, User Flash		REV.	A
Size	A3	Type	SE	DWG.No.	CSL_FTRN_PcIe
SHEET					6 OF 13

User interface - USB, Display, push buttons, HEX switch, LEDs



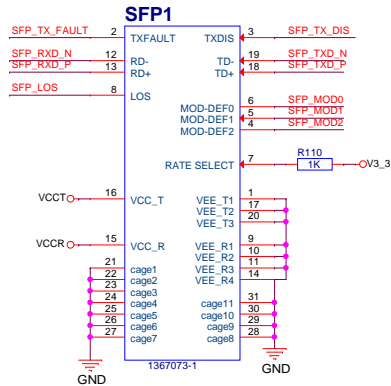
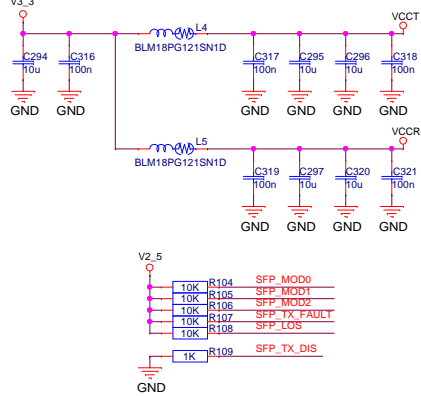


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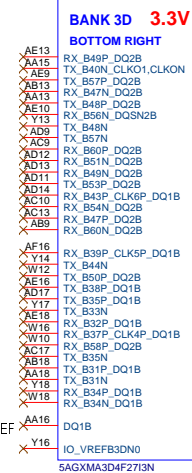
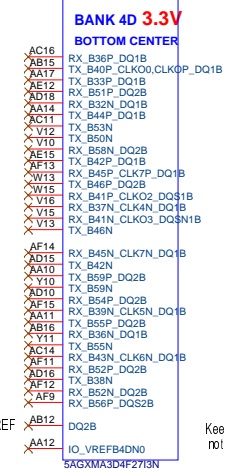
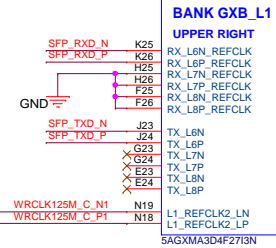
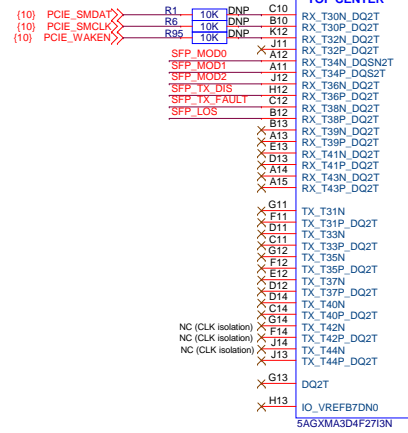
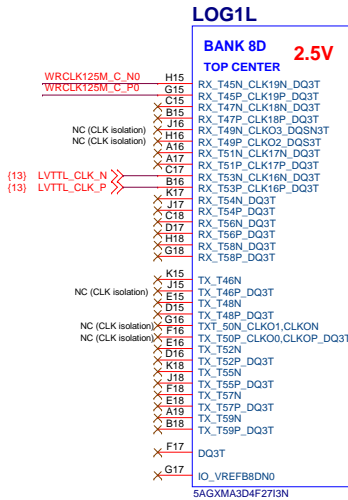
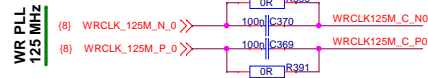
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Title		Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch	
Size	Type	CSL_FTRN_PCle	REV.
A3	SE		B
DWG.NO.		SHEET 8 OF 13	

Fiber SFP, PCI <> FPGA connections



Place resistor footprint over capacitor (optional AC-coupling)
Only resistors will be placed!



Keep DQ and
not connected

Keep DQ and IO_VREF
not connected

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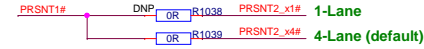
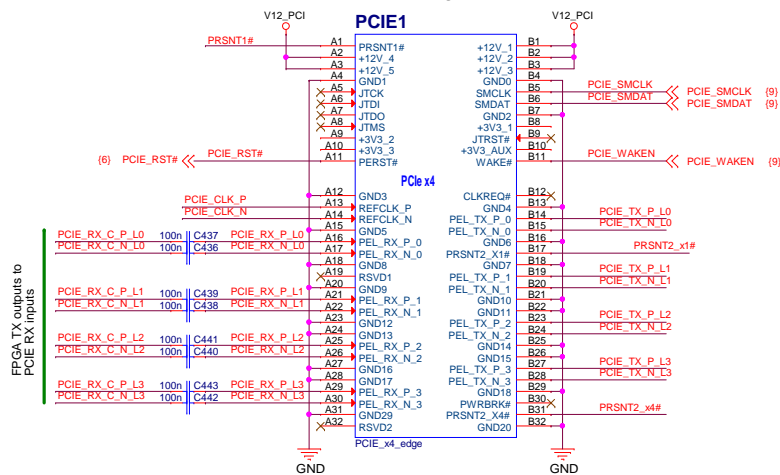
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Title	Fiber SFP, PCI <> FPGA connections
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Size A3	Type SE	DWG.NO. CSL_FTRN_PCle	REV. A
			SHEET 9 OF 13

PCIe host interface

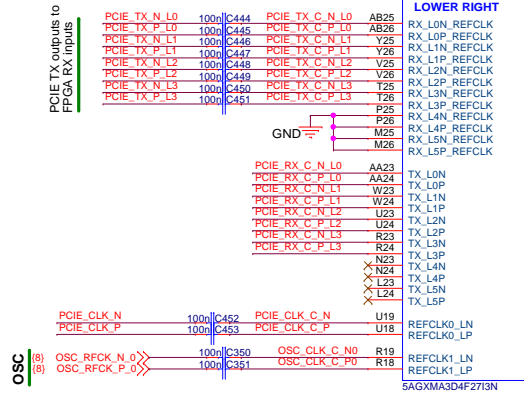
PCIe x4 PCB edge connector



LOG1M

BANK GXB_I

LOWER RIGHT



https://en.wikipedia.org/wiki/PCI_Express#Pinout

Pin	Side B	Side A	Description
1	+12 V	PRNST1#	Must connect to farthest PRNST2# pin
2	+12 V	+12 V	Main power pins
3	+12 V	+12 V	
4	Ground	Ground	
5	SMCLK	TCK	SMBus and JTAG port pins
6	SMDAT	TDI	
7	Ground	TDO	
8	+3.3 V	TMS	
9	TRST#	+3.3 V	Standby power
10	+3.3 V aux	+3.3 V	
11	WAKE#	PERST#	Link reactivation; fundamental reset

Key notch

12	CLKREQ# ^[14]	Ground	Clock Request Signal
13	Ground	REFCLK+	Reference clock differential pair
14	HSOp(0)	REFCLK-	Lane 0 transmit data, + and -
15	HSOn(0)	Ground	
16	Ground	HSIp(0)	Lane 0 receive data, + and -
17	PRSENTZ#	HSIn(0)	
18	Ground	Ground	

PCI Express x1 cards end at pin 18

19	HSOp(1)	Reserved	Lane 1 transmit data, + and -
20	HSOn(1)	Ground	
21	Ground	HSIp(1)	Lane 1 receive data, + and -
22	Ground	HSIn(1)	
23	HSOp(2)	Ground	Lane 2 transmit data, + and -
24	HSOn(2)	Ground	
25	Ground	HSIp(2)	Lane 2 receive data, + and -
26	Ground	HSIn(2)	
27	HSOp(3)	Ground	Lane 3 transmit data, + and -
28	HSOn(3)	Ground	
29	Ground	HSIp(3)	Lane 3 receive data, + and -
30	PWRBRK# ^[15]	HSIn(3)	
31	PRSENTZ#	Ground	
32	Ground	Reserved	

PCI Express x4 cards end at pin 32

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	Title				PCIe host interface	
	Size	Type	DWG.NO. CSL_FTRN_PCIe			REV.
	A3	SE				A
						SHEET 10 OF 13

IO block power supply, FPGA <=> IO block connections

(12) LVTTIO_OUT_P_1 << LVTTIO_OUT_P_1
(12) LVTTIO_OUT_N_1 << LVTTIO_OUT_N_1
(12) #LVTTIO_OE_1 << #LVTTIO_OE_1
(12) LVTTIO_IN_P_1 << LVTTIO_IN_P_1
(12) LVTTIO_IN_N_1 << LVTTIO_IN_N_1
(12) LVTTIO_TERM_EN_1 << LVTTIO_TERM_EN_1
(12) LVTTIO_DIR_LED_1 << LVTTIO_DIR_LED_1
(12) LVTTIO_ACT_LED_1 << LVTTIO_ACT_LED_1

(12) LVTTIO_OUT_P_2 << LVTTIO_OUT_P_2
(12) LVTTIO_OUT_N_2 << LVTTIO_OUT_N_2
(12) #LVTTIO_OE_2 << #LVTTIO_OE_2
(12) LVTTIO_IN_P_2 << LVTTIO_IN_P_2
(12) LVTTIO_IN_N_2 << LVTTIO_IN_N_2
(12) LVTTIO_TERM_EN_2 << LVTTIO_TERM_EN_2
(12) LVTTIO_DIR_LED_2 << LVTTIO_DIR_LED_2
(12) LVTTIO_ACT_LED_2 << LVTTIO_ACT_LED_2

(12) LVTTIO_OUT_P_3 << LVTTIO_OUT_P_3
(12) LVTTIO_OUT_N_3 << LVTTIO_OUT_N_3
(12) #LVTTIO_OE_3 << #LVTTIO_OE_3
(12) LVTTIO_IN_P_3 << LVTTIO_IN_P_3
(12) LVTTIO_IN_N_3 << LVTTIO_IN_N_3
(12) LVTTIO_TERM_EN_3 << LVTTIO_TERM_EN_3
(12) LVTTIO_DIR_LED_3 << LVTTIO_DIR_LED_3
(12) LVTTIO_ACT_LED_3 << LVTTIO_ACT_LED_3

(13) LVTTIO_OUT_P_4 << LVTTIO_OUT_P_4
(13) LVTTIO_OUT_N_4 << LVTTIO_OUT_N_4
(13) #LVTTIO_OE_4 << #LVTTIO_OE_4
(13) LVTTIO_IN_P_4 << LVTTIO_IN_P_4
(13) LVTTIO_IN_N_4 << LVTTIO_IN_N_4
(13) LVTTIO_TERM_EN_4 << LVTTIO_TERM_EN_4
(12) LVTTIO_DIR_LED_4 << LVTTIO_DIR_LED_4
(12) LVTTIO_ACT_LED_4 << LVTTIO_ACT_LED_4

(13) LVTTIO_OUT_P_5 << LVTTIO_OUT_P_5
(13) LVTTIO_OUT_N_5 << LVTTIO_OUT_N_5
(13) #LVTTIO_OE_5 << #LVTTIO_OE_5
(13) LVTTIO_IN_P_5 << LVTTIO_IN_P_5
(13) LVTTIO_IN_N_5 << LVTTIO_IN_N_5
(13) LVTTIO_TERM_EN_5 << LVTTIO_TERM_EN_5
(7) LVTTIO_DIR_LED_5 << LVTTIO_DIR_LED_5
(7) LVTTIO_ACT_LED_5 << LVTTIO_ACT_LED_5

LOG1F

BANK 5A
LOWER LEFT

3.3V

LVTTIO control signals

#LVTTIO_OE_1 N5
LVTTIO_TERM_EN_1 P1
LVTTIO_ACT_LED_1 P3
#LVTTIO_OE_2 R2
LVTTIO_TERM_EN_2 R3
LVTTIO_DIR_LED_2 T1
LVTTIO_ACT_LED_2 T2
#LVTTIO_OE_3 T3
LVTTIO_TERM_EN_3 T6
LVTTIO_ACT_LED_3 U1
LVTTIO_DIR_LED_3 T7
#LVTTIO_OE_4 U5
LVTTIO_TERM_EN_4 V1
LVTTIO_ACT_LED_4 V4
LVTTIO_DIR_LED_4 V5
#LVTTIO_OE_5 W1
LVTTIO_TERM_EN_5 W2
LVTTIO_ACT_LED_5 N6
LVTTIO_DIR_LED_5 P4
#LVTTIO_IN_CLK_EN << #LVTTIO_IN_CLK_EN
#LVTTIO_IN_CLK_EN << #LVTTIO_IN_CLK_EN

IO_1F
IO_2F
IO_3F
IO_4F
IO_5F
IO_6F
IO_7F
U3 DQSN1R
U3 DQS1R
U7 IO_VREFB8A0
5AGXMA3D4F2713N

LOG1I

BANK 7C
TOP LEFT 2.5V

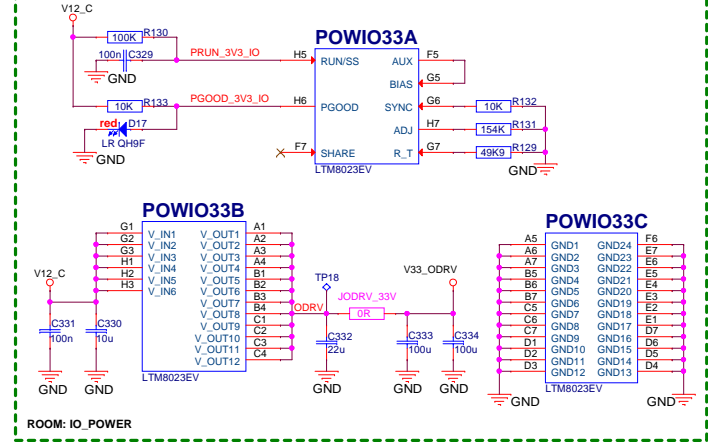
LVTTIO data inputs

LVTTIO_IN_N_1 A6
LVTTIO_IN_P_1 A5
LVTTIO_IN_P_2 C6
LVTTIO_IN_N_2 B6
LVTTIO_IN_N_3 E6
LVTTIO_IN_P_3 D6
LVTTIO_IN_N_4 F7
LVTTIO_IN_P_4 E7
LVTTIO_IN_N_5 H9
LVTTIO_IN_P_5 G9
LVTTIO_IN_N_6 D8
LVTTIO_IN_P_6 C8
LVTTIO_IN_N_7 E9
LVTTIO_IN_P_7 D9
LVTTIO_IN_N_8 H10
LVTTIO_IN_P_8 G10
LVTTIO_IN_N_9 A9
LVTTIO_IN_P_9 A8
LVTTIO_IN_N_10 C7
LVTTIO_IN_P_10 B7
LVTTIO_IN_N_11 D5
LVTTIO_IN_P_11 C5
LVTTIO_IN_N_12 G8
LVTTIO_IN_P_12 F8
LVTTIO_IN_N_13 J8
LVTTIO_IN_P_13 J9
LVTTIO_IN_N_14 K10
LVTTIO_IN_P_14 J10
LVTTIO_IN_N_15 C9
LVTTIO_IN_P_15 B9
LVTTIO_IN_N_16 E10
LVTTIO_IN_P_16 D10
LVTTIO_IN_N_17 F10

LVTTIO data outputs

LVTTIO_OUT_N_1 A9
LVTTIO_OUT_P_1 A8
LVTTIO_OUT_N_2 C7
LVTTIO_OUT_P_2 B7
LVTTIO_OUT_N_3 D5
LVTTIO_OUT_P_3 C5
LVTTIO_OUT_N_4 G8
LVTTIO_OUT_P_4 F8
LVTTIO_OUT_N_5 J8
LVTTIO_OUT_P_5 J9
LVTTIO_OUT_N_6 K10
LVTTIO_OUT_P_6 J10
LVTTIO_OUT_N_7 C9
LVTTIO_OUT_P_7 B9
LVTTIO_OUT_N_8 E10
LVTTIO_OUT_P_8 D10
LVTTIO_OUT_N_9 F10

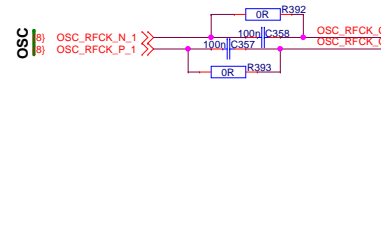
Power supply for output drivers



LOG1K

BANK 8A
TOP RIGHT 2.5V

Place resistor footprint over capacitor (optional AC-coupling)
Only resistors will be placed!



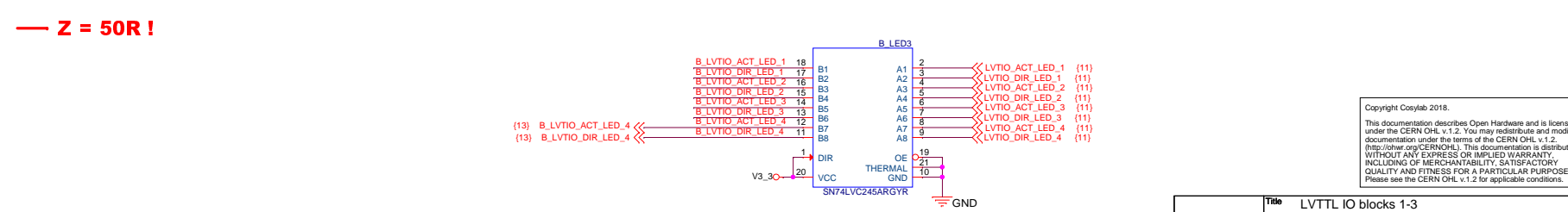
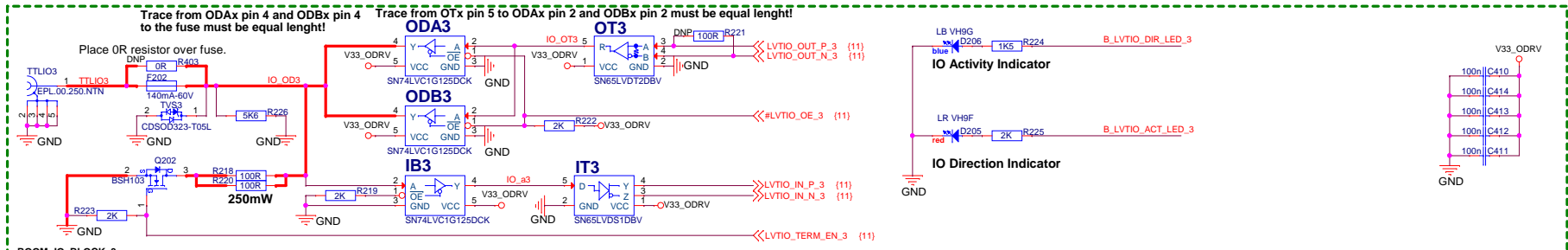
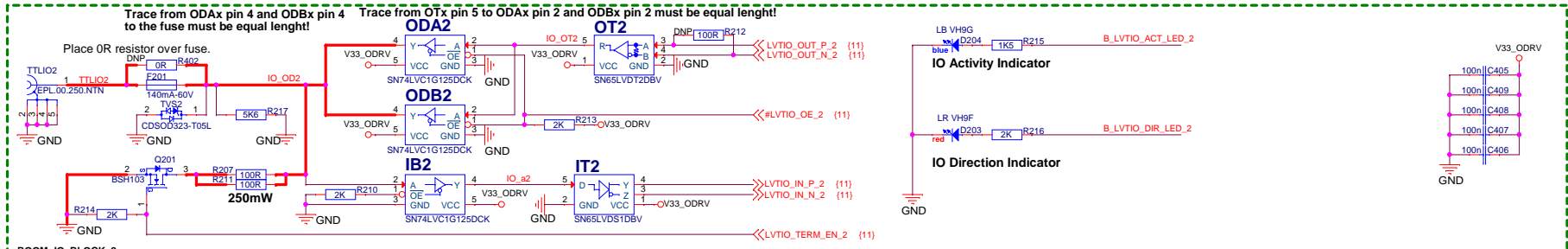
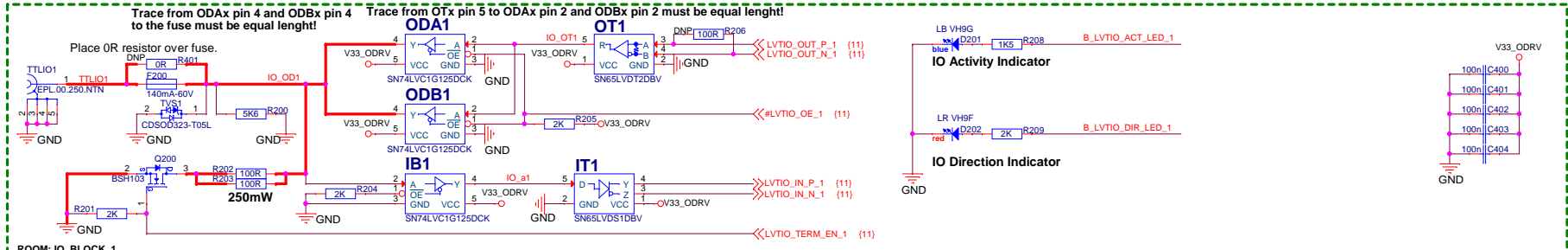
A23 RX_T86N_CLK21N
A21 RX_T86P_CLK21P
D21 TX_T82P
E21 TX_T86P
E21 TX_T89N_RZQ_6
A20 TX_T85P_CLK00_CLKOP
C19 RX_T81P_CLK23P
C19 RX_T79P
D20 TX_T87P
C22 RX_T84N_CLKOUT3
C22 RX_T88N_CLK20N
C23 RX_T88P_CLK20P
B19 RX_T81N_CLK23N
F19 TX_T80N
E19 TX_T80P
J19 TX_T87N
B21 RX_T83P_CLK22P
D19 RX_T79N
A22 TX_T85N_CLK01_CLKON
C21 TX_T82N
C21 RX_T83N_CLK22N
C20 RX_T84P_CLKOUT2
F20 IO_OK
G20 IO_VREFB8A0
5AGXMA3D4F2713N

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Title				REV	
IO block power supply, FPGA <=> IO block connections				B	
Size	Type	DWG.No.		SHEET	
A3	SE	CSL_FTRN_PcIe		11 of 13	

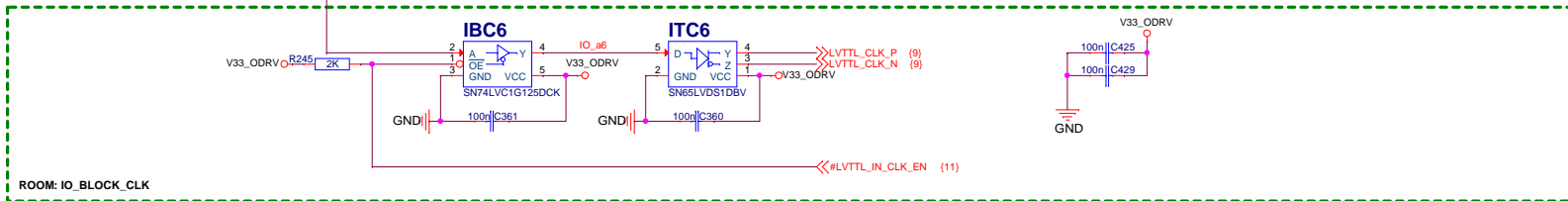
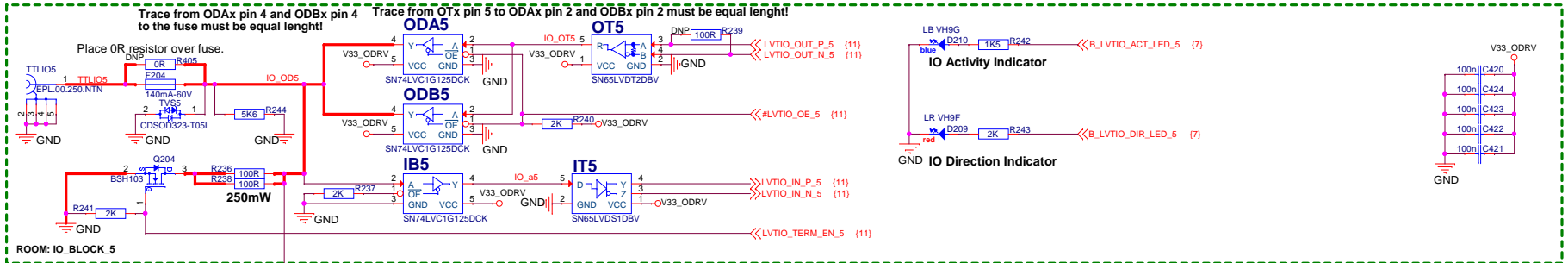
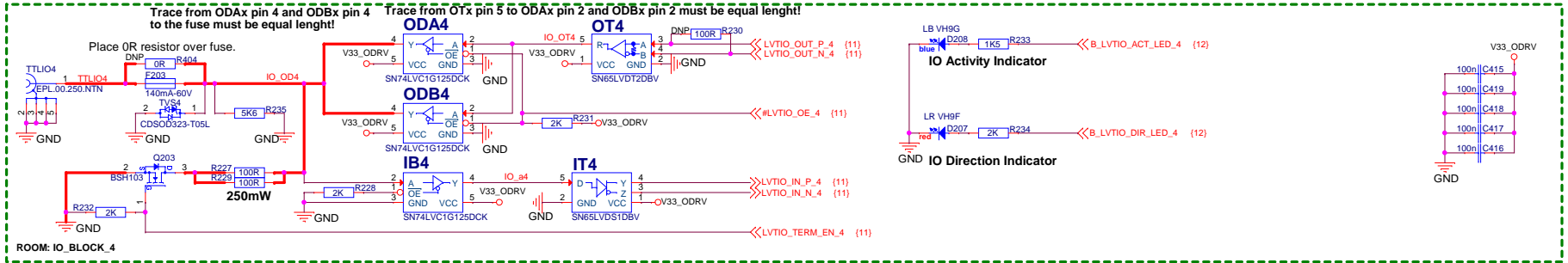
* - IO overvoltage protection bias circuit is based OHWR FMC-DIO-SCHTTLA

LVTTTL IO blocks 1-3



	Title				LVTTTL IO blocks 1-3			
	Size A3	Type SE	DWG.NO.	CSL_FTRN_PcIe				REV. A
							SHEET	
							12 OF	13

LVTTTL IO blocks 4-5, IO CLOCK input



— Z = 50R!

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Title		LVTTTL IO blocks 4-5, IO CLOCK input		
Size	Type	DWG.NO.		REV.
A3	SE	CSL_FTRN_PCle		A
SHEET				13 OF 13