FAIR Timing Receiver AMC form factor - CSL_FTRN_AMC
Single width, mid-height

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DATE	REVISION DESCRIPTION	DRAWN	REV
01.09.2014	Initial version	dslavinec	A
19.09.2014	Flattened IO blocks	dslavinec	A
02.12.2014	Updates after QA review	dslavinec	A
16.04.2015	Added ADC clock generation and trigger signals to backplane, moved LVTTL_CLK, nRES and FPGA_RES to different FPGA pins	dslavinec	A
23.07.2015	removed ADC clocking page, only one set of triggers to backplane kept, incorporated changes from PMC (LED driving), added power mux for MMC	dslavinec	A
17.08.2015	added sheet 15 with MTCA.4 triggers and clocks to/from backplane	dslavinec	A
01.10.2015	MTCA.4 out clocks not connected to clk outputs, backplane buffers enable signals connected only to FPGA	dslavinec	A
27.11.2015	MTCA.4 connections to backplane finished, MMC PGOOD modified, relevant updates from PMC, MMC reset modified	dslavinec	A
09.12.2015	MTCA.4 HSS connections (backplane ports 12-15) moved from FPGA GXB banks to LVDS IOs	dslavinec	A
16.12.2015	libera triggers, MTCA.4 tclk and mlvdios moved to top FPGA banks	dslavinec	A
16.06.2016	LTM4620 replaced with LTM4619, FPGA core voltage increased to 1.15V, different TCLK buffers, larger LED resistors, replaced IO TVS	dslavinec	A
26.07.2017	one LTM4619 reverted back to LTM4620, added resistors for LTM mode configuration, modified JTAG chain connections, added JTAG switch indicator, WR/STATUS LEDs replaced with 90deg, WR and OSC clk lines back to AC-coupling	dslavinec	A

Value	Capatitors used
12p	0402, 50V, C0G, 1%
22p	0402, 50V, C0G, 1%
10n	0402, 25V, X7R, 10%
100n	0402, 25V, X7R, 10%
1u	0603, 16V, X7R, 10%
2.2u	1210, 100V, X7R, 10%
10u	1210, 25V, X7R, 10%
22u	1210, 10V, X7R, 10%
100u	1210, 10V, X5R, 20%

All resistors are SMD 0402, 63mW, 1% except where marked differently.

Components marked DNP (Do Not Place) are foreseen for testing purposes and should NOT be placed.

TOP layer

FM1	FM2	FM3
FIDUCIAL	FIDUCIAL	FIDUCIAL

BOTTOM layer

FM4	FM5	FM6
FIDUCIAL	FIDUCIAL	FIDUCIAL

DRAWN	Dušan Slavinec		01.09.2014
CHECKED	-		
APPROVED	-		

Title

Size	Type	DWG.NO.	REV.
A3	SE	CSL_FTRN_AMC	A

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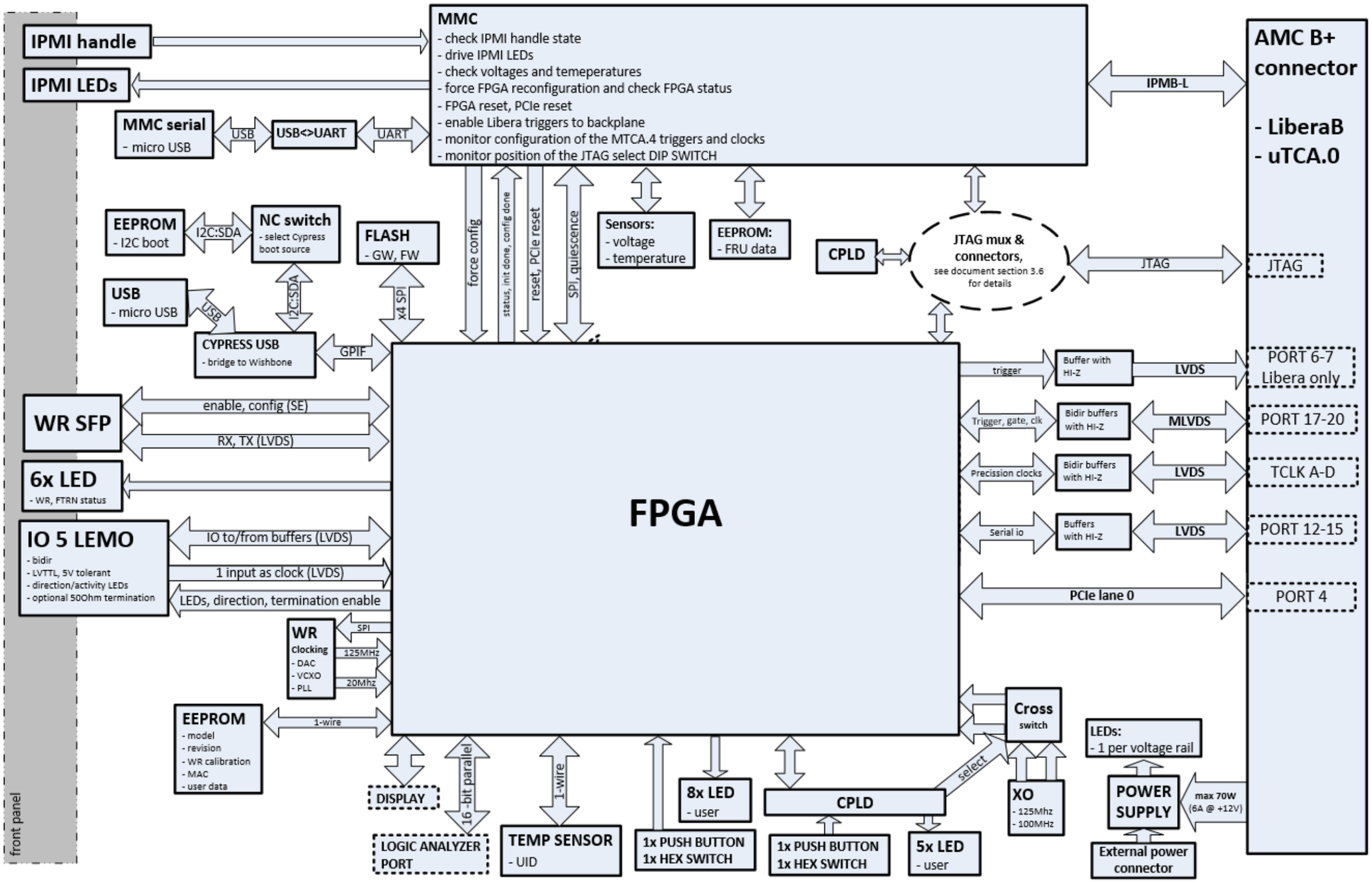
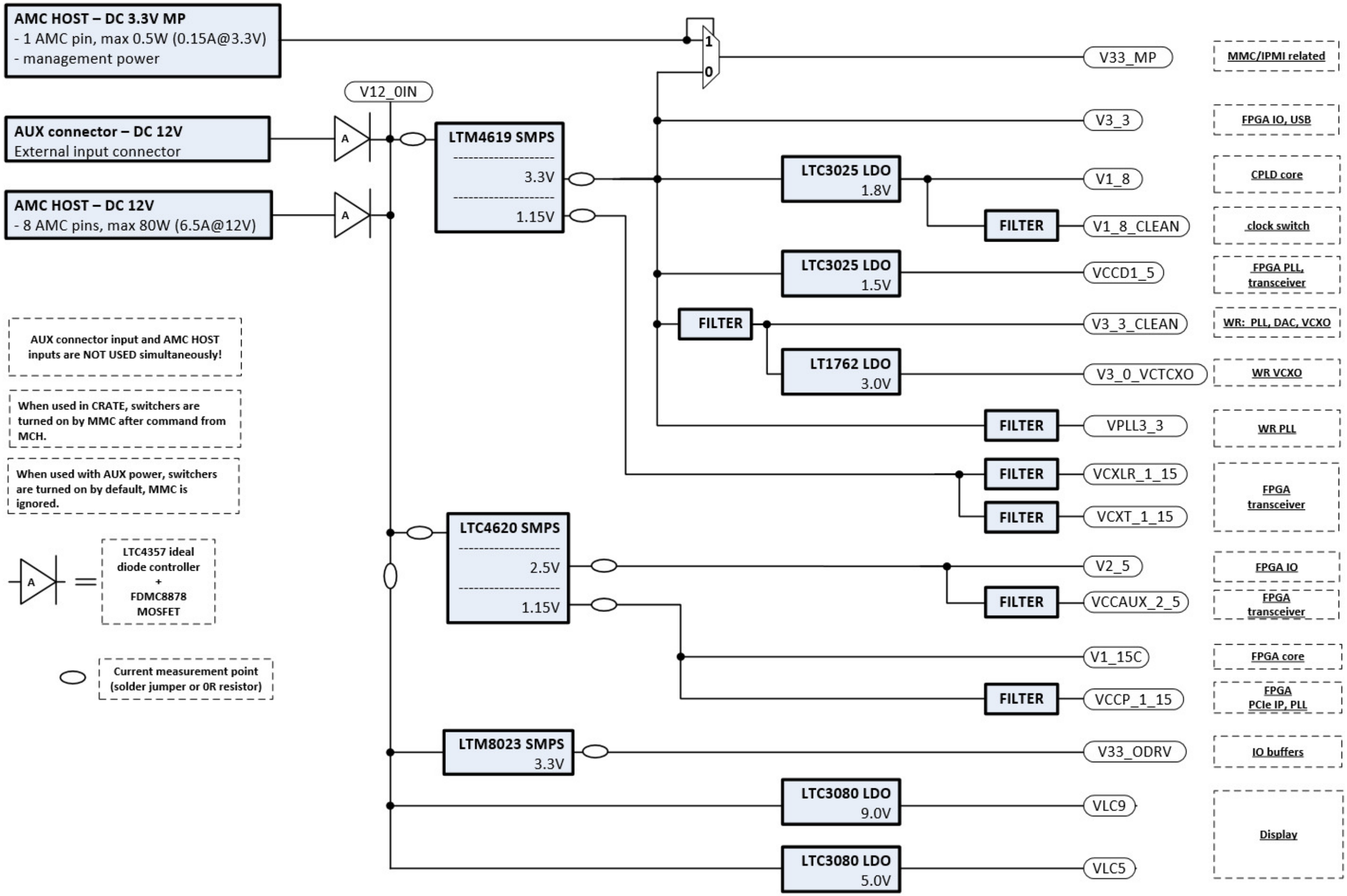
Block Diagram - FTRN, MMC



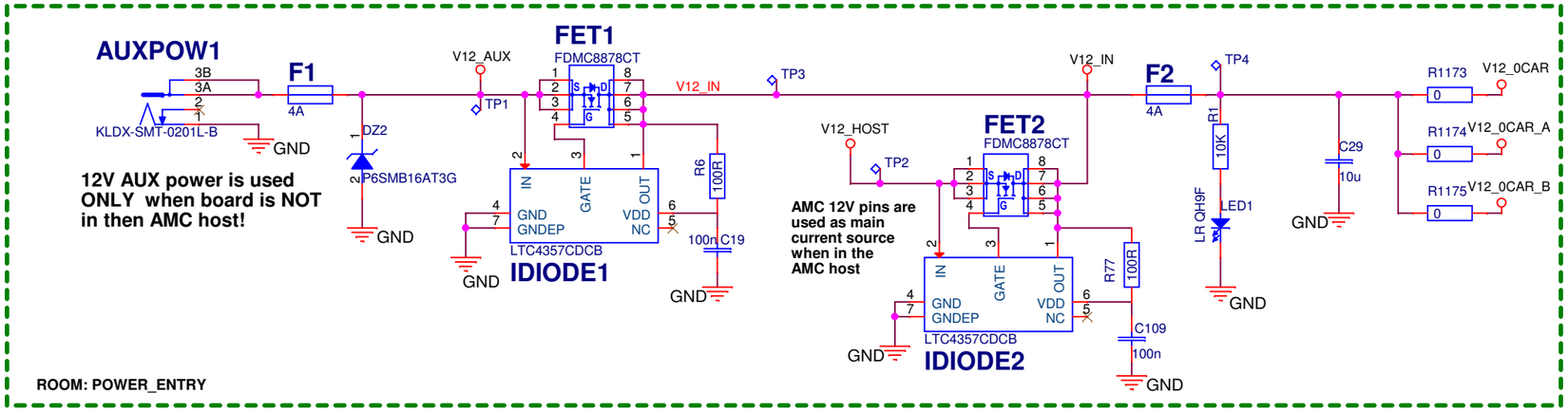
Title	Block Diagram - FTRN, MMC		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 2 OF 17

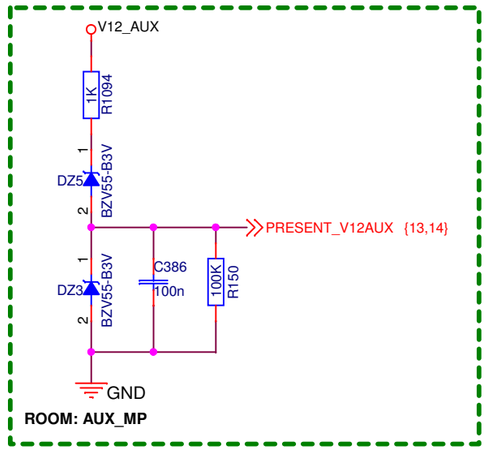
Power tree block scheme



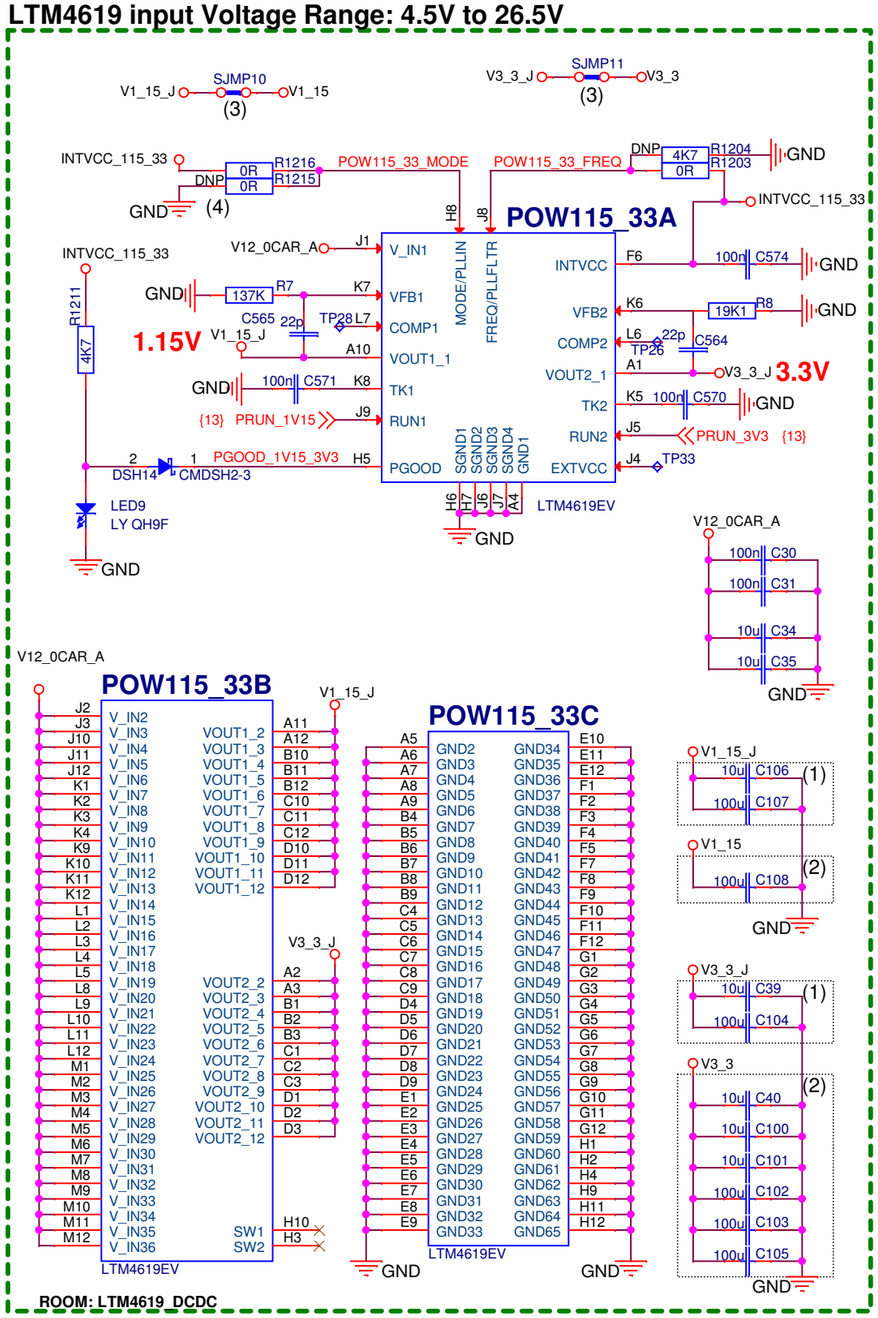
Title	Power tree block scheme		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 3 OF 17	

Power entry and main DCDC power regulators

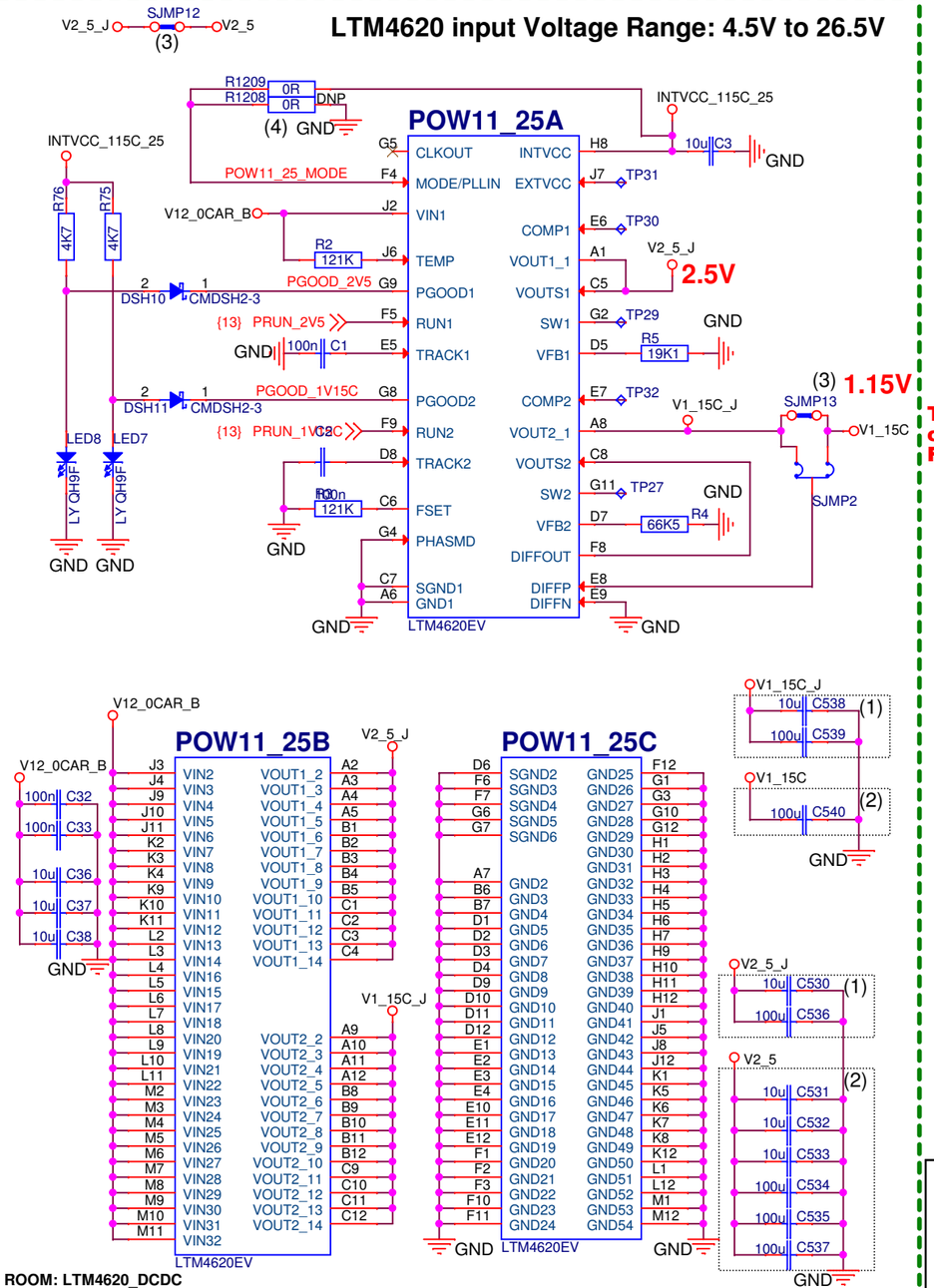




LTM4619 input Voltage Range: 4.5V to 26.5V



LTM4620 input Voltage Range: 4.5V to 26.5V



(1) - place capacitors on the regulator outputs

(2) - place capacitors away from the regulator outputs

(3) - solder jumper, to test power regulator outputs before powering FPGA and current measurement

(4) - None or only one resistor is placed to select converter mode (pulse-skipping, burst, continous)

Title: Power entry and main DCDC power regulators			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 4 OF 17	

FPGA decoupling, LDO regulators, power indicators

LOG1R

AA22	GND1	GND74	L25
AA25	GND2	GND75	L5
AA26	GND3	GND76	L8
AB11	GND4	GND77	M11
AB14	GND5	GND78	M13
AB17	GND6	GND79	M15
AB20	GND7	GND80	M17
AB23	GND8	GND81	M19
AB24	GND9	GND82	M23
AB5	GND10	GND83	M24
AB8	GND11	GND84	M9
AC2	GND12	GND85	N10
AC24	GND13	GND86	N12
AC25	GND14	GND87	N14
AC26	GND15	GND88	N16
AE11	GND16	GND89	N20
AE14	GND17	GND90	N22
AE17	GND18	GND91	N25
AE2	GND19	GND92	N26
AE20	GND20	GND93	N8
AE22	GND21	GND94	P11
AE5	GND22	GND95	P13
AE8	GND23	GND96	P15
AF2	GND24	GND97	P17
B11	GND25	GND98	P19
B14	GND26	GND99	P2
B17	GND27	GND100	P23
B2	GND28	GND101	P24
B20	GND29	GND102	P5
B23	GND30	GND103	R10
B26	GND31	GND104	R12
B5	GND32	GND105	R14
B8	GND33	GND106	R16
C26	GND34	GND107	R20
D23	GND35	GND108	R22
D24	GND36	GND109	R25
E11	GND37	GND110	R26
E14	GND38	GND111	R8
E17	GND39	GND112	T11
E2	GND40	GND113	T13
E20	GND41	GND114	T15
E22	GND42	GND115	T17
E25	GND43	GND116	T19
E26	GND44	GND117	T21
E5	GND45	GND118	T23
E8	GND46	GND119	T24
F23	GND47	GND120	T5
F24	GND48	GND121	T9
G22	GND49	GND122	U16
G25	GND50	GND123	U2
G26	GND51	GND124	U20
G5	GND52	GND125	U25
H11	GND53	GND126	U26
H14	GND54	GND127	U8
H17	GND55	GND128	V18
H2	GND56	GND129	V19
H20	GND57	GND130	V21
H23	GND58	GND131	V22
H24	GND59	GND132	V23
H5	GND60	GND133	V24
H8	GND61	GND134	W11
J22	GND62	GND135	W14
J25	GND63	GND136	W17
J26	GND64	GND137	W20
K11	GND65	GND138	W22
K23	GND66	GND139	W25
K24	GND67	GND140	W26
L14	GND68	GND141	W5
L16	GND69	GND142	W8
L19	GND70	GND143	Y2
L2	GND71	GND144	Y23
L20	GND72	GND145	Y24
L22	GND73	GND146	
AD1	DNU1	DNU5	H6
AD2	DNU2	DNU6	K14
C25	DNU3	DNU7	V14
D25	DNU4	DNU8	V20

5AGXMA3D4F27I3N

GND

LOG1P

V1_15C, V2_5, V3_3

M10	VCC1	VCCIO3A_1	AA19
M12	VCC2	VCCIO3A_2	AB22
M14	VCC3	VCCIO3A_3	AD21
M16	VCC4	VCCIO3D_1	AC15
N11	VCC5	VCCIO3D_2	AC18
N13	VCC6	VCCIO3D_3	AF17
N15	VCC7	VCCIO3D_4	Y15
N9	VCC8		
P10	VCC9	VCCIO4A_1	Y3
P12	VCC10	VCCIO4A_2	Y6
P14	VCC11		
P16	VCC12	VCCIO4C_1	AB7
P9	VCC13	VCCIO4C_2	AC4
R11	VCC14	VCCIO4C_3	AE7
R13	VCC15	VCCIO4C_4	AF4
R15	VCC16		
R9	VCC17	VCCIO4D_1	AB10
T10	VCC18	VCCIO4D_2	AC12
T12	VCC19	VCCIO4D_3	AF10
T14	VCC20	VCCIO4D_4	Y12
T16	VCC21		
		VCCIO5A_1	N4
VCCP_1_15		VCCIO5A_2	R1
L11	VCCP1	VCCIO5A_3	R4
L15	VCCP2	VCCIO5A_4	U4
L9	VCCP3		
M8	VCCP4	VCCIO6A_1	G1
N17	VCCP5	VCCIO6A_2	K1
R17	VCCP6	VCCIO6A_3	M5
T8	VCCP7	VCCIO6A_4	H4
U11	VCCP8		
U15	VCCP9	VCCIO7A_1	D3
U9	VCCP10	VCCIO7A_2	F5
VCCAUX_2_5			
L10	VCC_AUX1	VCCIO7C_1	A7
L17	VCC_AUX2	VCCIO7C_2	D7
U10	VCC_AUX3	VCCIO7C_3	F9
U17	VCC_AUX4	VCCIO7C_4	G7
		VCCIO7D_1	A10
U14	VCCA_FPLL1	VCCIO7D_2	C13
L13	VCCA_FPLL2	VCCIO7D_3	D10
P18	VCCA_FPLL3	VCCIO7D_4	F13
P7	VCCA_FPLL4		
M18	VCCA_FPLL5	VCCIO8A_1	D22
VCCD_1_5		VCCIO8A_2	F21
U13	VCCD_FPLL1	VCCIO8A_3	G19
L12	VCCD_FPLL2		
T18	VCCD_FPLL3	VCCIO8D_1	A18
N7	VCCD_FPLL4	VCCIO8D_2	C16
L18	VCCD_FPLL5	VCCIO8D_3	D18
		VCCIO8D_4	F15

5AGXMA3D4F27I3N

LOG1Q

VCCAUX_2_5, V2_5, V3_3

T20	VCCA_GXBL0	VCCPD3_1	V17
M20	VCCA_GXBL1	VCCPD3_2	W19
VCCD_1_5			
P20	VCCH_GXBL0	VCCPD5_1	R7
L21	VCCH_GXBL1	VCCPD5_2	P8
VCXLR_1_15			
P21	VCCL_GXBL0_1	VCCPD6_1	M7
P22	VCCL_GXBL0_2	VCCPD6_2	L7
K22	VCCL_GXBL1	VCCPD8_1	K16
		VCCPD8_2	K19
K21	VCCR_GXBL_1		
N21	VCCR_GXBL_2		
U21	VCCR_GXBL_3	VCCPD4A	V8
U22	VCCR_GXBL_4		
		VCCPD7A	K8
VCXT_1_15			
R21	VCCT_GXBL0_1		
T22	VCCT_GXBL0_2		
M21	VCCT_GXBL1_1	VCCPD4BCD_1	U12
M22	VCCT_GXBL1_2	VCCPD4BCD_2	V11
VCCD_1_5			
J21		VCCPD7BCD_1	K13
	VCCBAT	VCCPD7BCD_2	K9
2K R11	D26		
2K R12	AE1	RREF_TL	H7
		RREF_BR	VCCPGM1 W21
			VCCPGM2

5AGXMA3D4F27I3N

GND

IMPORTANT! (LOG1Q)
In the PCB layout, the traces from FPGA pins D26 and AE1 to the R11 and R12 resistors need to be routed so that they avoid any aggressor signals.
R11 and R12 must be 1% or better!

IMPORTANT!
Separate VCC and VCCP planes into two different power layers on the PCB!

VCC 1.15V

V1_15C, 21x

100n C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C122, C123, C132, C133, C134

GND

VCCP 1.15V

V1_15C, 10x

100n C135, C136, C137, C138, C139, C140, C141, C142, C143, C144

10u C286, C287, C288, C289

GND

ROOM: CAPS_VCC_1_1

VCCP 1.15V

VCCP_1_15, 10x

100n C222, C223, C224, C225, C226, C227, C228, C229, C230, C231

GND

ROOM: CAPS_VCCP_1_1

VCCP 1.15V

VCCP_1_15

100n C276, C277, C278, C279

10u C272, C273, C274, C275

GND

VCCT_GXB

VCXT_1_15

100n C280, C281, C282, C283

10u C284, C285

GND

VCCR_GXB VCCL_GXB

VCXLR_1_15, 7x

100n C264, C265, C266, C267, C268, C269, C270

10u C262, C263

GND

ROOM: CAPS_VCC_GX_1_15

VCCIO 2.5V

V2_5, 22x

100n C145, C146, C147, C148, C149, C150, C151, C152, C153, C154, C155, C156, C157, C158, C159, C160, C161, C162, C163, C164, C165, C166

GND

VCCPD 2.5V

V2_5, 6x

100n C170, C171, C172, C173, C174, C175

GND

ROOM: CAPS_VCC_2_5

VCCD_FPLL VCCH_GXBL VCCBAT

VCCD_1_5, 8x

100n C214, C215, C216, C217, C218, C219, C220, C221

GND

ROOM: CAPS_VCC_1_5

VCCAUX 2.5V VCCA_FPLL VCCA_GXB

VCCAUX_2_5, 9x

100n C232, C233, C234, C235, C236, C237, C238, C239, C240

4x

100n C242, C257, C258, C259

10u C260, C261

GND

ROOM: CAPS_VCCAUX_2_5

VCCIO 3.3V

V3_3, 20x

100n C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C211, C212

GND

ROOM: CAPS_VCCIO_3_3

VCCPD 3.3V

V3_3, 10x

100n C213, C183, C184, C185, C186, C187, C188, C189, C190, C191

GND

ROOM: CAPS_VCCPD_3_3

POWcpld18 — LDO 1.8V for CPLD, WR CLOCK SWITCH

V3_3 → C53 100n → LTC3025EDC (VIN, VOUT, ADJ, BIAS, GND, SHDN, GNDP)
ADJ: 30K1 R9 + 8K45 R10
V1_8_J — SJMP5 (1) — V1_8 — L1 BLM18PG121 — V1_8_CLEAN
C54 100n, C56 10u, C57 1u, C55 100n, C58 10u
TP11
GND

POW_1_5 — LDO 1.5V for VCCH_GXB VCCD_FPLL, VCC_BAT

V3_3 → C77 100n → LTC3025EDC (VIN, VOUT, ADJ, BIAS, GND, SHDN, GNDP)
ADJ: 30K1 R15 + 10K7 R16
TP12 — VCCD_1_5_J — SJMP6 (1) — VCCD_1_5
C78 100n, C80 10u, C81 1u, C79 100n
GND

ROOM: POWER_LDO

POWVLC5 — LDO 5.0V for LCD

V12_0CAR → C73 100n → LT3080EDD (IN1, IN2, IN3, VCON, OUT1, OUT2, OUT3, EPAD, SET)
R14 510K
TP13 — VLC5_J — SJMP7 (1) — VLC5
C74 100n, C76 10u, C75 100n
GND

POWVLC9 — LDO 9.0V for LCD

V12_0CAR → C69 100n → LT3080EDD (IN1, IN2, IN3, VCON, OUT1, OUT2, OUT3, EPAD, SET)
R13 806K
VLC9 — TP14
C70 100n, C72 10u, C71 100n
GND

ROOM: POWER_LCD_LDO

IND1 / IND2 / IND3 / IND4

IND1: V2_5 → C61 100n, C62 10u → VCCAUX_2_5 (BLM31PG121SN1L)
IND2: V1_15C → C63 100n, C64 10u → VCCP_1_15 (BLM31PG121SN1L)
IND3: V1_15 → C65 100n, C66 10u → VCXLR_1_15 (BLM31PG121SN1L)
IND4: V1_15 → C67 100n, C68 10u → VCXT_1_15 (BLM31PG121SN1L)
GND

ROOM: POWER_FILTERS

LED_5 / LED_33 / LED_18 / LED_115 / LED_11 / LED_15

	VLC5	V3_3	V12_IN	V1_8	V12_IN	V1_15	V12_IN	V1_15C	V12_IN	VCCD_1_5
R	R32 2K	R33 1K5	R21 10K		R23 10K		R26 10K		R29 10K	
LED	LED_5	LED_33	LED_18		LED_115		LED_11		LED_15	
LED	LR QH9F	LR QH9F	LR QH9F		LR QH9F		LR QH9F		LR QH9F	
Q			Q1 MMBT3904		Q2 MMBT3904		Q3 MMBT3904		Q4 MMBT3904	
R			R22 1K	R20 22K	R24 1K	R25 22K	R27 1K	R28 22K	R30 1K	R31 22K

GND

ROOM: POWER_INDICATORS

(1) - 0R solder connection, to test regulator outputs before connecting to load

Title	FPGA decoupling, LDO regulators, power indicators		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 5 OF 17

FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash

JTAG signals flow :
C (USB connector) > R (resistor) > B (buffer) > P (PROG - CPLD) > F (FPGA) > B > C
or
BPL (backplane) > BB (backplane buffer) > BS (backplane JTAG switch) > R (resistor) > P (PROG - CPLD) > F (FPGA) > R > BS > BB > BPL

JTAG connector
(on the front panel if possible)

JTAGCON1
ZX62-B-5PA(11)
MICRO-B
S1 S2 S3 S4 S5 S6
1 JTDI_CR
2 JTMS_CR
3 JTDO_RC
4 VCC_TRGT
5 JTCK_CR
GND

DTV1
TPD6E05U06RVZR
1 2 3 4 5 6 7 8 9 10 11 12 13 14
GND

V3_3
VCC_TRGT 1 DSH1 2 CMDSH2-3

JTDI_CR 100R R47 JTDI_RB
JTMS_CR 100R R48 JTMS_RB
JTDO_RC 100R R49 JTDO_BR
JTCK_CR 100R R51 JTCK_RB

Straight-through Routing

FPGA/CPLD JTAG master select (DIP1, p14):
DIP1 = HI, FPGA/CPLD JTAG from backplane
DIP1 = LO, FPGA/CPLD JTAG from front panel connector
{13,14} JTAGSW_SEL

Parallel to USB connector JTAG signals are JTAG signals from JSW1 swtich (JTAG from backplane)

JTCK_B 0R R1220 JTCK_SR {14}
JTMS_B 0R R1219 JTMS_SR {14}
JTDI_BP 0R R1218 JTDI_SR {14}
JTDO_FB 0R R1217 JTDO_RS {14}

JTAG buffer and protection

DRV1
SN74LVC125ARGY
1A 1OE 2A 2OE 3A 3OE 4A 4OE
1Y 2Y 3Y 4Y
GND VCC THERMAL
JTDI_RB 2 1 JTDI_BP 3
JTMS_RB 5 4 JTMS_B 6
JTDO_FB 9 10 JTDO_BR 8
JTCK_RB 12 13 JTCK_B 11
7 15 14
GND
100n C245
V3_3

V3_3
10K R50 JTMS_B
10K R53 JTDI_BP
10K R54 JTDO_PF
10K R55 JTDO_FB
GND
10K R52 JTCK_B

JTAG signal pull-ups

V3_3
10K R78 JTDI_RB
10K R91 JTMS_RB
GND
10K R79 JTCK_RB

ROOM: FPGA_CPLD_JTAG_INPUT

LOG1O
5AGXMA3D4F27I3N
JTAG
JTDO_PF AD24 3A_TDI
JTMS_B Y22 3A_TMS
JTCK_B AE24 3A_TCK
JTDO_FB AE26 3A_TDO

to/from SPIFLASHX4_1
SPI_SI_D0_FPGA AF24 3A_AS_DATA0_ASDO
SPI_SO_D1_FPGA AE25 3A_AS_DATA1
SPI_WP_D2_FPGA AF25 3A_AS_DATA2
SPI_HD_D3_FPGA AD25 3A_AS_DATA3
nSPI_CS_FPGA AD26 3A_nCSO_DATA4
SPI_CLK_FPGA AC23 3A_DCLK

CONFIG
set by PROG1
MSEL0 A24 8A_MSEL0
MSEL1 K20 8A_MSEL1
MSEL2 A25 8A_MSEL2
MSEL3 B24 8A_MSEL3
MSEL4 B25 8A_MSEL4
CONF_DONE F22 8A_CONF_DONE
nCONFIG C24 8A_nCONFIG
nSTATUS J20 8A_nSTATUS
H22 8A_nCE
GND

nCONFIG_PROG
#MMC_FPGA_CONFIG 0R R193 0R R194 nCONFIG

IC3
SN74LVC1G97DCK
nCONFIG_PROG 3 IN0
1 IN1
{13} #MMC_FPGA_CONFIG 6 IN2
Y 4 nCONFIG
GND 2 VCC 5 V3_3
Y = IN0 AND IN2
GND
C322 100n

FPGA status to MMC
CONF_DONE CONF_DONE {13}

SPIFLASHX4_1
N25Q256A13EF840
V3_3
C248 100n
VCC SI/D0 SO/D1 WP/D2 HD/D3 CS EP GND CK
SPI_SI_D0_FPGA
SPI_SO_D1_FPGA
SPI_WP_D2_FPGA
SPI_HD_D3_FPGA
nSPI_CS_FPGA
SPI_CLK_FPGA
GND
V3_3
R143 10K DNP SPI_WP_D2_FPGA
R144 10K DNP SPI_HD_D3_FPGA

ROOM: MEMORY

{7} ROM_DATA ROM_DATA
1-wire

ROM1
DS18B20U+
NC1 NC2 NC3 NC4 NC5 DQ VDD GND
ROM_DATA
R71 1K
V3_3
C254 100n
GND

ROM2
DS28EC20P
NC1 NC2 NC3 NC4 I/O GND
2 ROM_DATA
3
GND

PROG1C
XC2C64A-7CPG56C
BANK 1 FB2
BANK 2 FB1
BANK 1 FB4
BANK 2 FB3
I/O1 I/O2 I/O3 I/O4 I/O5(GCK0) I/O6(GCK1) I/O7 I/O8(GCK2) I/O9 I/O10 I/O11
I/O12 I/O13 I/O14 I/O15 I/O16 I/O17 I/O18 I/O19 I/O20 I/O21
I/O22 I/O23 I/O24 (GTS1)I/O25 (GTS0)I/O26 (GTS3)I/O27 (GTS2)I/O28 (GSR)I/O29 I/O30 I/O31
I/O32 I/O33 I/O34 I/O35 I/O36 I/O37 I/O38 I/O39 I/O40 I/O41 I/O42 I/O43 I/O44 I/O45

nCONFIG_PROG G1
CONF_DONE H1
PGCLK J1
HSWP_3 K1
HSWP_4 K4
{7} HSWP_3
{7} HSWP_4
{8} OSCRFCK_SRC_SEL_0 K2
MSEL1 K3
H3
K5
K6
PLED5 H5
{7} PLED5 K7
H7
HSWP_1 H8
{7} HSWP_1 K8
PLED1 H10
{7} PLED1
PLED2 G10
{7} PLED2
PLED3 F10
{7} PLED3
PLED4 E10
{7} PLED4

F1 MRES1
E3
E1 MSEL0
D1 FPGA_RES
C1 MSEL2
A3 HSWP_2
A2 CON3
B1 MSEL3
A1 MSEL4
C3 CONFIG_SPV
C4 A4 nSTATUS CRC_ERROR {10}
C5
A7 OSCRFCK_SRC_SEL_1 {8}
C8
A8 PBS_P
A9 CON1
A5 CON5
A10 CON4
B10 CON2
C10
D8
E8
D10

V3_3
10K R56 CONF_DONE
10K R57 CRC_ERROR
10K R58 nSTATUS
10K R92 nCONFIG
GND

XOF1
ECS-2033-500-BN
V3_3
C271 100n
4 VDD CLK 3 PGCLK
GND OE 1 V3_3
GND

PROG1A
XC2C64A-7CPG56C
JTAG
JTDI_BP J10 TDI
JTMS_B K9 TMS
JTCK_B K10 TCK
JTDO_PF A6 TDO

V1_8
PROG1B
XC2C64A-7CPG56C
100n C59
V3_3
100n C60
100n C111
100n C112
G8 VCC
H6 VCCIO1
C6 VCCIO2
D3 V_AUX
GND1 C7
GND2 F8
GND3 H4
GND

ROOM: PROG_CPLD

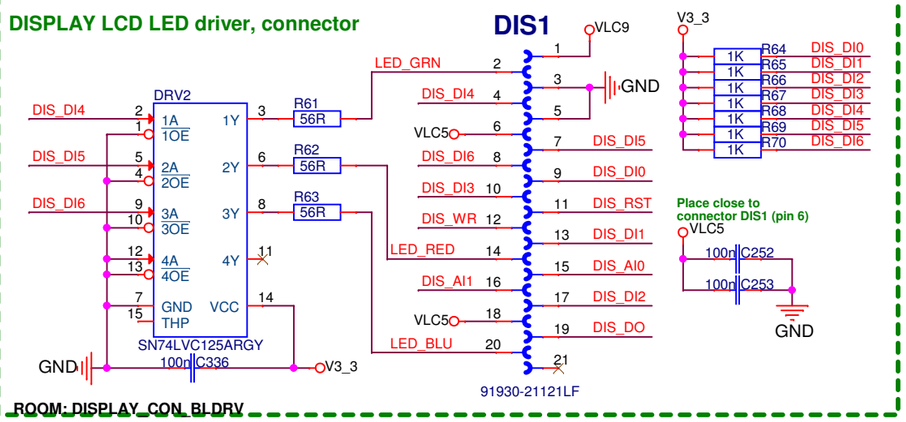
RST1 **to PROG1C (pin C3)**
V3_3
C244 100n
5 VDD out RST 1 CONFIG_SPV
in MR 3 V3_3
GND 2 GND WDI 4
TPS3823-33DBVT
GND

RST2 **to LOG1D (pin AC7)**
V3_3
C243 100n
5 VDD out RST 1 nRES nRES {7}
in MR 3 MRES1
GND 2 GND WDI 4 **from PROG1C (pin F1)**
TPS3823-33DBVT
GND

Title	FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 6 OF 17	

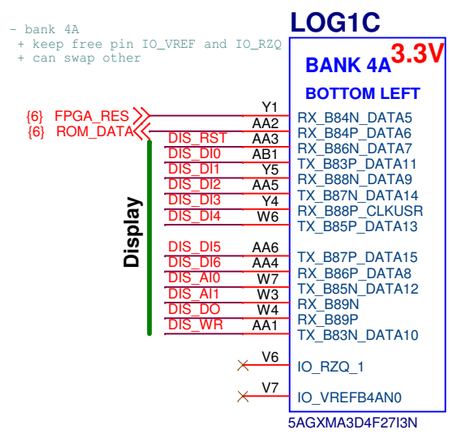
User interface - USB, Display, push buttons, HEX switch, LEDs

DISPLAY LCD LED driver, connector

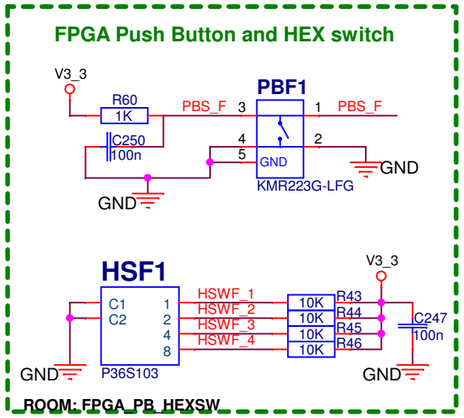


ROOM: DISPLAY_CON_BI_DRV

LOG1C

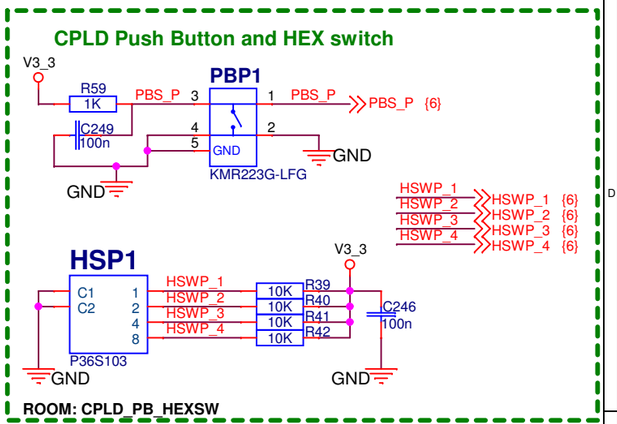


FPGA Push Button and HEX switch



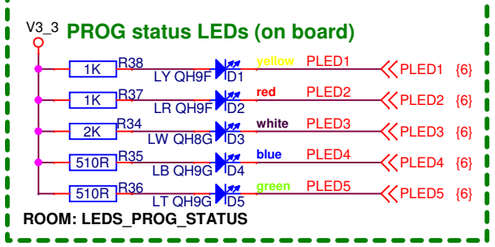
ROOM: FPGA_PB_HEXSW

CPLD Push Button and HEX switch



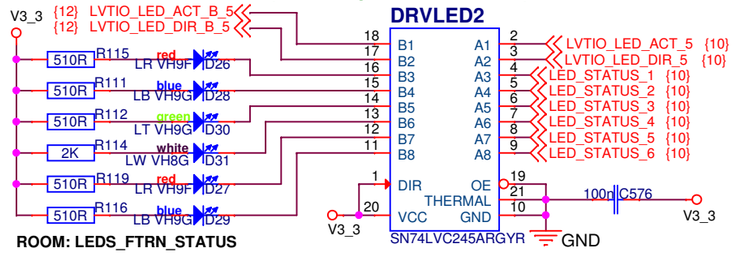
ROOM: CPLD_PB_HEXSW

PROG status LEDs (on board)



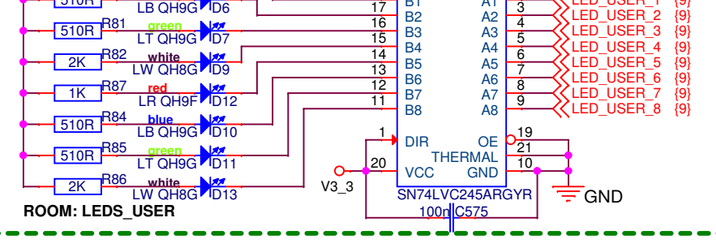
ROOM: LEDS_PROG_STATUS

WR / FTRN STATUS LEDs (on front panel from FPGA)



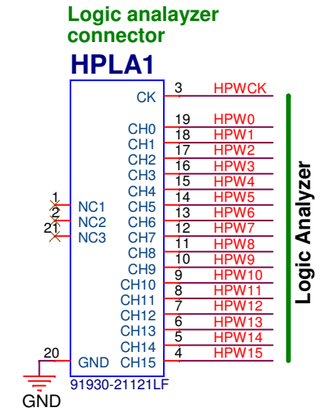
ROOM: LEDS_FTRN_STATUS

USER LEDs (on board from FPGA)

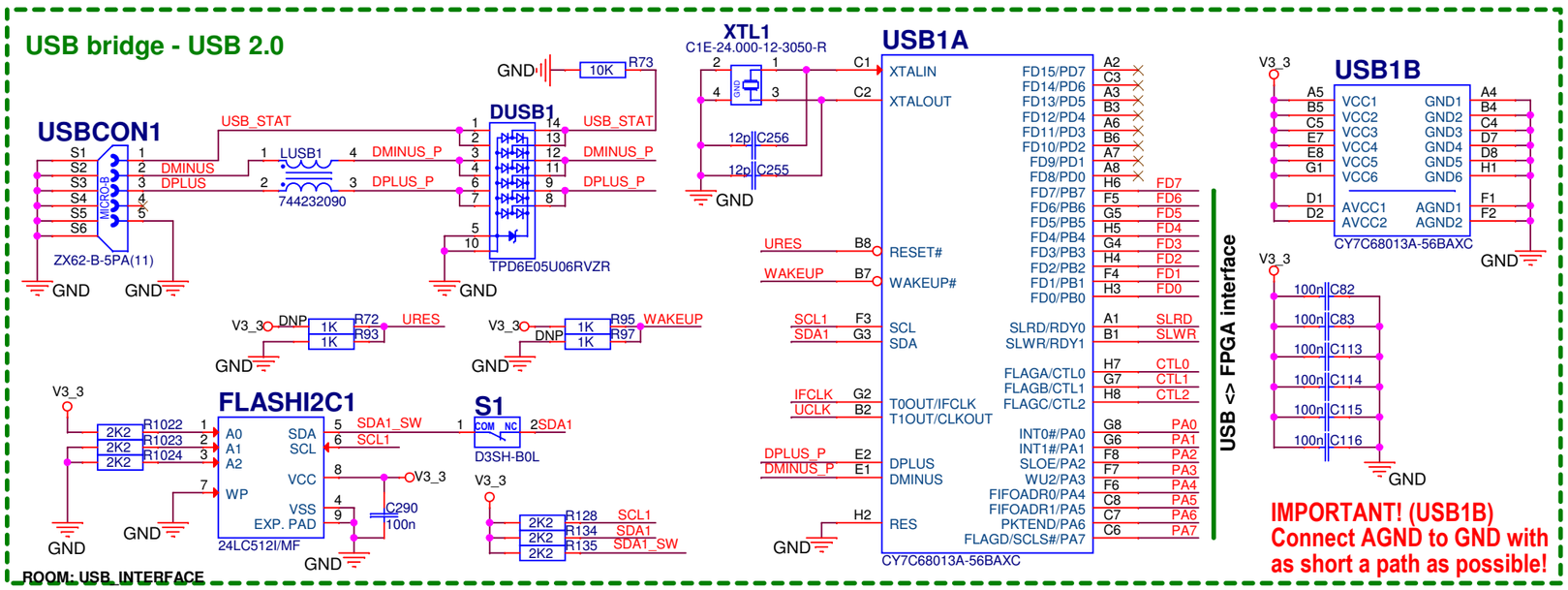


ROOM: LEDS_USER

Logic analayzer connector

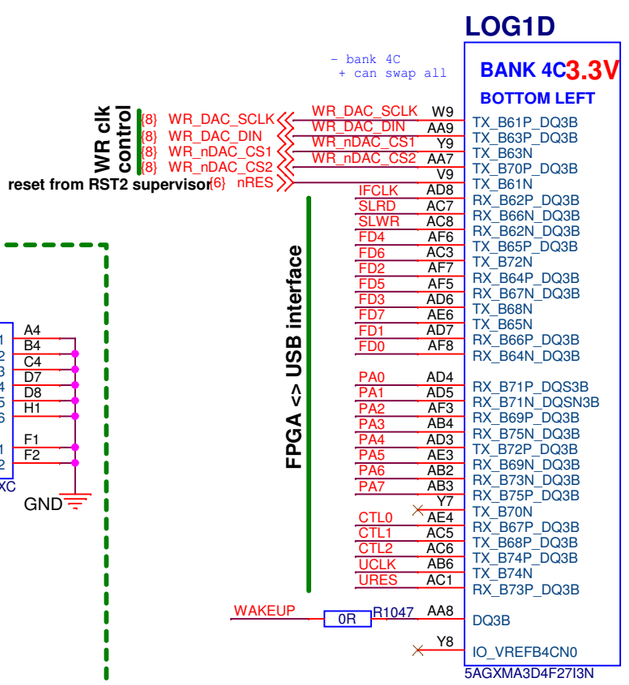


USB bridge - USB 2.0

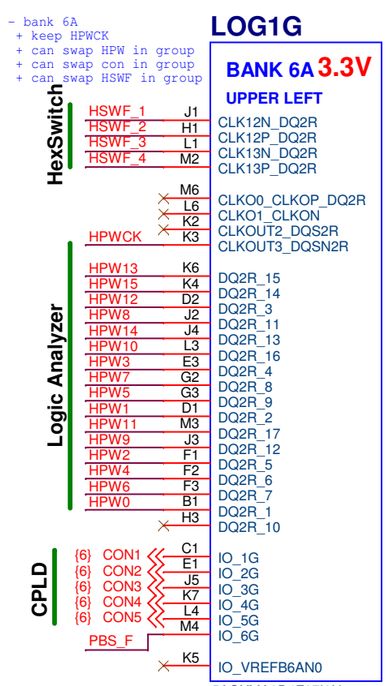


ROOM: USB_INTERFACE

LOG1D



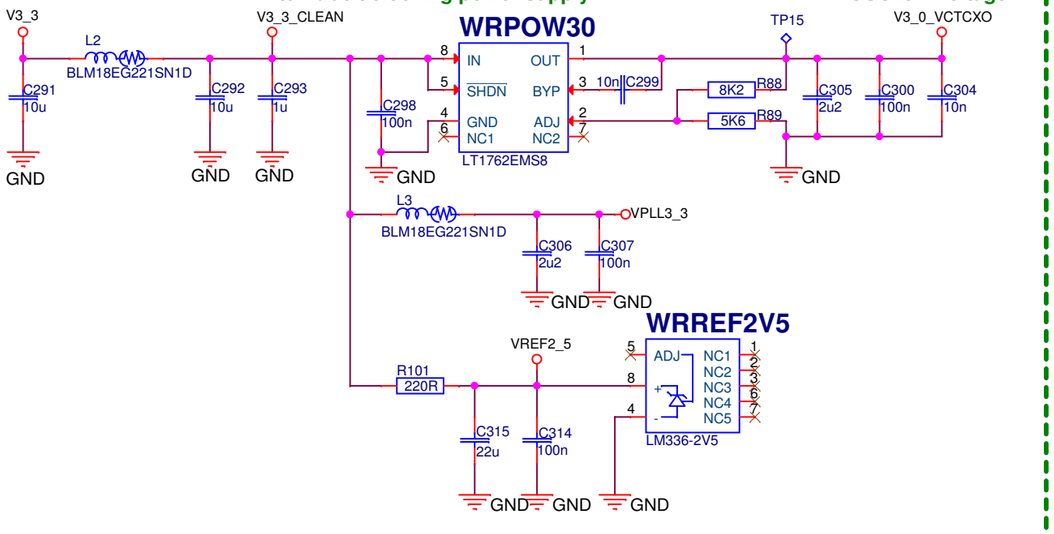
LOG1G



Title	User interface - USB, Display, push buttons, HEX switch, LEDs		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 7 OF 17	

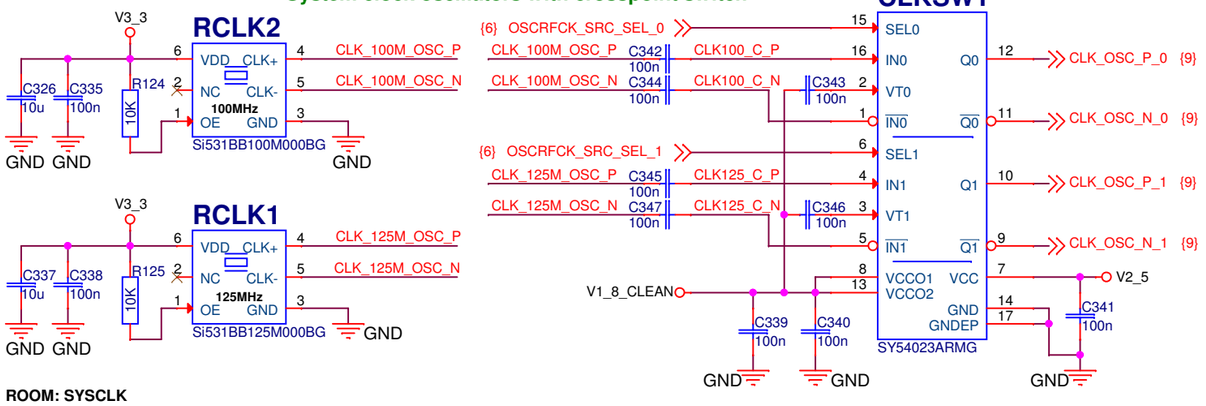
Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch

White Rabbit clocking power supply



ROOM: WRCLK_POWER

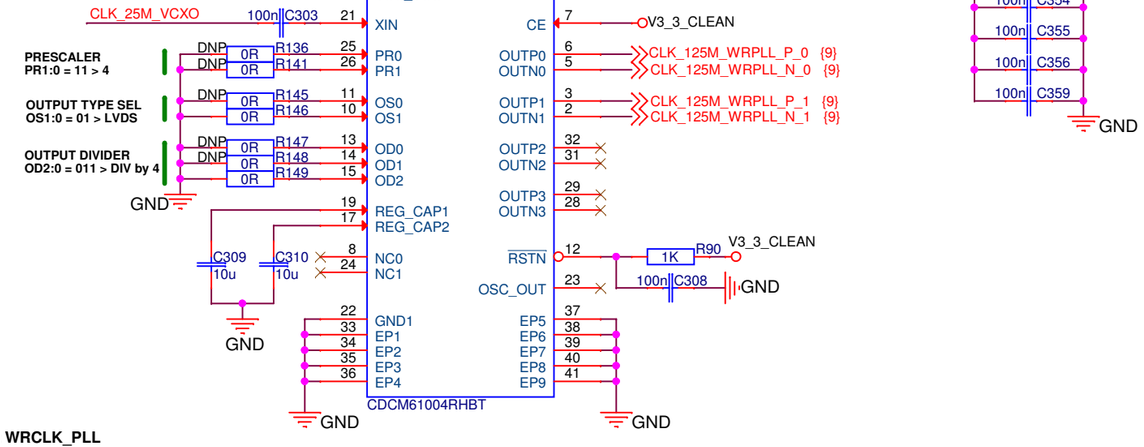
System clock oscillators with crosspoint switch



ROOM: SYSCLK

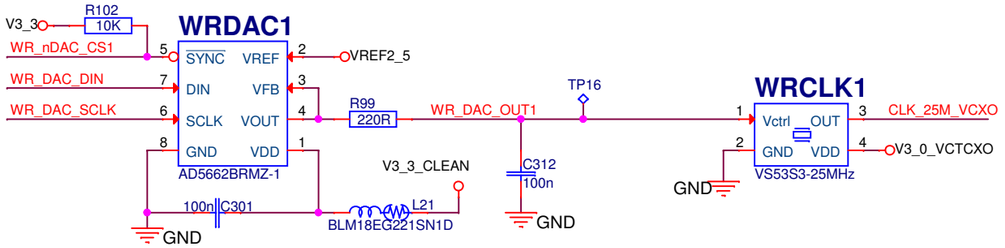
{7} WR_nDAC_CS1 — WR_nDAC_CS1
{7} WR_nDAC_CS2 — WR_nDAC_CS2
{7} WR_DAC_DIN — WR_DAC_DIN
{7} WR_DAC_SCLK — WR_DAC_SCLK

WRPLL1



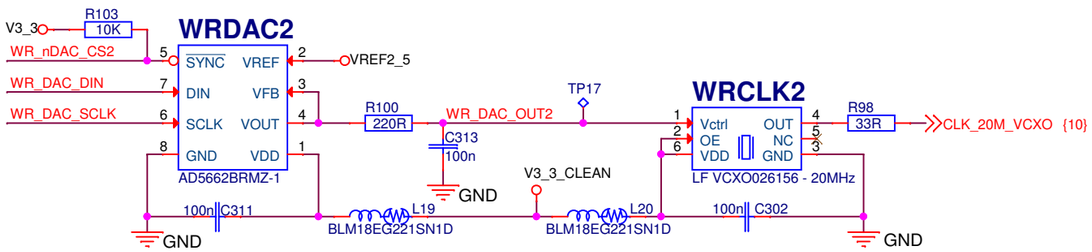
ROOM: WRCLK_PLL

WRDAC1



ROOM: WRCLK_DAC1_CLK1

WRDAC2

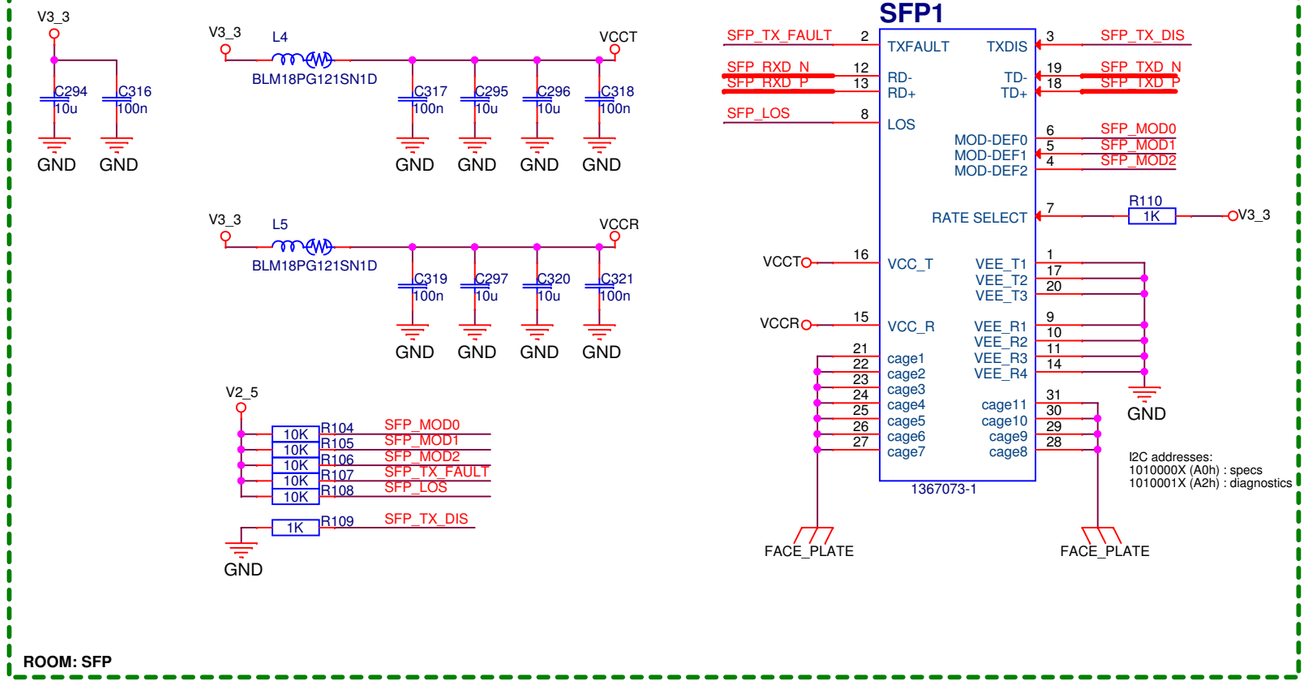


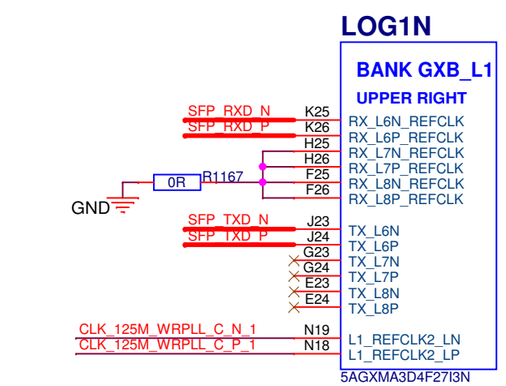
ROOM: WRCLK_DAC2_CLK2

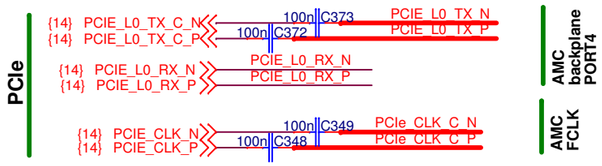
Title	Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 8 OF 17	

Fiber SFP, PCIe <> FPGA connections

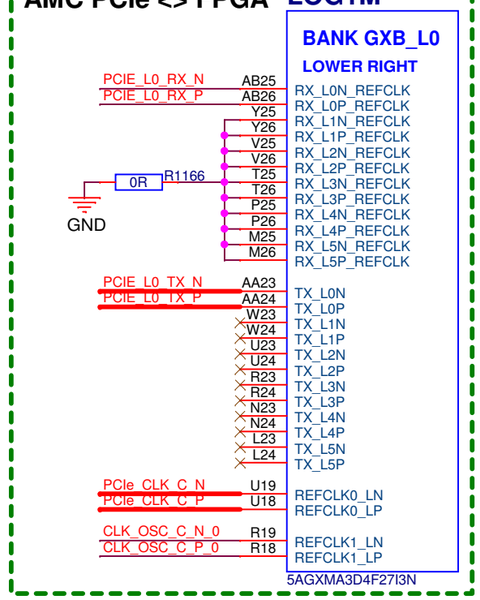
IMPORTANT!
Hi speed Gigabit lines
100R differential

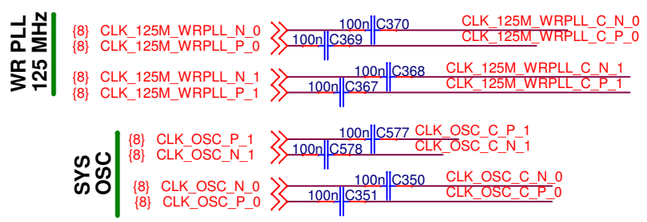


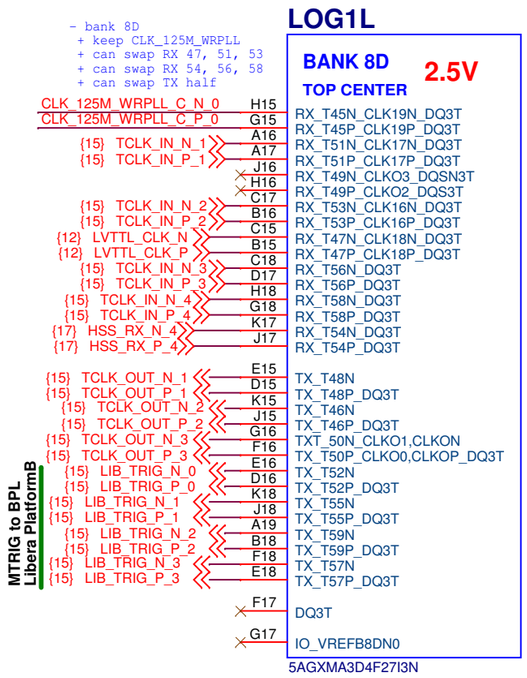


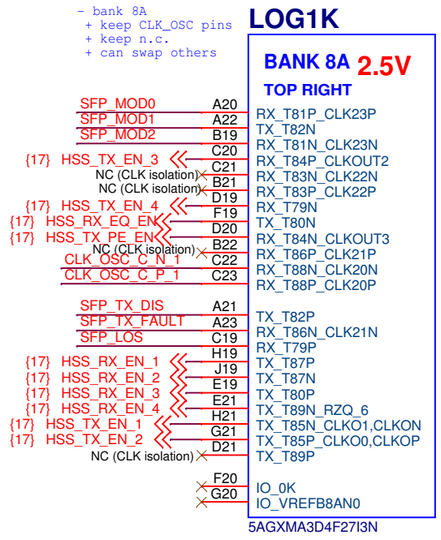


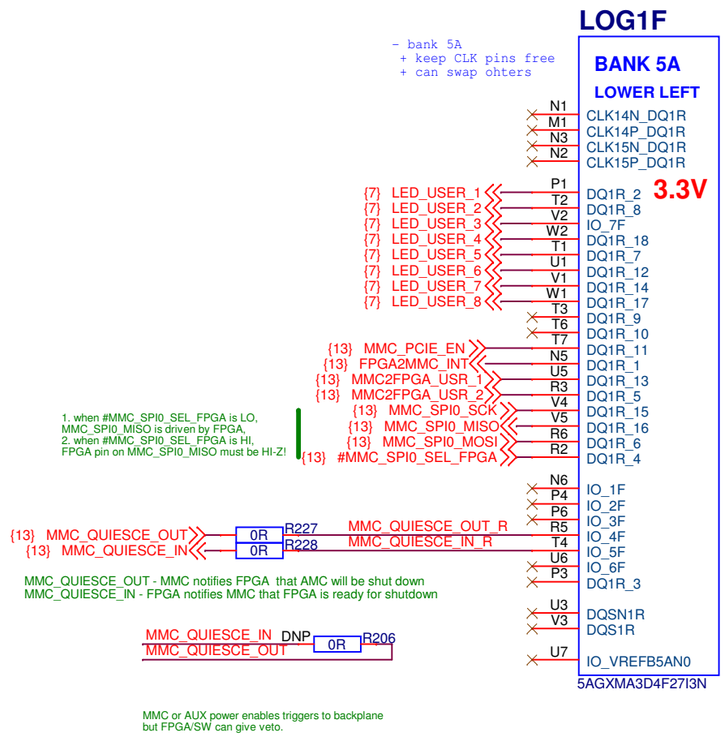
AMC PCIe <> FPGA











Title	Fiber SFP, PCIe <> FPGA connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 9 OF 17

IO block power supply, FPGA <> IO block connections

LOG1J

- bank 7D
+ can swap RX group pairs
+ can swap TX group pairs

BANK 7D — **TOP CENTER** — **2.5V**

MTCA.4 TRIG inputs from BPL

{16} MLVDIO_IN_N_1	K12	RX_T32N_DQ2T
{16} MLVDIO_IN_P_1	J11	RX_T32P_DQ2T
{16} MLVDIO_IN_N_2	A14	RX_T43N_DQ2T
{16} MLVDIO_IN_P_2	A15	RX_T43P_DQ2T
{16} MLVDIO_IN_N_3	B13	RX_T39N_DQ2T
{16} MLVDIO_IN_P_3	A13	RX_T39P_DQ2T
{16} MLVDIO_IN_N_4	E13	RX_T41N_DQ2T
{16} MLVDIO_IN_P_4	D13	RX_T41P_DQ2T
{16} MLVDIO_IN_N_5	C12	RX_T38N_DQ2T
{16} MLVDIO_IN_P_5	B12	RX_T38P_DQ2T
{16} MLVDIO_IN_N_6	A12	RX_T34N_DQSN2T
{16} MLVDIO_IN_P_6	A11	RX_T34P_DQS2T
{16} MLVDIO_IN_N_7	J12	RX_T36N_DQ2T
{16} MLVDIO_IN_P_7	H12	RX_T36P_DQ2T
{16} MLVDIO_IN_N_8	C10	RX_T30N_DQ2T
{16} MLVDIO_IN_P_8	B10	RX_T30P_DQ2T

MTCA.4 TRIG outputs from BPL

{16} MLVDIO_OUT_N_1	G14	TX_T42N
{16} MLVDIO_OUT_P_1	F14	TX_T42P_DQ2T
{16} MLVDIO_OUT_N_2	D14	TX_T40N
{16} MLVDIO_OUT_P_2	C14	TX_T40P_DQ2T
{16} MLVDIO_OUT_N_3	J14	TX_T44N
{16} MLVDIO_OUT_P_3	J13	TX_T44P_DQ2T
{16} MLVDIO_OUT_N_4	E12	TX_T37N
{16} MLVDIO_OUT_P_4	D12	TX_T37P_DQ2T
{16} MLVDIO_OUT_N_5	D11	TX_T33N
{16} MLVDIO_OUT_P_5	C11	TX_T33P_DQ2T
{16} MLVDIO_OUT_N_6	G12	TX_T35N
{16} MLVDIO_OUT_P_6	F12	TX_T35P_DQ2T
{16} MLVDIO_OUT_N_7	G11	TX_T31N
{16} MLVDIO_OUT_P_7	F11	TX_T31P_DQ2T
	G13	DQ2T
	H13	IO_VREFB7DN0

5AGXMA3D4F27I3N

LOG1I

- bank 7C
+ can swap RX group pairs
+ can swap TX group pairs

BANK 7C — **TOP LEFT** — **2.5V**

LVTTL IO data inputs LVDS, up to 200MHz

{11} LVTIO_IN_N_1	A6	RX_T19N_DQSN1T
{11} LVTIO_IN_P_1	A5	RX_T19P_DQS1T
{11} LVTIO_IN_N_2	C6	RX_T21N_DQ1T
{11} LVTIO_IN_P_2	B6	RX_T21P_DQ1T
{11} LVTIO_IN_N_3	E6	RX_T15N_DQ1T
{11} LVTIO_IN_P_3	D6	RX_T15P_DQ1T
{12} LVTIO_IN_N_4	F7	RX_T17N_DQ1T
{12} LVTIO_IN_P_4	E7	RX_T17P_DQ1T
{12} LVTIO_IN_N_5	H9	RX_T23N_DQ1T
{12} LVTIO_IN_P_5	G9	RX_T23P_DQ1T
	D8	RX_T24N_DQ1T
	C8	RX_T24P_DQ1T
	E9	RX_T26N_DQ1T
	D9	RX_T26P_DQ1T
{17} HSS_RX_N_3	H10	RX_T28N_DQ1T
{17} HSS_RX_P_3	G10	RX_T28P_DQ1T

LVTTL IO data outputs LVDS, up to 200MHz

{11} LVTIO_OUT_N_1	A9	TX_T25N
{11} LVTIO_OUT_P_1	A8	TX_T25P_DQ1T
{11} LVTIO_OUT_N_2	C7	TX_T22N
{11} LVTIO_OUT_P_2	B7	TX_T22P_DQ1T
{11} LVTIO_OUT_N_3	D5	TX_T18N
{11} LVTIO_OUT_P_3	C5	TX_T18P_DQ1T
{12} LVTIO_OUT_N_4	G8	TX_T20N
{12} LVTIO_OUT_P_4	F8	TX_T20P_DQ1T
{12} LVTIO_OUT_N_5	J8	TX_T16N
{12} LVTIO_OUT_P_5	J9	TX_T16P_DQ1T
{16} MLVDIO_OUT_N_8	C9	TX_T29N
{16} MLVDIO_OUT_P_8	B9	TX_T29P_DQ1T
{15} TCLK_OUT_N_4	K10	TX_T27N
{15} TCLK_OUT_P_4	J10	TX_T27P_DQ1T
	E10	DQ1T
	F10	IO_VREFB7CN0

5AGXMA3D4F27I3N

LOG1H

- bank 7A
+ keep CRC_ERROR
+ kepp PCIE_RST
+ can swap others

BANK 7A — **TOP LEFT** — **3.3V**

	G4	RX_T1N
	F4	RX_T1P
	E4	TX_T5N_PR_REQUEST
	D4	TX_T5P_PR_DONE
{6} CRC_ERROR	A3	RX_T4N_CRC_ERROR
	C4	RX_T6P_INIT_DONE
{12} #LVTTL_IN_CLK_EN	C3	RX_T2P_DEV_OE
	A2	RX_T4P_CVP_CONFDONE
{11} #LVTIO_OE_1	A4	TX_T7P_PR_ERROR
{11} #LVTIO_OE_2	B3	RX_T6N_NCEO
{11} #LVTIO_OE_3	B4	TX_T7N_PR_READY
{12} #LVTIO_OE_4	C2	RX_T2N_DEV_CLRN
{12} #LVTIO_OE_5		
	J6	IO_0H
{13} #MMC_PCIE_RST — R229 1K — #MMC_PCIE_RST_R	G6	IO_RZQ_5
	J7	IO_VREFB7AN0
	F6	NPERSTL0

5AGXMA3D4F27I3N

LOG1B

- bank 3D
+ keep HHS_TX_x on TX half, or move to bank 3A
+ can swap ohters

BANK 3D — **BOTTOM RIGHT** — **2.5V**

LVTTL IO control signals

{11} LVTIO_TERM_EN_1	AD18	RX_B32N_DQ1B
{11} LVTIO_LED_ACT_1	AE18	RX_B32P_DQ1B
{11} LVTIO_LED_DIR_1	AC16	RX_B36P_DQ1B
{11} LVTIO_TERM_EN_2	Y18	RX_B34P_DQ1B
{11} LVTIO_LED_ACT_2	AF13	RX_B45P_CLK7P_DQ1B
{11} LVTIO_LED_DIR_2	AB16	RX_B36N_DQ1B
{11} LVTIO_TERM_EN_3	V16	RX_B37N_CLK4N_DQ1B
{11} LVTIO_LED_ACT_3	W16	RX_B37P_CLK4P_DQ1B
{11} LVTIO_LED_DIR_3	AF15	RX_B39N_CLK5N_DQ1B
{12} LVTIO_TERM_EN_4	AF16	RX_B39P_CLK5P_DQ1B
{11} LVTIO_LED_ACT_4	AF14	RX_B45N_CLK7N_DQ1B
{11} LVTIO_LED_DIR_4	AD14	RX_B43P_CLK6P_DQ1B
{12} LVTIO_TERM_EN_5	AC14	RX_B43N_CLK6N_DQ1B
{7} LVTIO_LED_ACT_5	W15	RX_B41P_CLKO2_DQS1B
{7} LVTIO_LED_DIR_5	V15	RX_B41N_CLKO3_DQSN1B
	W18	RX_B34N_DQ1B
{7} LED_STATUS_1	AA18	TX_B31N
{7} LED_STATUS_2	AB18	TX_B31P_DQ1B
{7} LED_STATUS_3	Y17	TX_B33N
{7} LED_STATUS_4	AA17	TX_B33P_DQ1B
{7} LED_STATUS_5	AC17	TX_B35N
{7} LED_STATUS_6	AD17	TX_B35P_DQ1B
{17} HSS_TX_N_1	AD15	TX_B42N
{17} HSS_TX_P_1	AE15	TX_B42P_DQ1B
{17} HSS_TX_N_2	AD16	TX_B38N
{17} HSS_TX_P_2	AE16	TX_B38P_DQ1B
{17} HSS_TX_N_3	AA15	TX_B40N_CLKO1,CLKON
{17} HSS_TX_P_3	AB15	TX_B40P_CLKO0,CLKOP_DQ1B
{17} HSS_TX_N_4	Y14	TX_B44N
{17} HSS_TX_P_4	AA14	TX_B44P_DQ1B
	AA16	DQ1B
	Y16	IO_VREFB3DN0

5AGXMA3D4F27I3N

LOG1A

- bank 3A
+ keep CLK_20M_VCXO
+ can move hss_rx_1, hss_rx_2 to bank 3A

BANK 3A — **BOTTOM RIGHT** — **2.5V**

{17} HSS_RX_N_2	AB21	RX_B2N_CLK0N
{17} HSS_RX_P_2	AC21	RX_B2P_CLK0P
{17} HSS_RX_N_1	AC22	RX_B4N_CLK1N
{17} HSS_RX_P_1	AD22	RX_B4P_CLK1P
NC (CLK isolation)	AF22	RX_B6N_CLKOUT3
	AF23	RX_B6P_CLKOUT2
NC (CLK isolation)	AE21	RX_B7N_CLK2N
{8} CLK_20M_VCXO	AF21	RX_B7P_CLK2P
	AF19	RX_B9N_CLK3N
NC (CLK isolation)	AF20	RX_B9P_CLK3P
	AE19	RX_B11N
	AF18	RX_B11P
	AA20	TX_B1N_RZQ_0
	AB19	TX_B1P
	Y21	TX_B3N
	AA21	TX_B3P
	AD23	TX_B5N_CLKO1,CLKON
	AE23	TX_B5P_CLKO0,CLKOP
	AC20	TX_B8N
	AD20	TX_B8P
	AC19	TX_B10N
	AD19	TX_B10P
	Y19	IO_0A
	Y20	IO_VREFB3AN0

5AGXMA3D4F27I3N

Power supply for output drivers

RUN driven by MMC or AUX V12 presence

V12_0CAR — 10K R133 — D17 LR QH9F red — GND

PRUN_3V3_IO {13} — PGOOD_3V3_IO {13}

PRUN_3V3_IO — DSH12 — CMDSH2-3 — PGOOD_3V3_IO

POWIO33A — LTM8023EV

PRUN_3V3_IO	H5	RUN/SS	AUX F5
			BIAS G5
PGOOD_3V3_IO	H6	PGOOD	SYNC G6 — 10K R132
			ADJ H7 — 154K R131
	F7	SHARE	R_T G7 — 49K9 R129

GND

POWIO33B — LTM8023EV

	G1	V_IN1	V_OUT1 A1
	G2	V_IN2	V_OUT2 A2
	G3	V_IN3	V_OUT3 A3
	H1	V_IN4	V_OUT4 A4
	H2	V_IN5	V_OUT5 B1
	H3	V_IN6	V_OUT6 B2
			V_OUT7 B3
			V_OUT8 B4
			V_OUT9 C1
			V_OUT10 C2
			V_OUT11 C3
			V_OUT12 C4

V12_0CAR — C331 100n — C330 10u — GND GND

TP18 — SJMP8 (1) — C332 22u — GND

V33_ODRV — C333 100u — C334 100u — GND GND

POWIO33C — LTM8023EV

	A5	GND1	GND24 F6
	A6	GND2	GND23 E7
	A7	GND3	GND22 E6
	B5	GND4	GND21 E5
	B6	GND5	GND20 E4
	B7	GND6	GND19 E3
	C5	GND7	GND18 E2
	C6	GND8	GND17 E1
	C7	GND9	GND16 D7
	D1	GND10	GND15 D6
	D2	GND11	GND14 D5
	D3	GND12	GND13 D4

GND GND

ROOM: IO_POWER

LOG1E

- bank 4D
+ keep fee DQ2B, IO_VREF
+ can swap other

BANK 4D — **BOTTOM CENTER** — **3.3V**

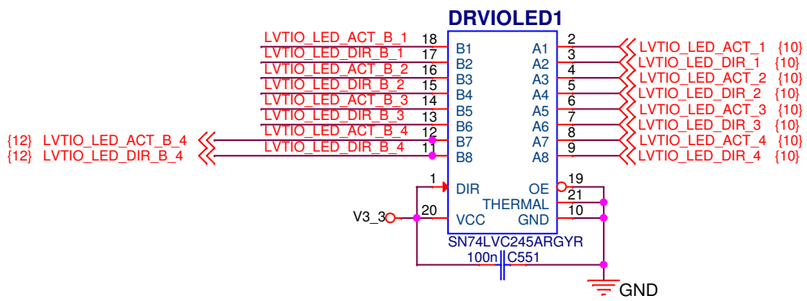
{16} MLVDIO_DE_1	AE12	RX_B51P_DQ2B
{16} #MLVDIO_RE_1	AB13	RX_B47N_DQ2B
{16} MLVDIO_DE_2	AD13	RX_B49N_DQ2B
{16} #MLVDIO_RE_2	AD12	RX_B51N_DQ2B
{16} MLVDIO_DE_3	AC13	RX_B47P_DQ2B
{16} #MLVDIO_RE_3	Y13	TX_B48N
{16} MLVDIO_DE_4	AA13	TX_B48P_DQ2B
{16} #MLVDIO_RE_4	V12	TX_B50N
{16} MLVDIO_DE_5	AE13	RX_B49P_DQ2B
{16} #MLVDIO_RE_5	Y11	TX_B55N
{16} MLVDIO_DE_6	AF12	RX_B52N_DQ2B
{16} #MLVDIO_RE_6	V13	TX_B46N
{16} MLVDIO_DE_7	AC10	RX_B54N_DQ2B
{16} #MLVDIO_RE_7	W10	RX_B58P_DQ2B
{16} MLVDIO_DE_8	AA10	TX_B59P_DQ2B
{16} #MLVDIO_RE_8	Y10	TX_B59N
{16} MLVDIO_FSEN	W12	TX_B50P_DQ2B
{16} #MLVDIO_PDN	V10	RX_B58N_DQ2B
{15} #TCLK_EN_1	AC9	RX_B60P_DQ2B
{15} TCLK_DIR_1	AF9	RX_B56P_DQS2B
{15} #TCLK_EN_2	AE9	TX_B57P_DQ2B
{15} TCLK_DIR_2	AD9	TX_B57N
{15} #TCLK_EN_3	AC11	TX_B53N
{15} TCLK_DIR_3	AD11	TX_B53P_DQ2B
{15} #TCLK_EN_4	W13	TX_B46P_DQ2B
{15} TCLK_DIR_4	AA11	TX_B55P_DQ2B
	AE10	RX_B56N_DQSN2B
{15} LIB_TRIG_OE	AB9	RX_B60N_DQ2B
	AD10	RX_B54P_DQ2B
	AF11	RX_B52P_DQ2B
	AB12	DQ2B
	AA12	IO_VREFB4DN0

5AGXMA3D4F27I3N

(1) - 0R solder connection, to test regulator outputs before connecting to load

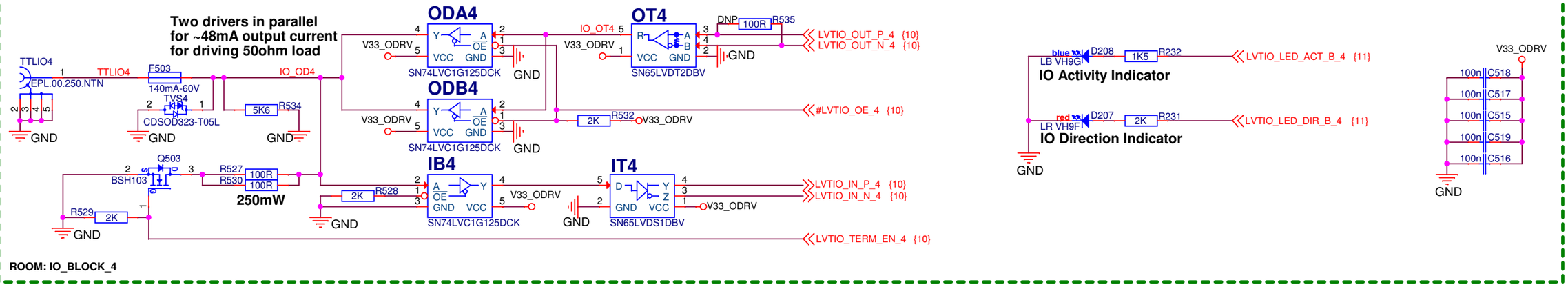
Title	IO block power supply, FPGA <> IO block connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 10 OF 17	

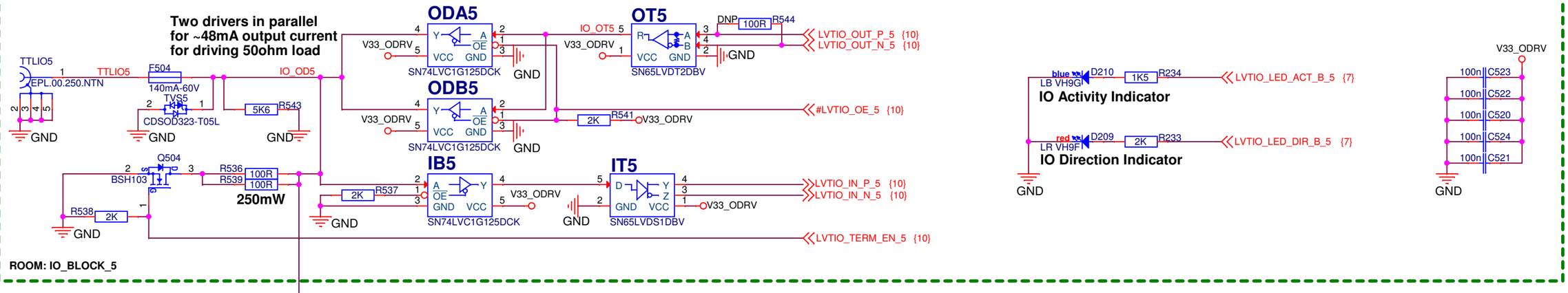
LVTTL IO blocks 1-3

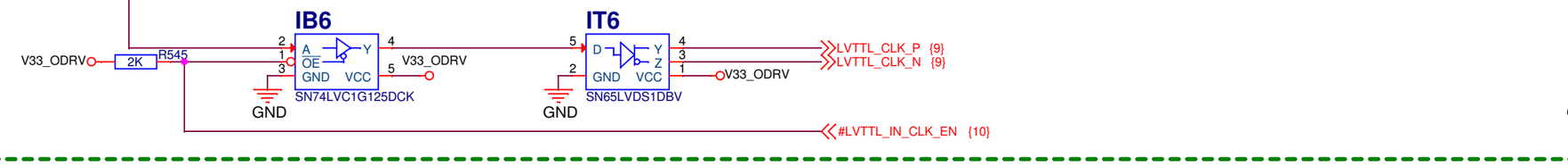


Title	LVTTL IO blocks 1-3		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 11 OF 17	

LVTTL IO blocks 4-5, IO CLOCK input







Title	LVTTL IO blocks 4-5, IO CLOCK input		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 12 OF 17	

MMC, IPMI

MMC user push button

PBM1 — KMR223G-LFG
V33_MP — 10K R175 — #MMC_PB_1
GND — C490 100n — GND

PBM2 — KMR223G-LFG
V33_MP — 10K R176 — #MMC_PB2_JCON
GND — C491 100n — GND

#MMC_PB_2 used as MMC reset

MMC user LEDs

V33_MP — 1K R96 — LR QH9F red DU1 — #MMC_ULED_0
510R R94 — LT QH9G green DU2 — #MMC_ULED_1

ROOM: MMC_PBS_LEDS

USB <> UART for MMC console (on the front panel if possible)

USBCON2 — MICRO-B — ZX62-B-5PA(11)
MMC_USB_K_DM, MMC_USB_K_DP
LUSB2 — 744232090
MMC_USB_L_DM, MMC_USB_L_DP
MMC_USB_VBUS

DUSB2 — TPD6E05U06RVZR
MMC_USB_VBUS — 10K R163 — 4K7 R162 — VBUS_SENSE
MMC_USB_L_DM — 33R R164 — MMC_USB_R_DM
MMC_USB_L_DP — 33R R165 — MMC_USB_R_DP
22p C381, 22p C383, 22p C382, 22p C387

IC1 — FT230XQ
MMC_USB_R_DM, MMC_USB_R_DP
USBDM, USBDP, CBUS3, CBUS2, CBUS1, CBUS0, GND1, GND2, EP, TXD, RXD, RTS#, CTS#, RESET#, VCCIO, 3V3OUT, VCC
MMC_UART_RX, MMC_UART_TX
VBUS_SENSE, #RX_LED, #TX_LED
V33_MP — 2.2u C378, 2.2u C379, 100n C374, 100n C375, 100n C380

V33_MP — 510R R350 — LT QH9G green D23 — #RX_LED
2K R351 — LW QH8G white D24 — #TX_LED

ROOM: MMC_USB

Resistor dividers for voltage sensors

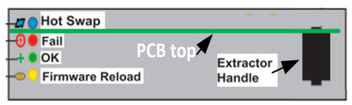
V12_0CAR — 4K7 R207 — 510R R208 — 1K R212 — MMC_VS_V12CAR
V33_MP — 510R R209 — 100R R210 — 1K R216 — MMC_VS_V3_3_MP
V3_3 — 220R R211 — 1K R217 — MMC_VS_V3_3
V2_5 — 33R R213 — 1K R218 — MMC_VS_V2_5
V1_15 — 33R R214 — 1K R219 — MMC_VS_V1_15
V1_15C — 33R R215 — 1K R220 — MMC_VS_V1_15C
GND

ROOM: MMC_VOLT_RED_DIV

MTCA Extractor handle switch

SW1 — HDT0001 (N.O.)
10K R153 — V33_MP
R1031 1K — #MMC_HANDLE_SW
C412 100n — GND

ROOM: MMC_HANDLE



IPMI/AMC status LEDs on the front panel

QH - top (green, white), VH - side (blue, red)

V33_MP
510R R300 — LB VH9G D32 blue — #MMC_LED_HOTSWAP
1K R301 — LR VH9F D33 red — #MMC_LED_FAIL
510R R302 — LT QH9G D20 green — #MMC_LED_OK
1K R303 — LW VH8G D22 white — #MMC_LED_FWRELOAD

ROOM: MMC_IPMI_LEDS

PMX1

V33_MP_BPL, V3_3 — IN1, IN2, VSNS, EN, STAT, OUT, ILIM, GND — TPS2112APW
0R R1165 — V33_MP
510R R1095
GND

MP power MUX:
- in crate: V33_MP_BPL > 0.8V
  out = V33_MP_BPL
- not in crate, on AUX:
  V33_MP_BPL (0V) < 0.8V
  out = V3_3

MMC FW FLASH

MMEM1 — M25P80-VMN6P
HOLD#, DOUT, DIN, CLK, CS#, W#, VSS, VCC
MMC_SPI0_MISO, MMC_SPI0_MOSI, MMC_SPI0_SCK, #MMC_SPI0_SEL_FLASH
V33_MP — 100n C403
GND

MMC1A

TX and RX signal naming is refering to the MMC side

CLI and Debug UART: MMC_UART_TX, MMC_UART_RX
{14} IPMB_L_SCL, {14} IPMB_L_SDA
{9} MMC_SPI0_SCK, {9} MMC_SPI0_MISO, {9} MMC_SPI0_MOSI, #MMC_SPI0_SEL_FLASH
{9} #MMC_SPI0_SEL_FPGA, {6,14} JTAGSW_SEL, {9} MMC_PCIE_EN, {9} MMC_I2C_SCL, MMC_DCDC_EN, MMC_PGOOD, MMC_I2C_SDA, {9} MMC_I2C_SDA, #MMC_HANDLE_SW

P0.0/TXD0/PWM1, P0.1/RXD0/PWM3/EINT0, P0.2/SCL0/CAP0.0, P0.3/SDA0/MAT0.0/EINT1, P0.4/SCK0/CAP0.1/AD0.6, P0.5/MISO0/MAT0.1/AD0.7, P0.6/MOSI0/CAP0.2/AD1.0, P0.7/SSEL0/PWM2/EINT2
P0.8/TXD1/PWM4/AD1.1, P0.9/RXD1/PWM6/EINT3, P0.10/RTS1/CAP1.0/AD1.2, P0.11/CTS1/CAP1.1/SCL1, P0.12/DSR1/MAT1.0/AD1.3, P0.13/DTR1/MAT1.1/AD1.4, P0.14/DCD1/EINT1/SDA1, P0.15/RI1/EINT2/AD1.5
P0.16/EINT0/MAT0.2/CAP0.2, P0.17/CAP1.2/SCK1/MAT1.2, P0.18/CAP1.3/MISO1/MAT1.3, P0.19/MAT1.2/MOSI1/CAP1.2, P0.20/MAT1.3/SSEL1/EINT3, P0.21/PWM5/AD1.6/CAP1.3, P0.22/AD1.7/CAP0.0/MAT0.0, P0.23
P0.25/AD0.4/AOUT, P0.26/AD0.5, P0.27/AD0.0/CAP0.1/MAT0.1, P0.28/AD0.1/CAP0.2/MAT0.2, P0.29/AD0.2/CAP0.3/MAT0.3, P0.30/AD0.3/EINT3/CAP0.0, P0.31

#MMC_PB_1
FPGA2MMC_INT {9}, #MMC_FPGA_CONFIG {6}, MMC_QUIESCE_OUT {9}, MMC_QUIESCE_IN {9}
MMC2FPGA_USR_1 {9}, MMC2FPGA_USR_2 {9}, #MMC_PCIE_RST {10}
MMC_VS_V1_15, MMC_VS_V1_15C, MMC_VS_V3_3, MMC_VS_V2_5, MMC_VS_V12CAR, MMC_VS_V3_3_MP, #MMC_LED_HOTSWAP
power voltage sensing - analog inputs

LPC2138FBD64/01

MMC1B

V33_MP — 30K1 R186 IPMB_L_SDA — TP19
30K1 R187 IPMB_L_SCL — TP20, TP24
Test pads for I2C bus sniffing
GND

#MMC_LED_FAIL, #MMC_LED_OK, #MMC_LED_FWRELOAD, #MMC_ULED_0, #MMC_ULED_1
{14} IPMI_GA_0, {14} IPMI_GA_1, {14} IPMI_GA_2 — 3K3 R196 IPMI_GA_0, 3K3 R197 IPMI_GA_1, 3K3 R198 IPMI_GA_2
AMC geographical address from backplane
{6} CONF_DONE, {4,13,14} PRESENT_V12AUX, MMC_GA_COMMON

P1.16/TRACEPKT0, P1.17/TRACEPKT1, P1.18/TRACEPKT2, P1.19/TRACEPKT3, P1.20/TRACESYNC, P1.21/PIPESTAT0, P1.22/PIPESTAT1, P1.23/PIPESTAT2, P1.24/TRACECLK, P1.25/EXTIN0, P1.26/RTCK
P1.27/TDO, P1.28/TDI, P1.29/TCK, P1.30/TMS, P1.31/TRST
JTDO_MMC, JTDI_MMC, JTCK_MMC, JTMS_MMC
0R R1169 — #JTRST_MMC
10K R168 — V33_MP

JTRST# only from backplane, JTAG connector does not provide JTRST#

LPC2138FBD64/01

MMC1C

XTL2 — C1E-24.000-12-3050-R
#MMC_RESET, 12p C401, 12p C402
RESET, XTAL1, XTAL2, RTCX1, RTCX2, VBAT, VREF, VDDA, VDD1, VDD2, VDD3, VSSA, VSS1, VSS2, VSS3, VSS4, VSS5
V33_ADC, AGND, V33_MMC, VREF2_5_MMC

LPC2138FBD64/01

MVREF1

V33_MP — R188 220R — VREF2_5_MMC
C410 22u, C327 100n
ADJ, NC1, NC2, NC3, NC4, NC5 — LM336-2V5
GND

JTAG1 connector

MMC JTAG
VCC, GND1, GND2, GND3, RTCK/NU, TMS/SWDIO, TCLK/SWCLK, TDO/SWO, TDI/NU, #RESET — M50-3600542
V33_MP — 100R R1032 JTMS_MMC, 100R R1033 JTCK_MMC, 100R R1034 JTDO_MMC, 100R R1035 JTDI_MMC, #MMC_PB2_JCON
#JTRST_MMC, JTMS_MMC, JTCK_MMC, JTDO_MMC, JTDI_MMC

DTV2 — TPD6E05U06RVZR
V33_MP — 10K R157, 10K R161, 10K R158, 10K R159, 10K R160
C366 100n
GND

Force #IPMI_MMC_ENABLE low when FTRN powered from AUX power (not in the crate). Use Push-button for MMC reset.

V33_MP — R183 10K — {13,14} #IPMI_MMC_ENABLE — Q10 BSH103
{4,13,14} PRESENT_V12AUX
GND

{13,14} #IPMI_MMC_ENABLE — #IPMI_MMC_ENABLE_R — 0R R199, DNP 10K R200
GND
Option to not use #IPMI_MMC_ENABLE for MMC reset

2-Input AND Gate With One Inverted Input (IN2):
If (NOT #IPMI_MMC_EN) = H and #MMC_PB_2 = H
#MMC_RESET_CMB = H
else
#MMC_RESET_CMB = L (active)

IC2 — SN74LVC1G97DCK
#MMC_PB2_JCON, #IPMI_MMC_ENABLE_R — IN0, IN1, IN2, GND, VCC, Y
V33_MP — C384 100n
GND

MRST1

V33_MP — C385 100n — GND
VDD, out RST, in MR, GND, WDI — TPS3823-33DBVT
#MMC_RESET, #MMC_RESET_CMB

ROOM: MMC_RST_EN

MMC local I2C bus: - temp sensors, FRU EEPROM

V33_MP
10K R154 MMC_I2C_SDA — TP21
10K R155 MMC_I2C_SCL — TP22 — TP25
10K R156 #OVERTEMP — TP23
GND

TS1 — LM73CIMK-0
100n C400
VDD, SDA, SCL, ALERT, GND, ADDR
MMC_I2C_SDA, MMC_I2C_SCL, #OVERTEMP
10K R166 — 1001:001

TS2 — LM73CIMK-0
100n C404
VDD, SDA, SCL, ALERT, GND, ADDR
MMC_I2C_SDA, MMC_I2C_SCL, #OVERTEMP
10K R167 — 1001:010

FRU, SDR, CONFIG EEPROM — MMEM2 — 24LC512I/MF
MMC_I2C_SDA, MMC_I2C_SCL
SDA, SCL, A0, A1, A2, VCC, WP, VSS, EXP. PAD
1010:000
10K R172, 10K R173, 10K R174
100n C371

ROOM: MMC_TEMP_FRUMEM

TURN ON for main power regulators, 2 use cases:
- when in crate, by MMC_DCDC_EN
- when on AUX power, DCDC converters are turned on by default, MMC is overriden

MMC_DCDC_EN — DSH7 CMDSH2-3
{4,13,14} PRESENT_V12AUX — DSH8 CMDSH2-3
GND — 1K R185

0R R201 PRUN_3V3 — PRUN_3V3 {4}
0R R202 PRUN_1V15 — PRUN_1V15 {4}
0R R203 PRUN_1V15C — PRUN_1V15C {4}
0R R204 PRUN_2V5 — PRUN_2V5 {4}
0R R205 PRUN_3V3_IO — PRUN_3V3_IO {10}

enable outputs of payload power converters

V33_MP — R184 10K — MMC_PGOOD
DSH3 CMDSH2-3 — PGOOD_1V15_3V3 {4}
DSH4 CMDSH2-3 — PGOOD_1V15C {4}
DSH5 CMDSH2-3 — PGOOD_2V5 {4}
DSH6 CMDSH2-3 — PGOOD_3V3_IO {10}

monitor status of payload power converters

PGOOD signals from each power converter are joined but still isolated (wired AND function).
This way each PGOOD can still have its own LED indicator.

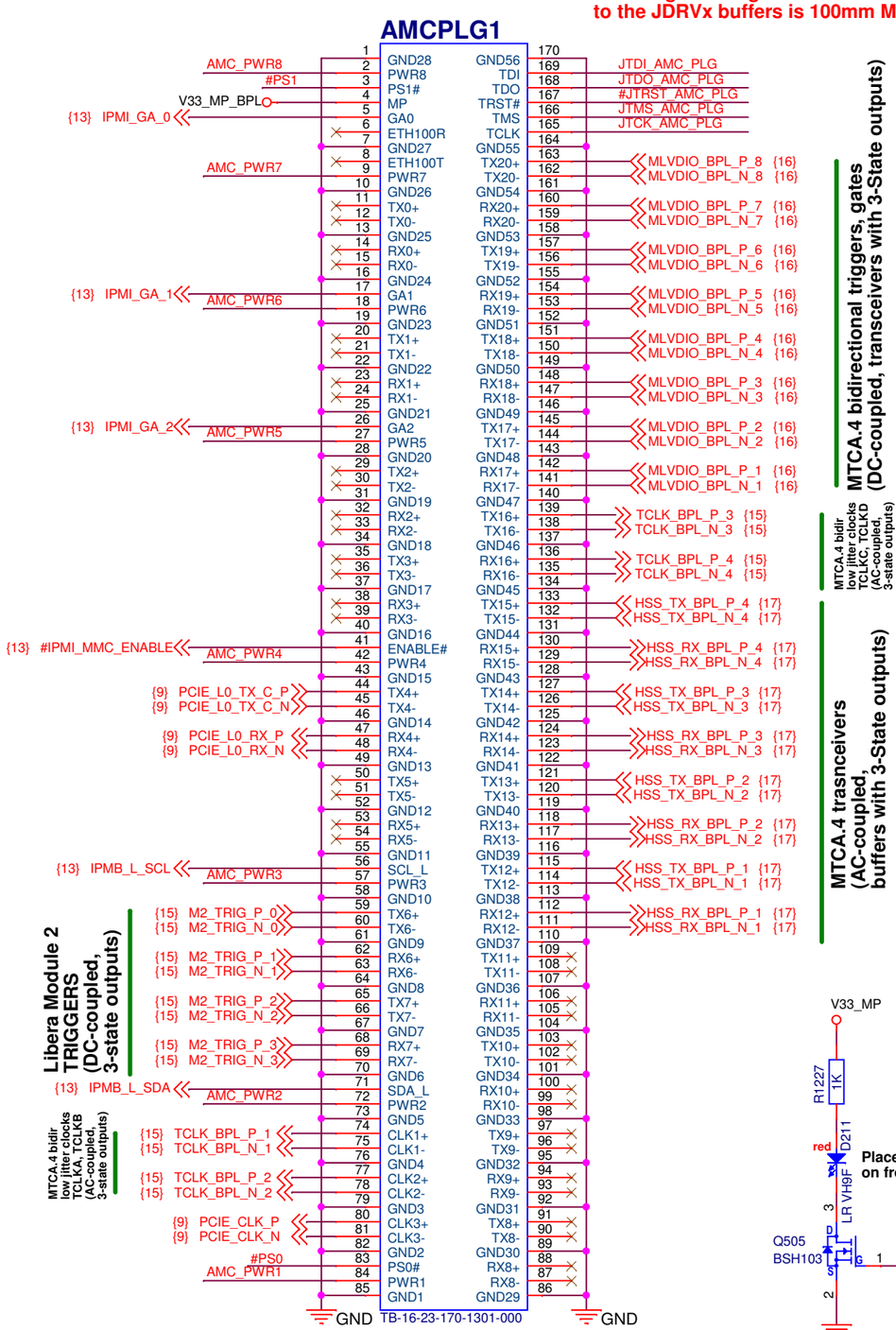
V33_MMC — L17 BLM18PG221SN1D — V33_MP
22u C395, 22u C396, 100n C392, 100n C393, 100n C394
GND

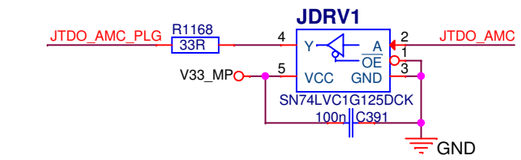
V33_ADC — L18 BLM18PG221SN1D — V33_MP
100n C397, 100n C399, 10n C398
L16 BLM18PG221SN1D — AGND
GND

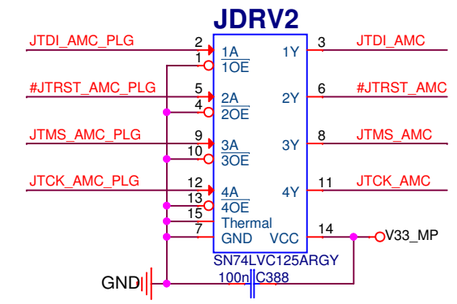
Title	MMC, IPMI		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 13 OF 17

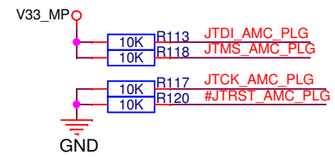
AMC backplane plug

JTAG signals length from the AMCPLG1 connector to the JDRVx buffers is 100mm MAX!!!

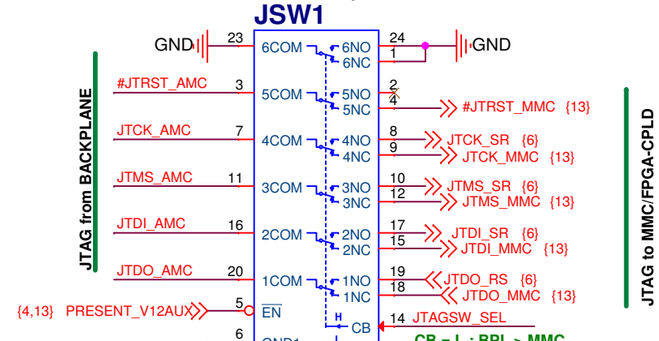


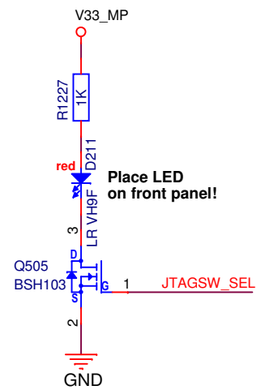


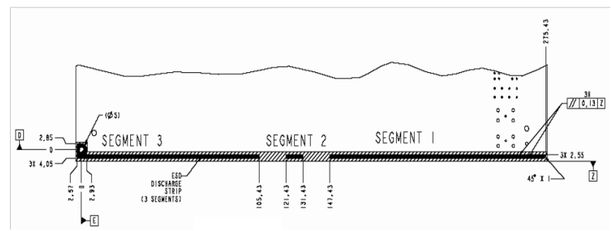


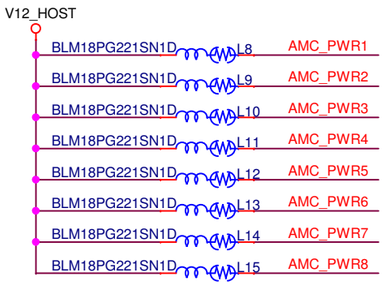


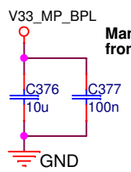
JTAG swithc for routing Backplane JTAG to MMC or CPLD/FPGA. Monitored by MMC.





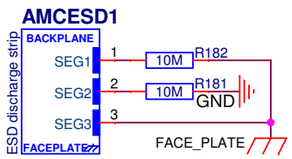


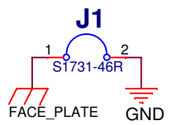




Management Power from MTCA backplane

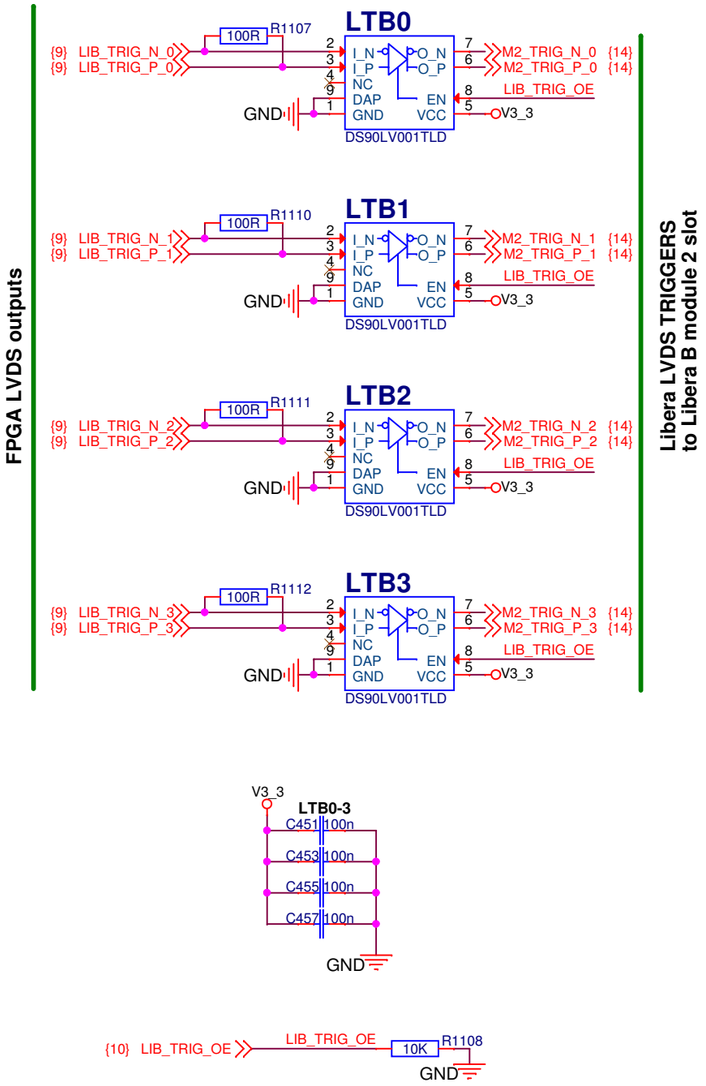
AMC card presence detection. PS1 "shorted" to PS0 when card fully inserted into host.

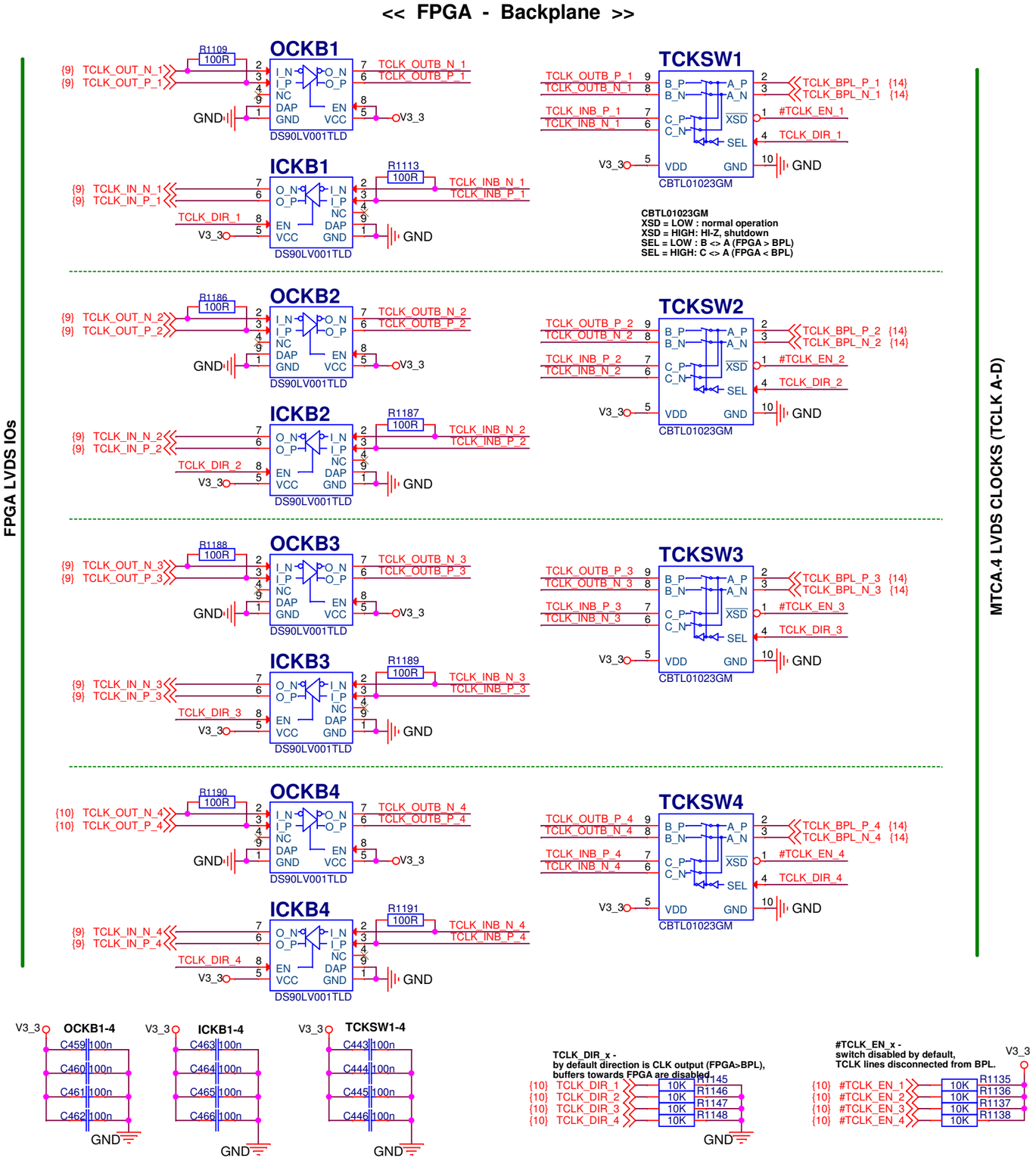




Title	AMC backplane plug		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 14 OF 17	

Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers





Title	Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 15 OF 17	

Backplane buffers - MTCA.4 PORT 17-20 (M-LVDS triggers, clocks, gates)

FPGA LVDS IOs

{10} MLVDIO_FSEN >> MLVDIO_FSEN
{10} #MLVDIO_PDN >> #MLVDIO_PDN

OTB1 SN65LVDT2DBV
{10} MLVDIO_OUT_P_1 → 3 (A)
{10} MLVDIO_OUT_N_1 → 4 (B)
2 (R) → GND
GND → 2 (GND)
5 (D) → MLVDIO_OUT_1
1 (VCC) → V3_3

OTB2 SN65LVDT2DBV
{10} MLVDIO_OUT_P_2 → 3 (A)
{10} MLVDIO_OUT_N_2 → 4 (B)
2 (R) → GND
GND → 2 (GND)
5 (D) → MLVDIO_OUT_2
1 (VCC) → V3_3

OTB3 SN65LVDT2DBV
{10} MLVDIO_OUT_P_3 → 3 (A)
{10} MLVDIO_OUT_N_3 → 4 (B)
2 (R) → GND
GND → 2 (GND)
5 (D) → MLVDIO_OUT_3
1 (VCC) → V3_3

OTB4 SN65LVDT2DBV
{10} MLVDIO_OUT_P_4 → 3 (A)
{10} MLVDIO_OUT_N_4 → 4 (B)
2 (R) → GND
GND → 2 (GND)
5 (D) → MLVDIO_OUT_4
1 (VCC) → V3_3

OTB5 SN65LVDT2DBV
{10} MLVDIO_OUT_P_5 → 3 (A)
{10} MLVDIO_OUT_N_5 → 4 (B)
2 (R) → GND
GND → 2 (GND)
5 (D) → MLVDIO_OUT_5
1 (VCC) → V3_3

OTB6 SN65LVDT2DBV
{10} MLVDIO_OUT_P_6 → 3 (A)
{10} MLVDIO_OUT_N_6 → 4 (B)
2 (R) → GND
GND → 2 (GND)
5 (D) → MLVDIO_OUT_6
1 (VCC) → V3_3

OTB7 SN65LVDT2DBV
{10} MLVDIO_OUT_P_7 → 3 (A)
{10} MLVDIO_OUT_N_7 → 4 (B)
2 (R) → GND
GND → 2 (GND)
5 (D) → MLVDIO_OUT_7
1 (VCC) → V3_3

OTB8 SN65LVDT2DBV
{10} MLVDIO_OUT_P_8 → 3 (A)
{10} MLVDIO_OUT_N_8 → 4 (B)
2 (R) → GND
GND → 2 (GND)
5 (D) → MLVDIO_OUT_8
1 (VCC) → V3_3

ITB1 SN65LVDS1DBV
{10} MLVDIO_IN_P_1 → 4 (Y)
{10} MLVDIO_IN_N_1 → 3 (Z)
V3_3 → 1 (VCC)
GND → 2 (GND)
5 (D) → MLVDIO_IN_1

ITB2 SN65LVDS1DBV
{10} MLVDIO_IN_P_2 → 4 (Y)
{10} MLVDIO_IN_N_2 → 3 (Z)
V3_3 → 1 (VCC)
GND → 2 (GND)
5 (D) → MLVDIO_IN_2

ITB3 SN65LVDS1DBV
{10} MLVDIO_IN_P_3 → 4 (Y)
{10} MLVDIO_IN_N_3 → 3 (Z)
V3_3 → 1 (VCC)
GND → 2 (GND)
5 (D) → MLVDIO_IN_3

ITB4 SN65LVDS1DBV
{10} MLVDIO_IN_P_4 → 4 (Y)
{10} MLVDIO_IN_N_4 → 3 (Z)
V3_3 → 1 (VCC)
GND → 2 (GND)
5 (D) → MLVDIO_IN_4

ITB5 SN65LVDS1DBV
{10} MLVDIO_IN_P_5 → 4 (Y)
{10} MLVDIO_IN_N_5 → 3 (Z)
V3_3 → 1 (VCC)
GND → 2 (GND)
5 (D) → MLVDIO_IN_5

ITB6 SN65LVDS1DBV
{10} MLVDIO_IN_P_6 → 4 (Y)
{10} MLVDIO_IN_N_6 → 3 (Z)
V3_3 → 1 (VCC)
GND → 2 (GND)
5 (D) → MLVDIO_IN_6

ITB7 SN65LVDS1DBV
{10} MLVDIO_IN_P_7 → 4 (Y)
{10} MLVDIO_IN_N_7 → 3 (Z)
V3_3 → 1 (VCC)
GND → 2 (GND)
5 (D) → MLVDIO_IN_7

ITB8 SN65LVDS1DBV
{10} MLVDIO_IN_P_8 → 4 (Y)
{10} MLVDIO_IN_N_8 → 3 (Z)
V3_3 → 1 (VCC)
GND → 2 (GND)
5 (D) → MLVDIO_IN_8

<< FPGA - Backplane >>

MTCA.4 M-LVDS TRIGGERS, GATES (PORT 17-20)

MTB1A SN65MLVD040RGZ

{10} MLVDIO_DE_4	1	1DE			
MLVDIO_OUT_4	35	1D	1A	47	MLVDIO_BPL_P_4 {14}
			1B	48	MLVDIO_BPL_N_4 {14}
MLVDIO_FSEN	39	1FSEN			
MLVDIO_IN_4	36	1R			
{10} #MLVDIO_RE_4	40	1RE			
{10} MLVDIO_DE_3	5	2DE			
MLVDIO_OUT_3	32	2D	2A	3	MLVDIO_BPL_P_3 {14}
			2B	4	MLVDIO_BPL_N_3 {14}
MLVDIO_FSEN	41	2FSEN			
MLVDIO_IN_3	33	2R			
{10} #MLVDIO_RE_3	42	2RE			
{10} MLVDIO_DE_2	8	3DE			
MLVDIO_OUT_2	28	3D	3A	9	MLVDIO_BPL_P_2 {14}
			3B	10	MLVDIO_BPL_N_2 {14}
MLVDIO_FSEN	20	3FSEN			
MLVDIO_IN_2	29	3R			
{10} #MLVDIO_RE_2	19	3RE			
{10} MLVDIO_DE_1	12	4DE			
MLVDIO_OUT_1	25	4D	4A	13	MLVDIO_BPL_P_1 {14}
			4B	14	MLVDIO_BPL_N_1 {14}
MLVDIO_FSEN	22	4FSEN			
MLVDIO_IN_1	26	4R			
{10} #MLVDIO_RE_1	21	4RE			
		PDN		30	#MLVDIO_PDN

MTB2A SN65MLVD040RGZ

{10} MLVDIO_DE_8	1	1DE			
MLVDIO_OUT_8	35	1D	1A	47	MLVDIO_BPL_P_8 {14}
			1B	48	MLVDIO_BPL_N_8 {14}
MLVDIO_FSEN	39	1FSEN			
MLVDIO_IN_8	36	1R			
{10} #MLVDIO_RE_8	40	1RE			
{10} MLVDIO_DE_7	5	2DE			
MLVDIO_OUT_7	32	2D	2A	3	MLVDIO_BPL_P_7 {14}
			2B	4	MLVDIO_BPL_N_7 {14}
MLVDIO_FSEN	41	2FSEN			
MLVDIO_IN_7	33	2R			
{10} #MLVDIO_RE_7	42	2RE			
{10} MLVDIO_DE_6	8	3DE			
MLVDIO_OUT_6	28	3D	3A	9	MLVDIO_BPL_P_6 {14}
			3B	10	MLVDIO_BPL_N_6 {14}
MLVDIO_FSEN	20	3FSEN			
MLVDIO_IN_6	29	3R			
{10} #MLVDIO_RE_6	19	3RE			
{10} MLVDIO_DE_5	12	4DE			
MLVDIO_OUT_5	25	4D	4A	13	MLVDIO_BPL_P_5 {14}
			4B	14	MLVDIO_BPL_N_5 {14}
MLVDIO_FSEN	22	4FSEN			
MLVDIO_IN_5	26	4R			
{10} #MLVDIO_RE_5	21	4RE			
		PDN		30	#MLVDIO_PDN

/RE and FSEN pins have internal pull-UP resistors.
DE and /PDN pin has internal pull-DOWN resistors.

MLVDIO_IN_1	10K	R1153
MLVDIO_IN_2	10K	R1154
MLVDIO_IN_3	10K	R1155
MLVDIO_IN_4	10K	R1156
MLVDIO_IN_5	10K	R1157
MLVDIO_IN_6	10K	R1158
MLVDIO_IN_7	10K	R1159
MLVDIO_IN_8	10K	R1160

Define state when /RE is HI. → GND

MTB1B SN65MLVD040RGZ
49 THP; 6 1GND; 7 2GND; 18 3GND; 23 4GND; 27 7GND; 31 6GND; 34 5GND; 38 9GND; 43 8GND
44 2NC; 17 1NC
2 1VCC; 11 2VCC; 15 3VCC; 16 4VCC; 24 5VCC; 37 6VCC; 45 7VCC; 46 8VCC
V3_3
C389 100n, C413 100n, C414 100n, C415 100n, C416 100n, C417 100n, C418 100n, C419 100n
GND, GND

MTB2B SN65MLVD040RGZ
49 THP; 6 1GND; 7 2GND; 18 3GND; 23 4GND; 27 7GND; 31 6GND; 34 5GND; 38 9GND; 43 8GND
44 2NC; 17 1NC
2 1VCC; 11 2VCC; 15 3VCC; 16 4VCC; 24 5VCC; 37 6VCC; 45 7VCC; 46 8VCC
V3_3
C390 100n, C420 100n, C421 100n, C422 100n, C423 100n, C424 100n, C425 100n, C426 100n
GND, GND

OTB1-8
V3_3
C431 100n, C432 100n, C433 100n, C434 100n, C427 100n, C428 100n, C429 100n, C430 100n
GND, GND

ITB1-8
V3_3
C435 100n, C436 100n, C437 100n, C438 100n, C439 100n, C440 100n, C441 100n, C442 100n
GND, GND

Title	Backplane buffers - MTCA.4 PORT 17-20 (M-LVDS triggers, clocks, gates)	
Size A3 / Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 16 OF 17

Backplane buffers - MTCA.4 PORT 12-15 (High Speed Serial)

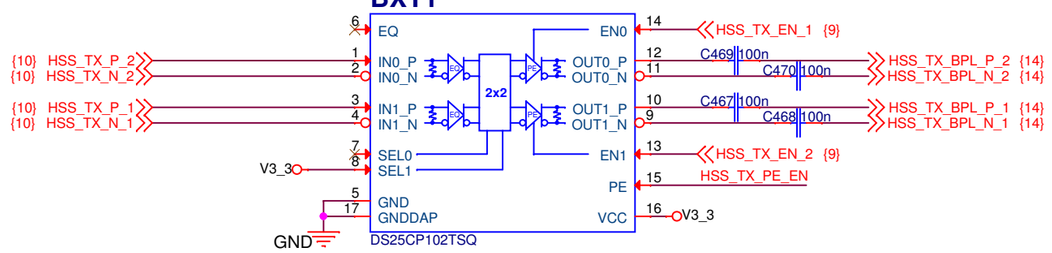
IMPORTANT!
Hi speed Gigabit lines
100R differential

FPGA BANK GXB L0, Gigabit Transceivers

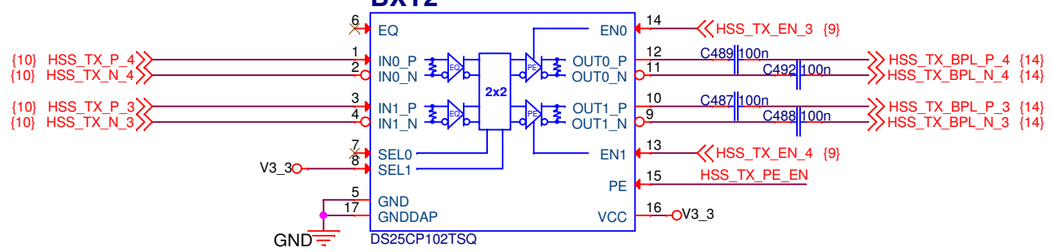
<< FPGA - Backplane >>

{9} HSS_RX_EQ_EN
{9} HSS_TX_PE_EN
HSS_RX_EQ_EN
HSS_TX_PE_EN

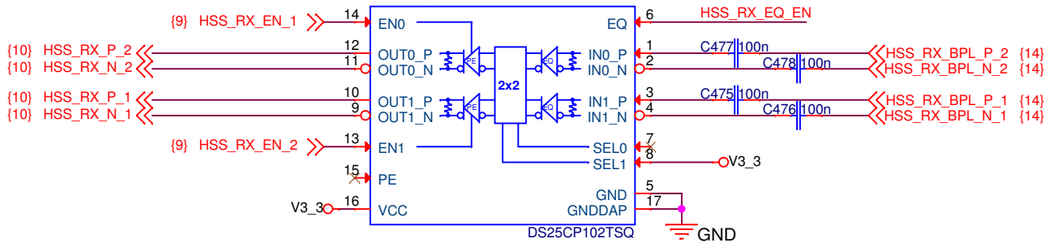
BXT1



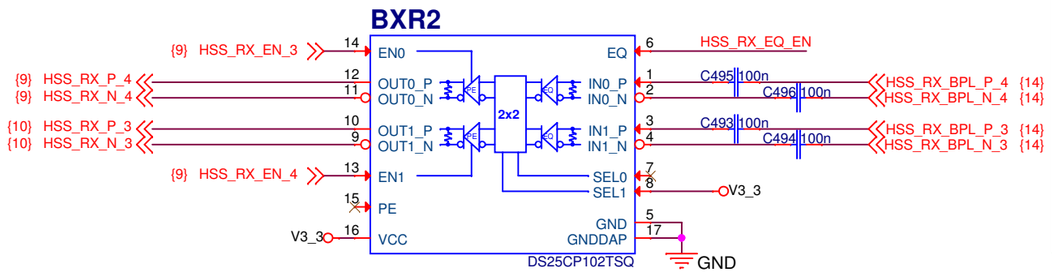
BXT2



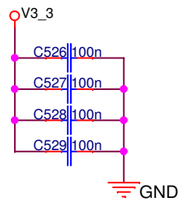
BXR1



BXR2



PE - Transmit Pre-Emphasis select pin. There is a 20k pulldown resistor on this pin
EQ - Receive Equalization select pin. There is a 20k pulldown resistor on this pin.
SEL0, SEL1 - Switch configuration pins. There is a 20k pulldown resistor on this pin.



MTCA.4 backplane PORTs 12-15,

Title	Backplane buffers - MTCA.4 PORT 12-15 (High Speed Serial)		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 17 OF 17	