FAIR Timing Receiver AMC form factor - CSL_FTRN_AMC
Single width, mid-height

DATE	REVISION DESCRIPTION	DRAWN	REV
01.09.2014	Initial version	dslavinec	A
19.09.2014	Flattened IO blocks	dslavinec	A
02.12.2014	Updates after QA review	dslavinec	A
16.04.2015	Added ADC clock generation and trigger signals to backplane, moved LVTTL_CLK, nRES and FPGA_RES to different FPGA pins	dslavinec	A
23.07.2015	removed ADC clocking page, only one set of triggers to backplane kept, incorporated changes from PMC (LED driving), added power mux for MMC	dslavinec	A
17.08.2015	added sheet 15 with MTCA.4 triggers and clocks to/from backplane	dslavinec	A
01.10.2015	MTCA.4 out clocks not connected to clk outputs, backplane buffers enable signals connected only to FPGA	dslavinec	A
27.11.2015	MTCA.4 connections to backplane finished, MMC PGOOD modified, relevant updates from PMC, MMC reset modified	dslavinec	A
09.12.2015	MTCA.4 HSS connections (backplane ports 12-15) moved from FPGA GXB banks to LVDS IOs	dslavinec	A
16.12.2015	libera triggers, MTCA.4 tclk and mlvdios moved to top FPGA banks	dslavinec	A
16.06.2016	LTM4620 replaced with LTM4619, FPGA core voltage increased to 1.15V, different TCLK buffers, larger LED resistors, replaced IO TVS	dslavinec	A
26.07.2017	one LTM4619 reverted back to LTM4620, added resistors for LTM mode configuration, modified JTAG chain connections, added JTAG switch indicator, WR/STATUS LEDs replaced with 90deg, WR and OSC clk lines back to AC-coupling	dslavinec	A
05.02.2018	Page 02: - updated block diagram Page 04: - DZ2 replaced with lower package variant - changed PRESENT_V12AUX circuit: DZ5 replaced with lower package variant, removed DZ3; added POWAP1 3.3V voltage regulator, R150 value to 1k Page 05: - added R17, R18 on the POWVLC5, POWVLC9 outputs as minimal load for LDOs - Caps C58,C72,C80,C261,C272,C274 replaced with lower package variant Page 06: - R193,R194 marked as DNP - added : R74 pull-down on nCONFIG_PROG; R92 pull-up on nCONFIG; R192 pull-up on #MMC_FPGA_CONFIG Page 07: - changed values of R115,R111,R112,R114,R119,R116 and led colors of D26,D28,D30,D31,D27,D29; - USBCON1 shield pins connected to FACE_PLATE Page 08: - Caps C289,C306,C309,C310,326,C337 replaced with lower package variant Page 09: - added AC-coupling caps C357,C358 on PCIe RX Page 13: - Caps C395,C396,C410 replaced with lower package variant - changed value of current limit resistor R1095 to 220R, added 1K5 R1096, to set current limit of PMX1 to max ~148mA - added C20, C21 to the PMC1 inputs - replaced JTAG1 connector with the one with keying to ensure proper connection of the JTAG cable - MMC1A P1.19: removed MMC_ULED_0 (R96, DU1), connected PRESENT_V12AUX to P1.19 - MMC1A P1.26: renamed to JTRCK_MMC, connected to pin7 of the JTAG1 via R1036, added pull-down R1033 - added R304 pull-up and Q11 for driving HotSwap LED (same as on DENX reference board) - led D33 changed to green, D20 changed to red, swapped values for R301,R302 - IC1 (FT230XQ) power source changed to USB 5V; added L22 and C374 on the USB 5V rail; removed C374; C380 to V33_USB rail; removed R162,R163; added IC4,C362,R169 to buffer RX line towards MMC; added IC5,C364,R170 to buffer TX line towards FTD; optional R162,R163 instead of IC4,IC5; - USBCON2 shield pins connected to FACE_PLATE Page 14: - MMC_I2C_SDA connected via R121 to DIP1 switch (option to boot MMC bootloader) Page 15: - R1108 value to 2K on LIB_TRIG_EN as stronger pull-down to overcome 20k FPGA pull-up during FPGA boot Page 16: - added pull-down R359 to #MLVDIO_PDN to overcome 20k FPGA pull-up during FPGA boot Page 17: - added pull-down R360,R361,R362,R363 to HSS_TX_EN_x to overcome 20k FPGA pull-up during FPGA boot	dslavinec	B
24.08.2018	Page 14: - C376, C377 marked as DNP (Do Not Place) - AMCPLG1 value to PCB_AMC_PLUG, since plug is implemented on the PCB	dslavinec	B

SHEET	TITLE
1	TITLE PAGE
2	Block diagram
3	Power Tree
4	POWER DC-DC
5	POWER LDOs, FPGA BYPASS
6	FPGA configuration
7	FPGA user interface
8	WR clocking, system CLOCKS
9	PCIe, SFP
10	IO power and IO FPGA
11	IO blocks 1-4
12	IO block 5
13	IPMI MMC
14	AMC BACKPLANE PLUG
15	Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers
16	Backplane buffers - MTCA.4 PORTs 17-20
17	Backplane buffers - MTCA.4 PORTs 12-15

Value	Capatitors used
12p	0402, 50V, C0G, 1%
22p	0402, 50V, C0G, 1%
10n	0402, 25V, X7R, 10%
100n	0402, 25V, X7R, 10%
1u	0603, 16V, X7R, 10%
2.2u	1206, 25V, X7R, 10%
2.2u	1210, 100V, X7R, 10%
10u	0805, 10V, X7R, 10%
10u	1210, 25V, X7R, 10%
22u	1206, 10V, X7R, 10%
22u	1210, 10V, X7R, 10%
100u	1210, 10V, X5R, 20%

All resistors are SMD 0402, 63mW, 1%
except where marked differently.

Components marked DNP
(Do Not Place) are foreseen
for testing purposes and
should NOT be placed.

TOP layer

FM1	FM2	FM3
FIDUCIAL	FIDUCIAL	FIDUCIAL

BOTTOM layer

FM4	FM5	FM6
FIDUCIAL	FIDUCIAL	FIDUCIAL

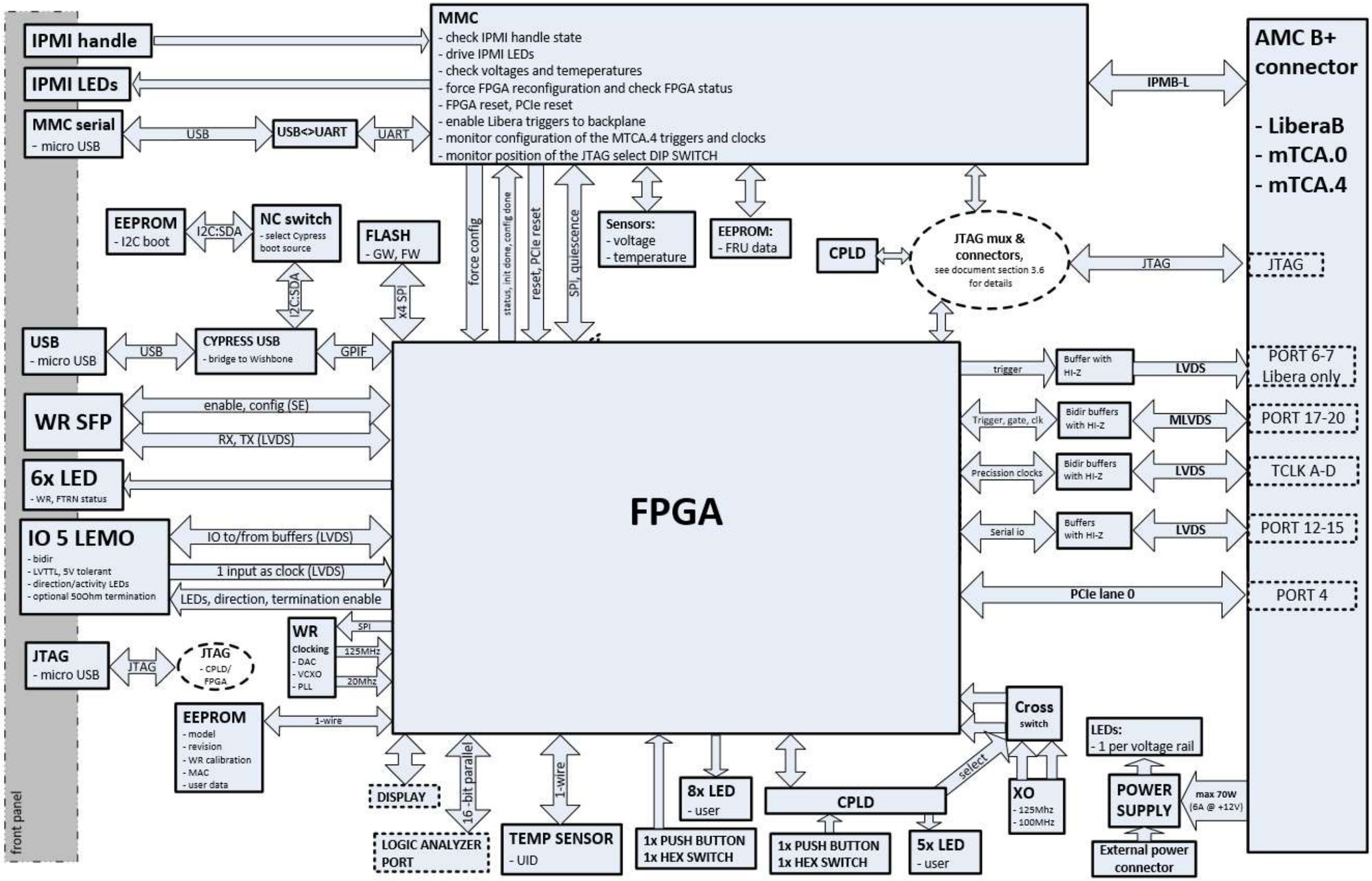
DRAWN	Dušan Slavinec		05.02.2018
CHECKED	-		
APPROVED	-		

Title

Size	Type	DWG.NO.	REV.
A3	SE	CSL_FTRN_AMC	B

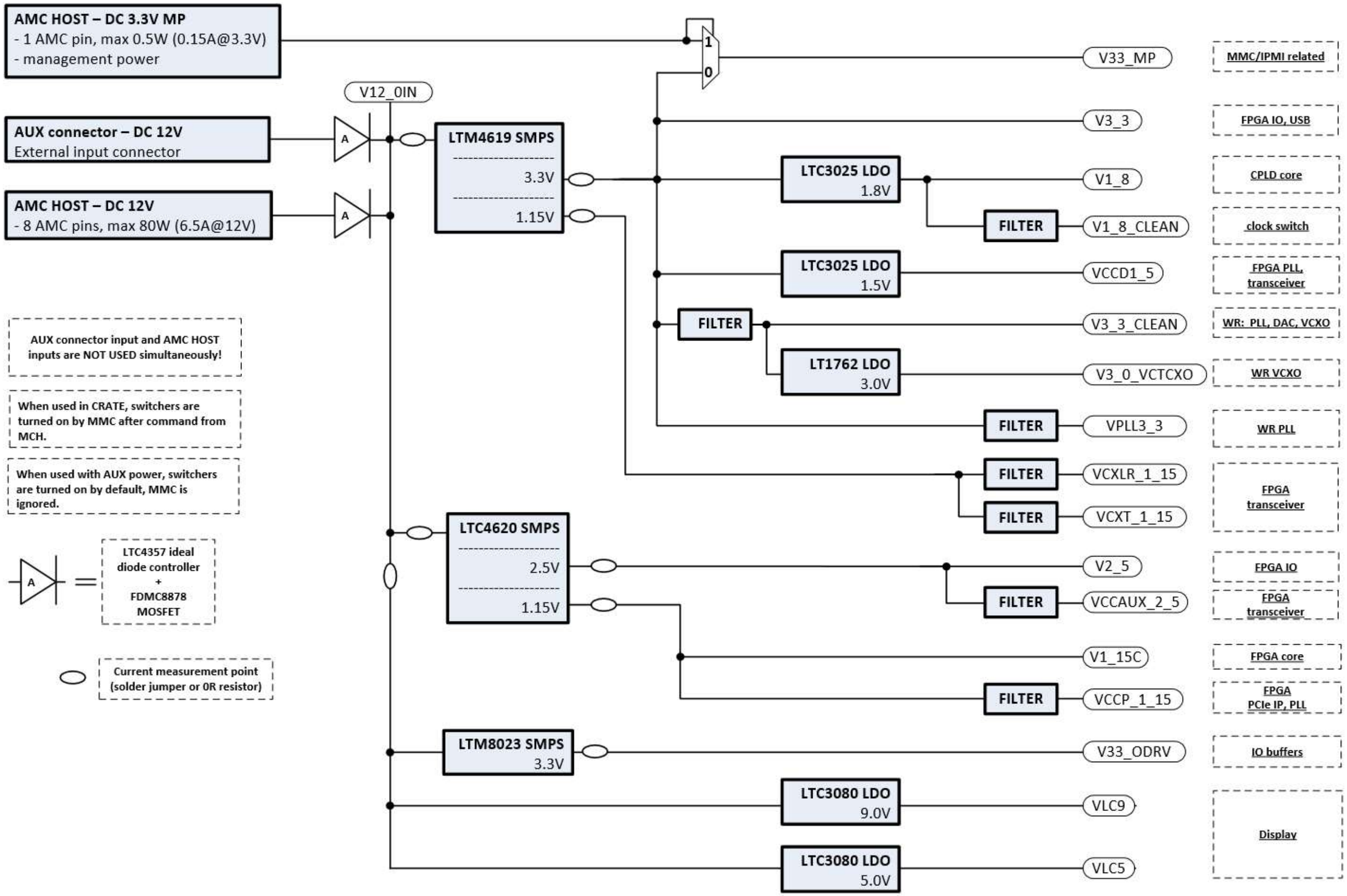
SHEET 1 OF 17

Block Diagram - FTRN, MMC



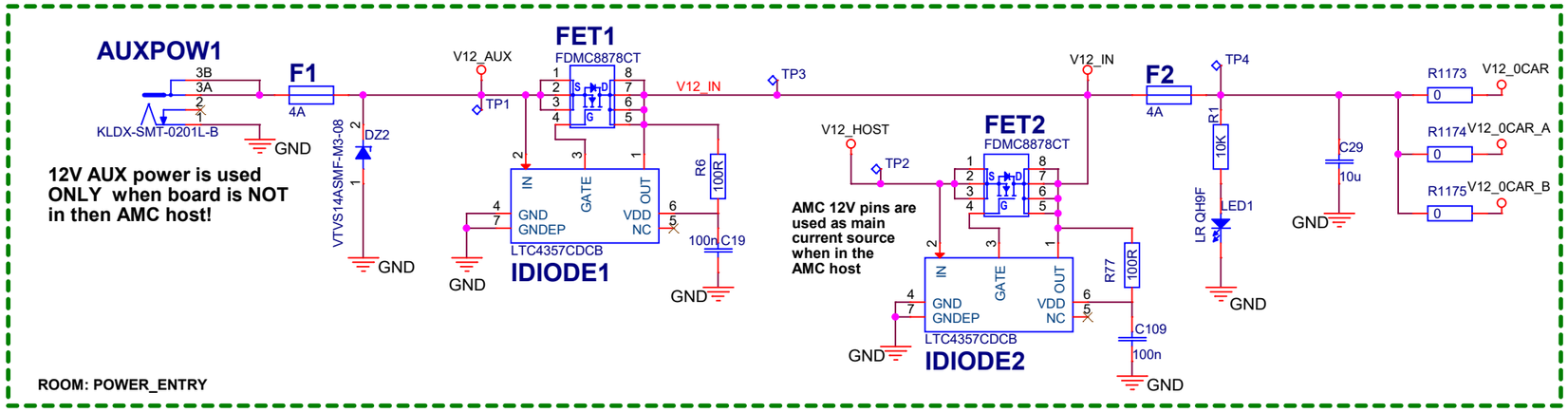
Title: Block Diagram - FTRN, MMC			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 2 OF 17

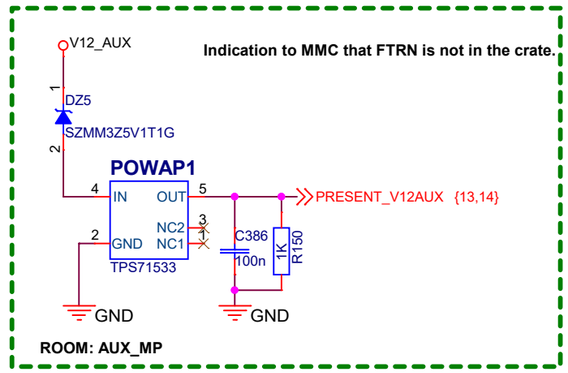
Power tree block scheme



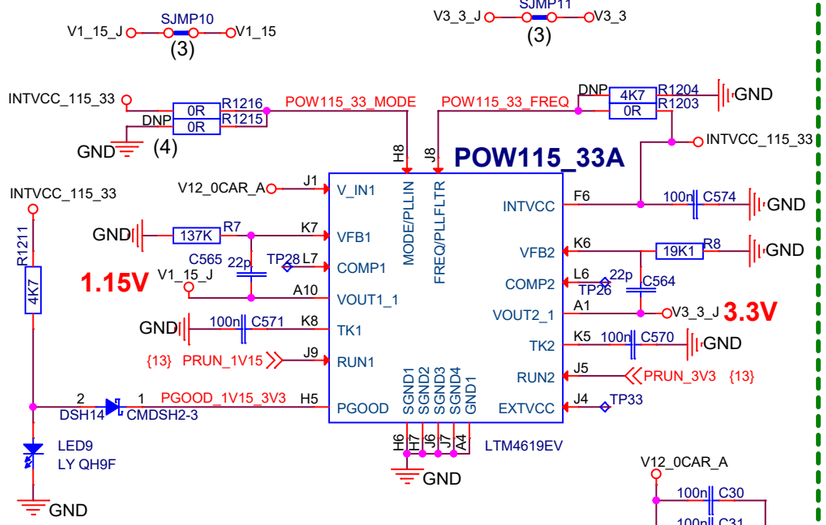
Title: Power tree block scheme			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 3 OF 17

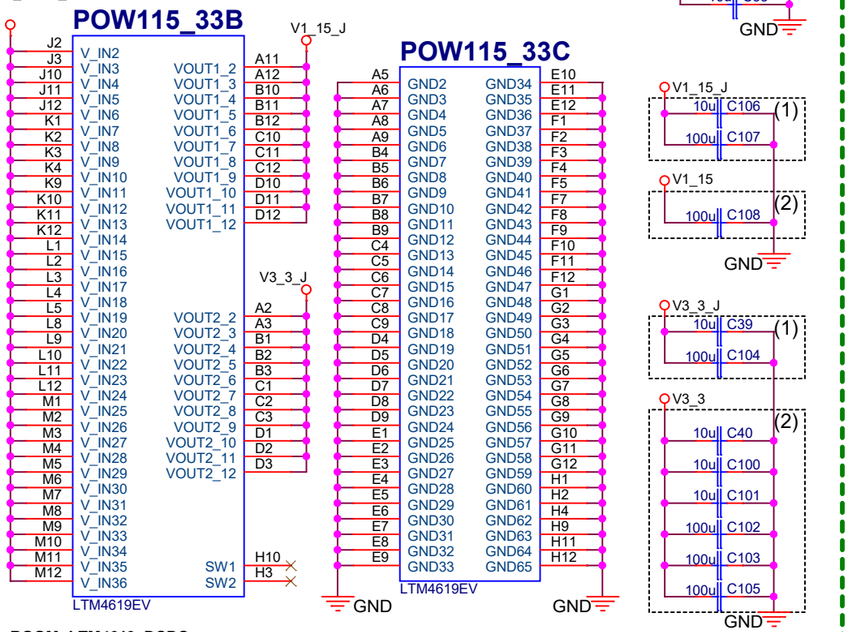
Power entry and main DCDC power regulators





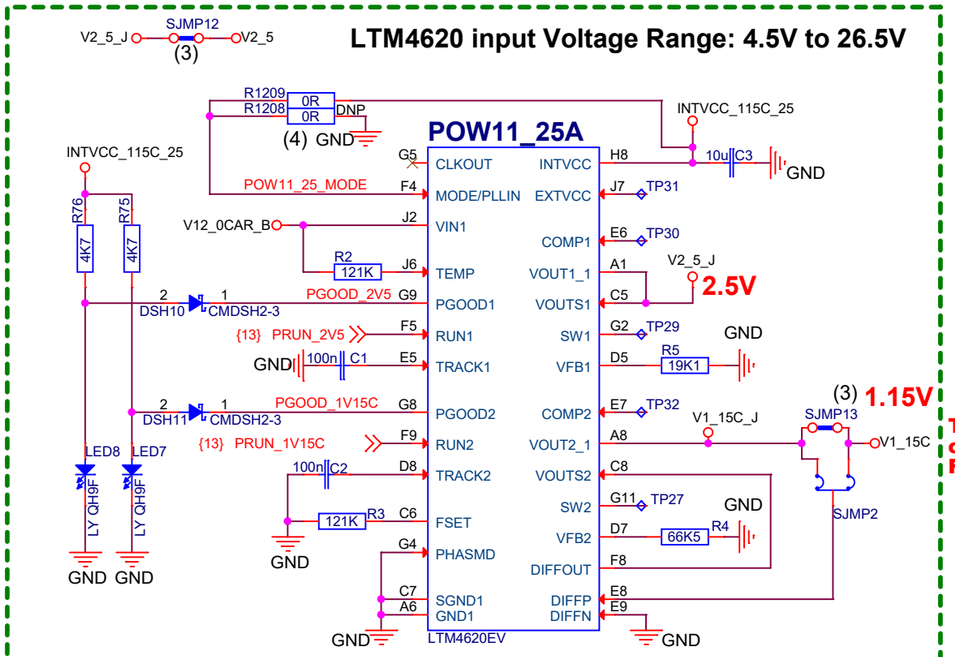
LTM4619 input Voltage Range: 4.5V to 26.5V

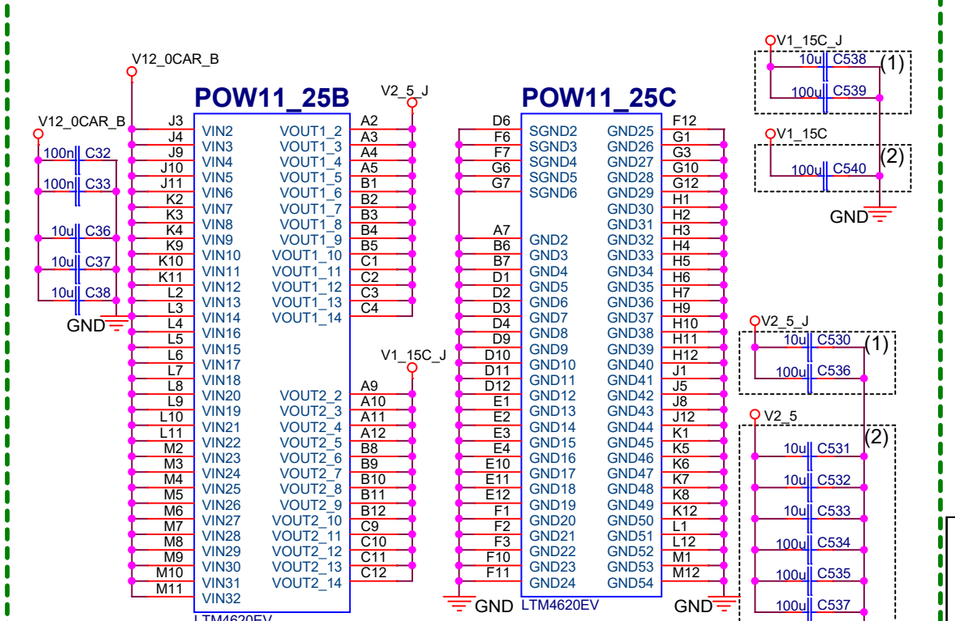




ROOM: LTM4619_DCDC

LTM4620 input Voltage Range: 4.5V to 26.5V





ROOM: LTM4620_DCDC

PGOOD indicators to MMC

PGOOD_1V15C {13}
PGOOD_2V5 {13}
PGOOD_1V15_3V3 {13}

(1) - place capacitors on the regulator outputs

(2) - place capacitors away from the regulator outputs

(3) - solder jumper, to test power regulator outputs before powering FPGA and current measurement

(4) - None or only one resistor is placed to select converter mode (pulse-skipping, burst, continous)

Title	Power entry and main DCDC power regulators		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. B
		SHEET 4 OF 17	

FPGA decoupling, LDO regulators, power indicators

LOG1R

AA22	GND1	GND74	L25
AA25	GND2	GND75	L26
AA26	GND3	GND76	L5
AB11	GND4	GND77	L8
AB14	GND5	GND78	M11
AB17	GND6	GND79	M13
AB20	GND7	GND80	M15
AB23	GND8	GND81	M17
AB24	GND9	GND82	M19
AB5	GND10	GND83	M23
AB8	GND11	GND84	M24
AC2	GND12	GND85	M9
AC24	GND13	GND86	N10
AC25	GND14	GND87	N12
AC26	GND15	GND88	N14
AE11	GND16	GND89	N16
AE14	GND17	GND90	N20
AE17	GND18	GND91	N22
AE2	GND19	GND92	N25
AE20	GND20	GND93	N26
AE22	GND21	GND94	N8
AE5	GND22	GND95	P11
AE8	GND23	GND96	P13
AF2	GND24	GND97	P15
B11	GND25	GND98	P17
B14	GND26	GND99	P19
B17	GND27	GND100	P2
B2	GND28	GND101	P23
B20	GND29	GND102	P24
B23	GND30	GND103	P5
B26	GND31	GND104	R10
B5	GND32	GND105	R12
B8	GND33	GND106	R14
C26	GND34	GND107	R16
D23	GND35	GND108	R20
D24	GND36	GND109	R22
E11	GND37	GND110	R25
E14	GND38	GND111	R26
E17	GND39	GND112	R8
E2	GND40	GND113	T11
E20	GND41	GND114	T13
E22	GND42	GND115	T15
E25	GND43	GND116	T17
E26	GND44	GND117	T19
E5	GND45	GND118	T21
E8	GND46	GND119	T23
F23	GND47	GND120	T24
F24	GND48	GND121	T5
G22	GND49	GND122	T9
G25	GND50	GND123	U16
G26	GND51	GND124	U2
G5	GND52	GND125	U20
H11	GND53	GND126	U25
H14	GND54	GND127	U26
H17	GND55	GND128	U8
H2	GND56	GND129	V18
H20	GND57	GND130	V19
H23	GND58	GND131	V21
H24	GND59	GND132	V22
H5	GND60	GND133	V23
H8	GND61	GND134	V24
J22	GND62	GND135	W11
J25	GND63	GND136	W14
J26	GND64	GND137	W17
K11	GND65	GND138	W20
K23	GND66	GND139	W22
K24	GND67	GND140	W25
L14	GND68	GND141	W26
L16	GND69	GND142	W5
L19	GND70	GND143	W8
L2	GND71	GND144	Y2
L20	GND72	GND145	Y23
L22	GND73	GND146	Y24
AD1	DNU1	DNU5	H6
AD2	DNU2	DNU6	K14
C25	DNU3	DNU7	V14
D25	DNU4	DNU8	V20

5AGXMA3D4F27I3N

GND

LOG1P

V1_15C

M10	VCC1	
M12	VCC2	
M14	VCC3	
M16	VCC4	
N11	VCC5	
N13	VCC6	
N15	VCC7	
N9	VCC8	
P10	VCC9	
P12	VCC10	
P14	VCC11	
P16	VCC12	
P9	VCC13	
R11	VCC14	
R13	VCC15	
R15	VCC16	
R9	VCC17	
T10	VCC18	
T12	VCC19	
T14	VCC20	
T16	VCC21	

VCCP_1_15

L11	VCCP1	
L15	VCCP2	
L9	VCCP3	
M8	VCCP4	
N17	VCCP5	
R17	VCCP6	
T8	VCCP7	
U11	VCCP8	
U15	VCCP9	
U9	VCCP10	

VCCAUX_2_5

L10	VCC_AUX1	
L17	VCC_AUX2	
U10	VCC_AUX3	
U17	VCC_AUX4	
U14		

L13	VCCA_FPLL1	
P18	VCCA_FPLL2	
P7	VCCA_FPLL3	
M18	VCCA_FPLL4	
	VCCA_FPLL5	

VCCD_1_5

U13	VCCD_FPLL1	
L12	VCCD_FPLL2	
T18	VCCD_FPLL3	
N7	VCCD_FPLL4	
L18	VCCD_FPLL5	

	VCCIO3A_1	AA19
	VCCIO3A_2	AB22
	VCCIO3A_3	AD21
	VCCIO3D_1	AC15
	VCCIO3D_2	AC18
	VCCIO3D_3	AF17
	VCCIO3D_4	Y15
	VCCIO4A_1	Y3
	VCCIO4A_2	Y6
	VCCIO4C_1	AB7
	VCCIO4C_2	AC4
	VCCIO4C_3	AE7
	VCCIO4C_4	AF4
	VCCIO4D_1	AB10
	VCCIO4D_2	AC12
	VCCIO4D_3	AF10
	VCCIO4D_4	Y12
	VCCIO5A_1	N4
	VCCIO5A_2	R1
	VCCIO5A_3	R4
	VCCIO5A_4	U4
	VCCIO6A_1	G1
	VCCIO6A_2	K1
	VCCIO6A_3	M5
	VCCIO6A_4	H4
	VCCIO7A_1	D3
	VCCIO7A_2	F5
	VCCIO7C_1	A7
	VCCIO7C_2	D7
	VCCIO7C_3	F9
	VCCIO7C_4	G7
	VCCIO7D_1	A10
	VCCIO7D_2	C13
	VCCIO7D_3	D10
	VCCIO7D_4	F13
	VCCIO8A_1	D22
	VCCIO8A_2	F21
	VCCIO8A_3	G19
	VCCIO8D_1	A18
	VCCIO8D_2	C16
	VCCIO8D_3	D18
	VCCIO8D_4	F15

5AGXMA3D4F27I3N

LOG1Q

VCCAUX_2_5

T20	VCCA_GXBL0	
M20	VCCA_GXBL1	
VCCD_1_5 P20	VCCH_GXBL0	
L21	VCCH_GXBL1	
VCXLR_1_15 P21	VCCL_GXBL0_1	
P22	VCCL_GXBL0_2	
K22	VCCL_GXBL1	
K21	VCCR_GXBL_1	
N21	VCCR_GXBL_2	
U21	VCCR_GXBL_3	
U22	VCCR_GXBL_4	
VCXT_1_15 R21	VCCT_GXBL0_1	
T22	VCCT_GXBL0_2	
M21	VCCT_GXBL1_1	
M22	VCCT_GXBL1_2	
VCCD_1_5 J21	VCCBAT	
2K R11 D26	RREF_TL	
2K R12 AE1	RREF_BR	

	VCCPD3_1	V17
	VCCPD3_2	W19
	VCCPD5_1	R7
	VCCPD5_2	P8
	VCCPD6_1	M7
	VCCPD6_2	L7
	VCCPD8_1	K16
	VCCPD8_2	K19
	VCCPD4A	V8
	VCCPD7A	K8
	VCCPD4BCD_1	U12
	VCCPD4BCD_2	V11
	VCCPD7BCD_1	K13
	VCCPD7BCD_2	K9
	VCCPGM1	H7
	VCCPGM2	W21

5AGXMA3D4F27I3N

GND

V2_5 V3_3 V3_3

VCC 1.15V

V1_15C 21x

100n C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94 C95 C96 C97 C98 C99 C122 C123 C132 C133 C134

GND

VCCP 1.15V

V1_15C 10x

100n C135 C136 C137 C138 C139 C140 C141 C142 C143 C144

10u C286 C287 C288 C289

GND

ROOM: CAPS_VCC_1_1

VCCP 1.15V

VCCP_1_15 10x

100n C222 C223 C224 C225 C226 C227 C228 C229 C230 C231

GND

ROOM: CAPS_VCCP_1_1

VCCP 1.15V

VCCP_1_15

100n C276 C277 C278 C279

10u C272 C273 C274 C275

GND

VCCT_GXB

VCXT_1_15

100n C280 C281 C282 C283

10u C284 C285

GND

VCCR_GXB VCCL_GXB

VCXLR_1_15 7x

100n C264 C265 C266 C267 C268 C269 C270

10u C262 C263

GND

ROOM: CAPS_VCC_GX_1_15

VCCD_FPLL VCCH_GXBL VCCBAT

VCCD_1_5 8x

100n C214 C215 C216 C217 C218 C219 C220 C221

GND

ROOM: CAPS_VCC_1_5

VCCIO 2.5V

V2_5 22x

100n C145 C146 C147 C148 C149 C150 C151 C152 C153 C154 C155 C156 C157 C158 C159 C160 C161 C162 C163 C164 C165 C166

GND

VCCPD 2.5V

V2_5 6x

100n C170 C171 C172 C173 C174 C175

GND

ROOM: CAPS_VCC_2_5

VCCAUX 2.5V VCCA_FPLL VCCA_GXB

VCCAUX_2_5 9x

100n C232 C233 C234 C235 C236 C237 C238 C239 C240

4x

100n C242 C257 C258 C259

10u C260 C261

GND

ROOM: CAPS_VCCAUX_2_5

VCCIO 3.3V

V3_3 20x

100n C193 C194 C195 C196 C197 C198 C199 C200 C201 C202 C203 C204 C205 C206 C207 C208 C209 C210 C211 C212

GND

ROOM: CAPS_VCCIO_3_3

VCCPD 3.3V

V3_3 10x

100n C213 C183 C184 C185 C186 C187 C188 C189 C190 C191

GND

ROOM: CAPS_VCCPD_3_3

POWcpld18 — LDO 1.8V for CPLD, WR CLOCK SWITCH

V3_3 — C53 100n — VIN VOUT ADJ BIAS GND SHDN GNDP — LTC3025EDC — 30K1 R9 — 8K45 R10 — C54 100n C56 10u C57 1u C55 100n — V1_8_J (1) SJMP5 — V1_8 — L1 BLM18PG121 — TP11 — V1_8_CLEAN — C58 10u — GND

POW_1_5 — LDO 1.5V for VCCH_GXB VCCD_FPLL, VCC_BAT

V3_3 — C77 100n — VIN VOUT ADJ BIAS GND SHDN GNDP — LTC3025EDC — 30K1 R15 — 10K7 R16 — C78 100n C80 10u C81 1u C79 100n — TP12 — VCCD_1_5_J — SJMP6 (1) — VCCD_1_5 — GND

ROOM: POWER_LDO

POWVLC5 — LDO 5.0V for LCD

V12_0CAR — C73 100n — IN1 IN2 IN3 VCON — OUT1 OUT2 OUT3 EPAD SET — LT3080EDD — R14 510K — C74 100n C76 10u C75 100n — R18 4K7 — TP13 — VLC5_J — SJMP7 (1) — VLC5 — GND

POWVLC9 — LDO 9.0V for LCD

V12_0CAR — C69 100n — IN1 IN2 IN3 VCON — OUT1 OUT2 OUT3 EPAD SET — LT3080EDD — R13 806K — C70 100n C72 10u C71 100n — R17 4K7 — VLC9 — TP14 — GND

ROOM: POWER_LCD_LDO

V2_5 — IND1 BLM31PG121SN1L — VCCAUX_2_5 — C61 100n C62 10u — GND

V1_15C — IND2 BLM31PG121SN1L — VCCP_1_15 — C63 100n C64 10u — GND

V1_15 — IND3 BLM31PG121SN1L — VCXLR_1_15 — C65 100n C66 10u — GND

V1_15 — IND4 BLM31PG121SN1L — VCXT_1_15 — C67 100n C68 10u — GND

ROOM: POWER_FILTERS

VLC5 — R32 2K — LED_5 LR QH9F

V3_3 — R33 1K5 — LED_33 LR QH9F

V12_IN — V1_8 — R21 10K — LED_18 LR QH9F — MMBT3904 Q1 — R20 22K — R22 1K

V12_IN — V1_15 — R23 10K — LED_115 LR QH9F — MMBT3904 Q2 — R25 22K — R24 1K

V12_IN — V1_15C — R26 10K — LED_11 LR QH9F — MMBT3904 Q3 — R28 22K — R27 1K

V12_IN — VCCD_1_5 — R29 10K — LED_15 LR QH9F — MMBT3904 Q4 — R31 22K — R30 1K

GND

ROOM: POWER_INDICATORS

IMPORTANT! (LOG1Q)
In the PCB layout, the traces from FPGA pins D26 and AE1 to the R11 and R12 resistors need to be routed so that they avoid any aggressor signals. R11 and R12 must be 1% or better!

IMPORTANT!
Separate VCC and VCCP planes into two different power layers on the PCB!

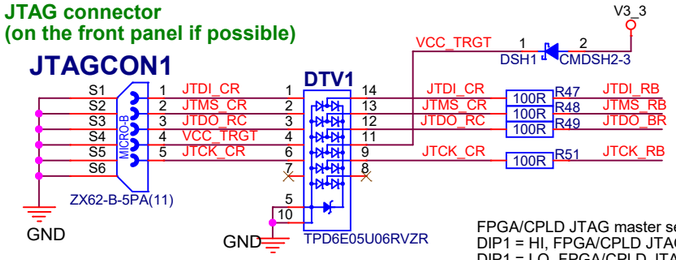
(1) - 0R solder connection, to test regulator outputs before connecting to load

Title	FPGA decoupling, LDO regulators, power indicators		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. B
			SHEET 5 OF 17

FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash

JTAG signals flow :
C (USB connector) > R (resistor) > B (buffer) > P (PROG - CPLD) > F (FPGA) > B > C
or
BPL (backplane) > BB (backplane buffer) > BS (backplane JTAG switch) > R (resistor) > P (PROG - CPLD) > F (FPGA) > R > BS > BB > BPL

JTAG connector
(on the front panel if possible)

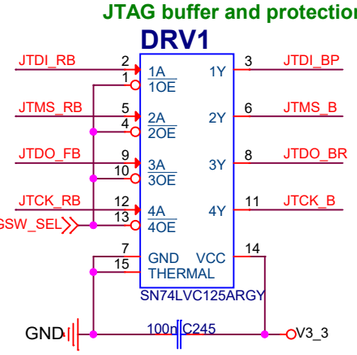


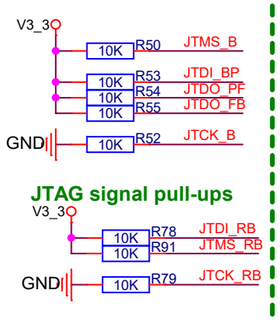
Straight-through Routing

FPGA/CPLD JTAG master select (DIP1, p14):
DIP1 = HI, FPGA/CPLD JTAG from backplane
DIP1 = LO, FPGA/CPLD JTAG from front panel connector

Parallel to USB connector JTAG signals are JTAG signals from JSW1 swtich (JTAG from backplane)

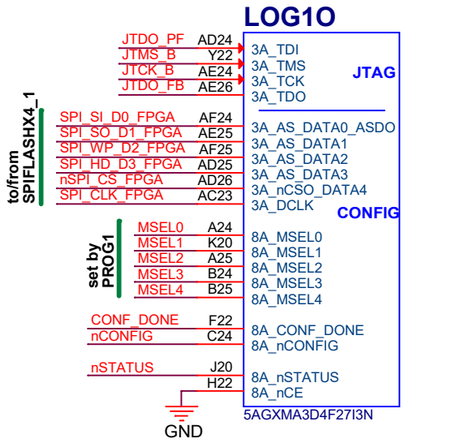
JTAG buffer and protection

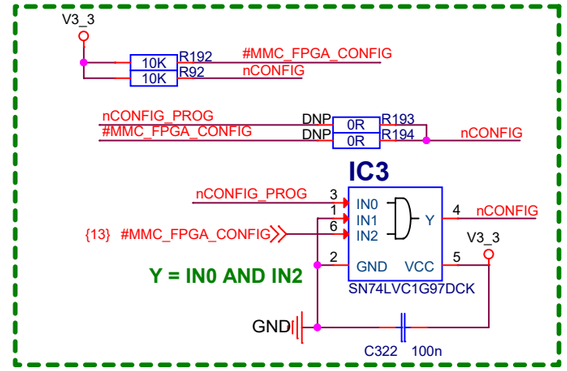




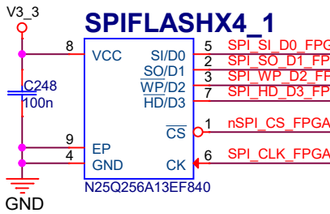
JTAG signal pull-ups

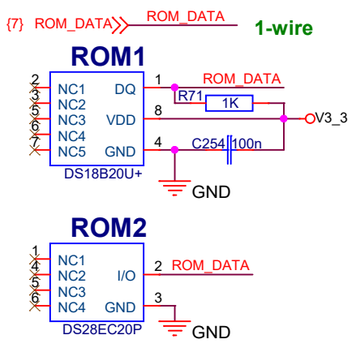
ROOM: FPGA_CPLD_JTAG_INPUT





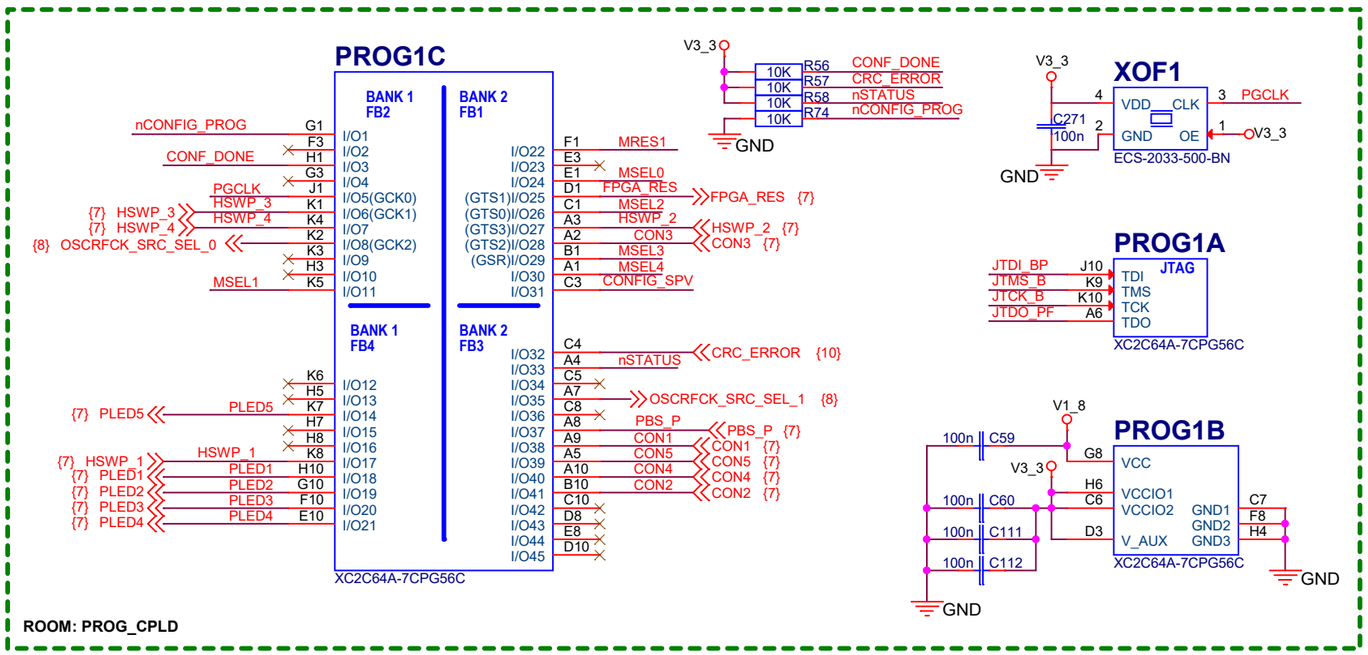
ROOM: MEMORY





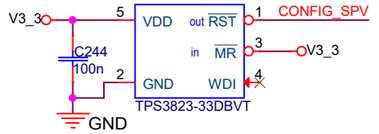
ROOM: MEMORY

FPGA status to MMC

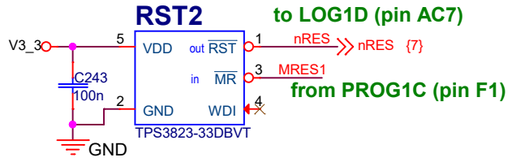


ROOM: PROG_CPLD

RST1 — **to PROG1C (pin C3)**



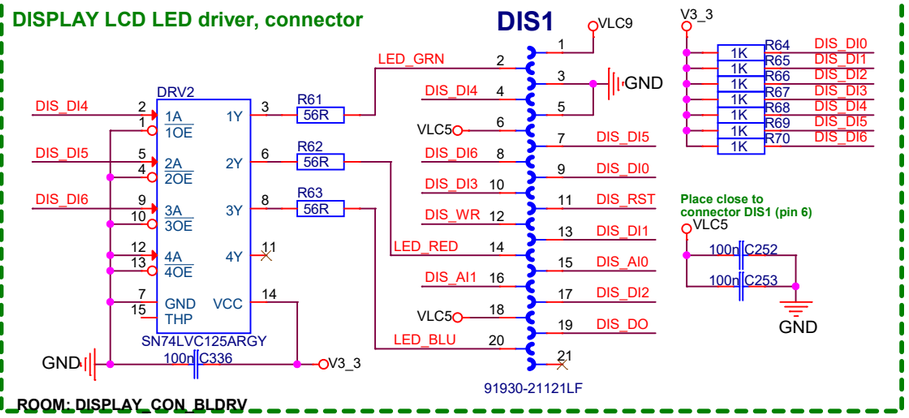
RST2 — **to LOG1D (pin AC7)**



Title: FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. B
		SHEET 6 OF 17	

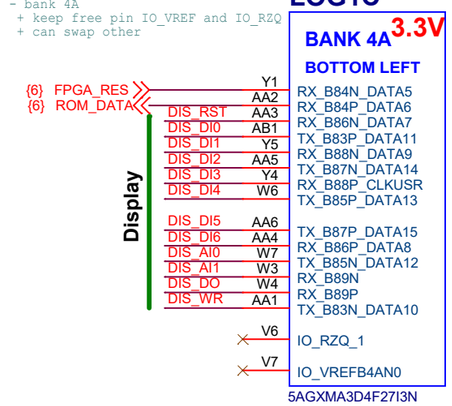
User interface - USB, Display, push buttons, HEX switch, LEDs

DISPLAY LCD LED driver, connector

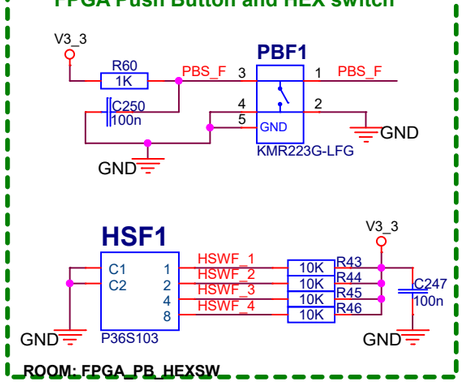


ROOM: DISPLAY_CON_BLDRV

LOG1C

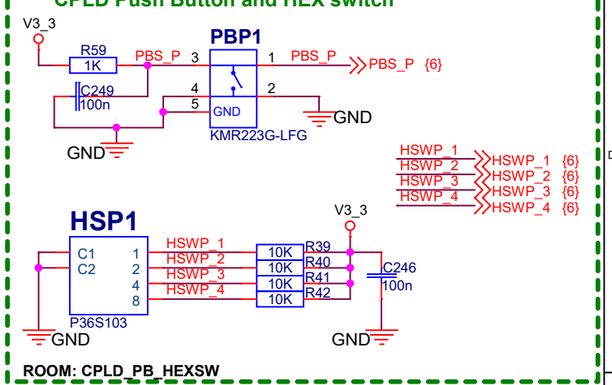


FPGA Push Button and HEX switch



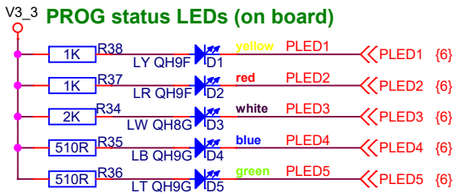
ROOM: FPGA_PB_HEXSW

CPLD Push Button and HEX switch



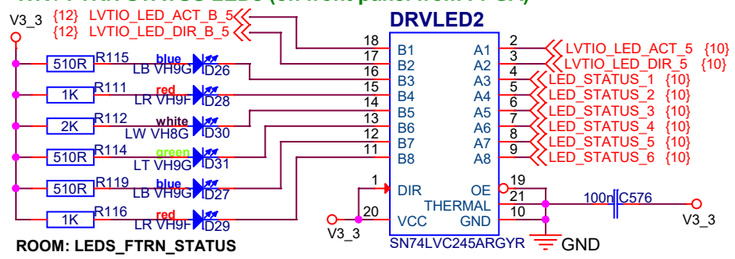
ROOM: CPLD_PB_HEXSW

PROG status LEDs (on board)



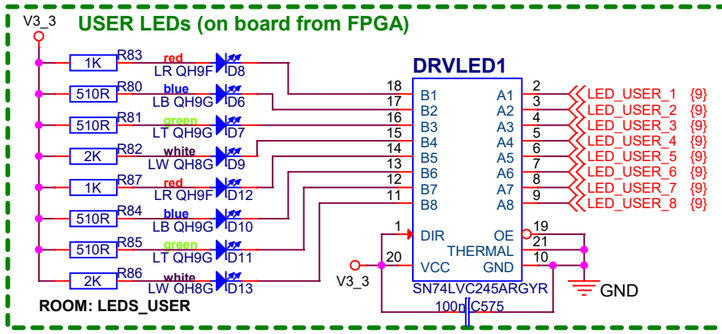
ROOM: LEDS_PROG_STATUS

WR / FTRN STATUS LEDs (on front panel from FPGA)



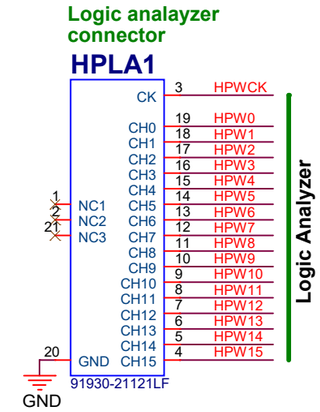
ROOM: LEDS_FTRN_STATUS

USER LEDs (on board from FPGA)

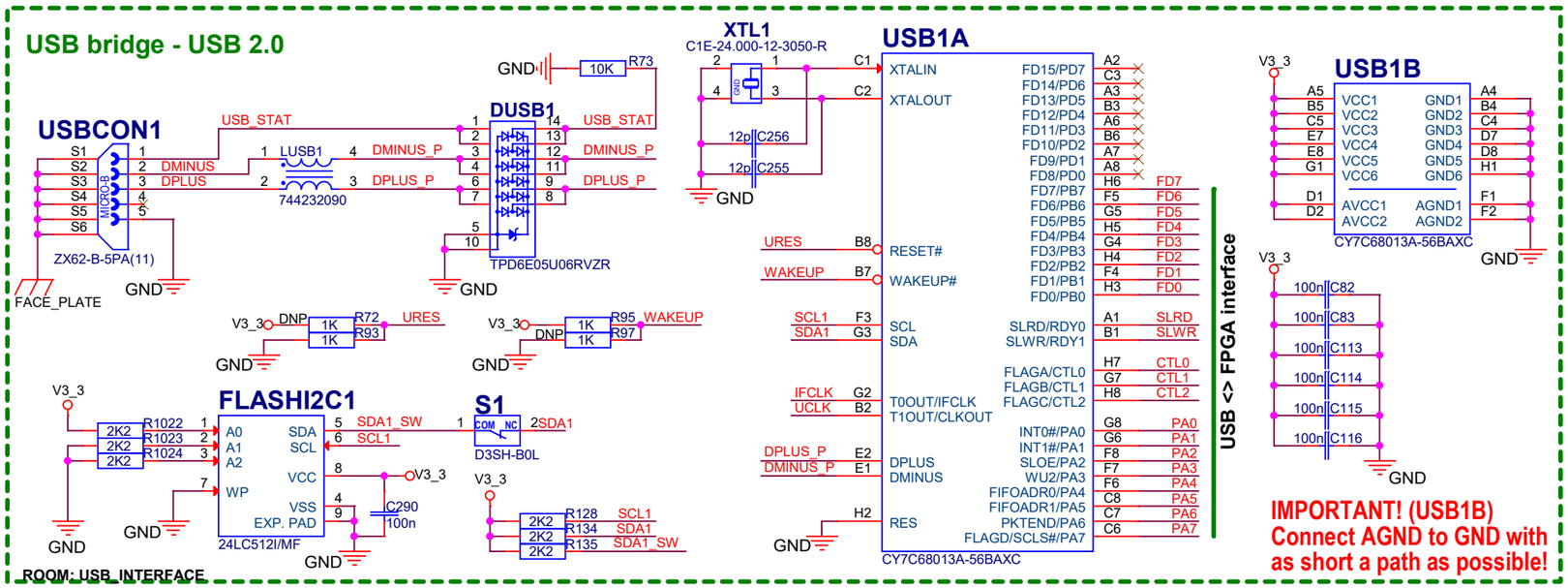


ROOM: LEDS_USER

Logic analayzer connector



USB bridge - USB 2.0

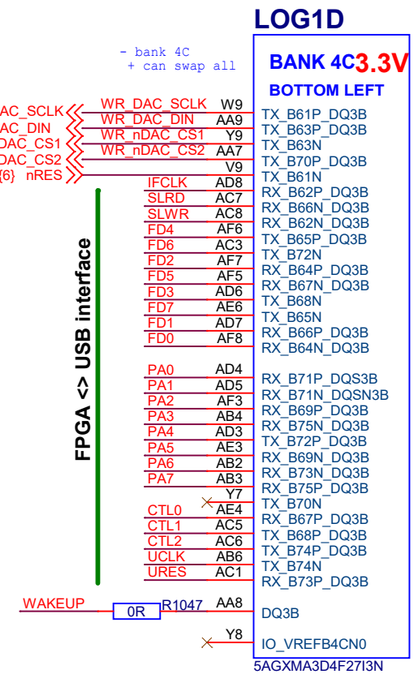


ROOM: USB_INTERFACE

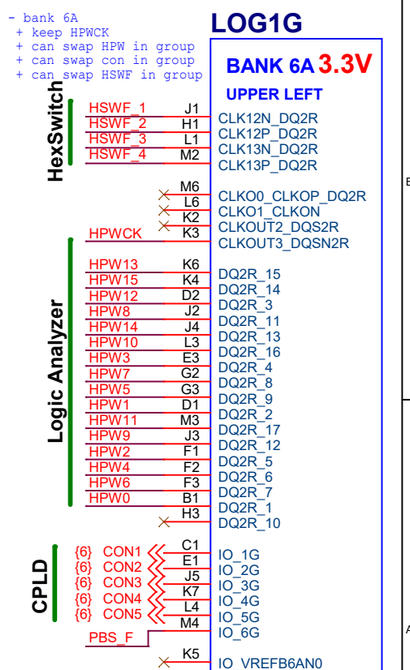
USB <> FPGA interface

IMPORTANT! (USB1B)
Connect AGND to GND with as short a path as possible!

LOG1D



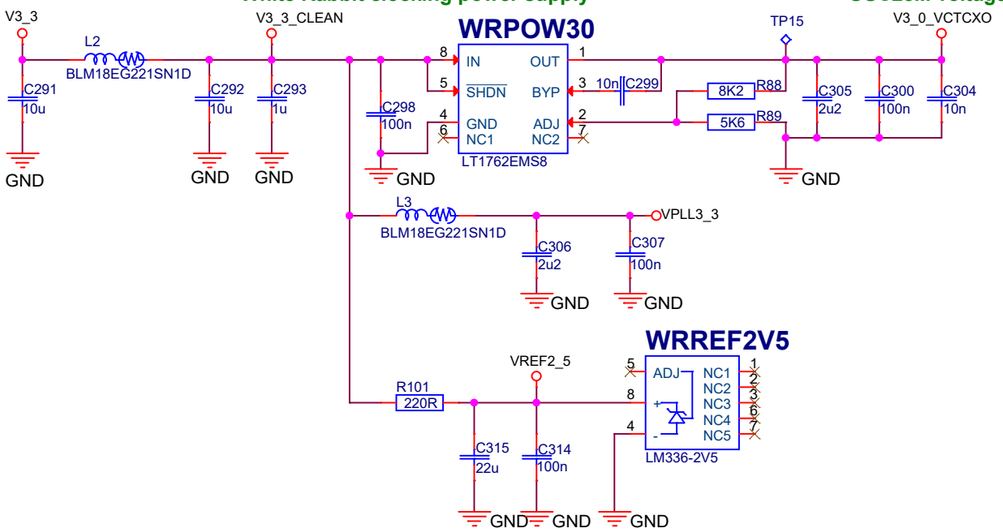
LOG1G



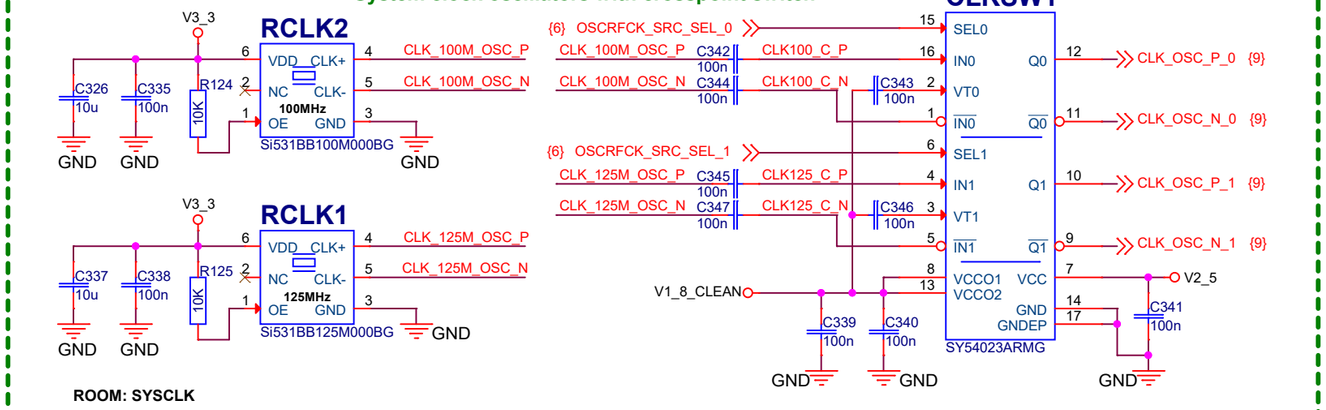
Title	User interface - USB, Display, push buttons, HEX switch, LEDs		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. B
		SHEET 7 OF 17	

Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch

White Rabbit clocking power supply

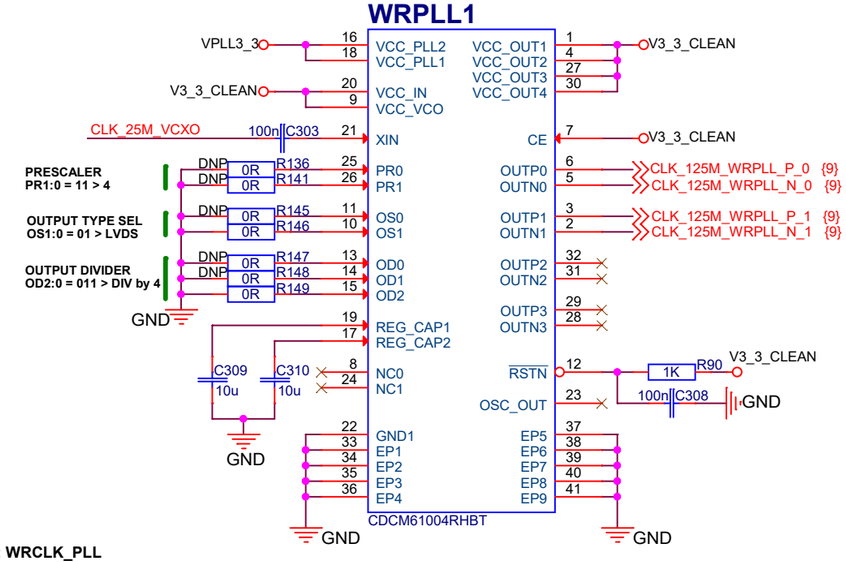


System clock oscillators with crosspoint switch

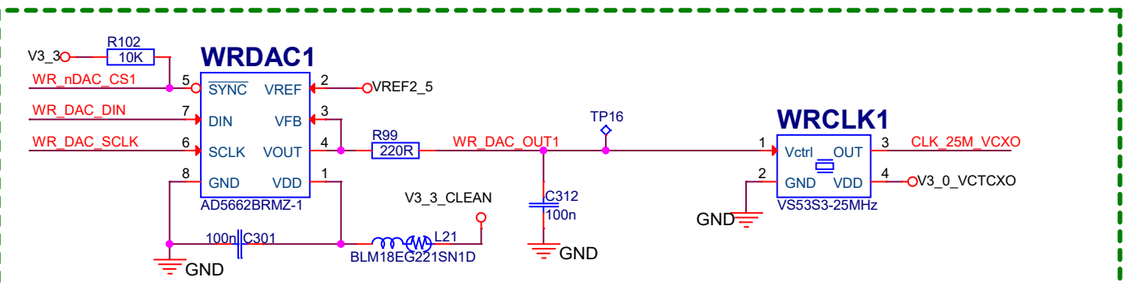


{7} WR_nDAC_CS1 >> WR_nDAC_CS1
{7} WR_nDAC_CS2 >> WR_nDAC_CS2
{7} WR_DAC_DIN >> WR_DAC_DIN
{7} WR_DAC_SCLK >> WR_DAC_SCLK

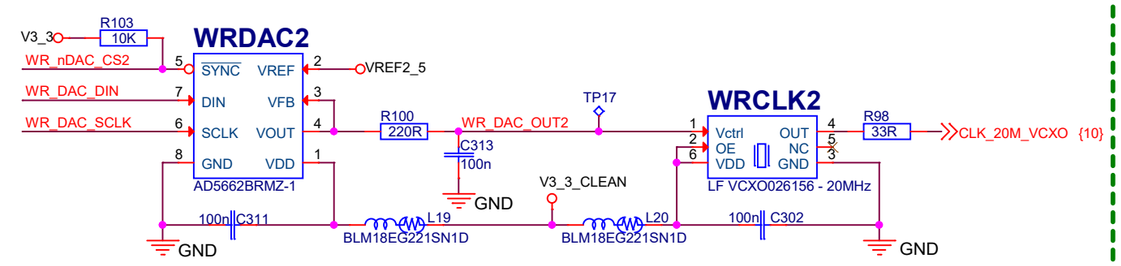
WRPLL1



WRDAC1



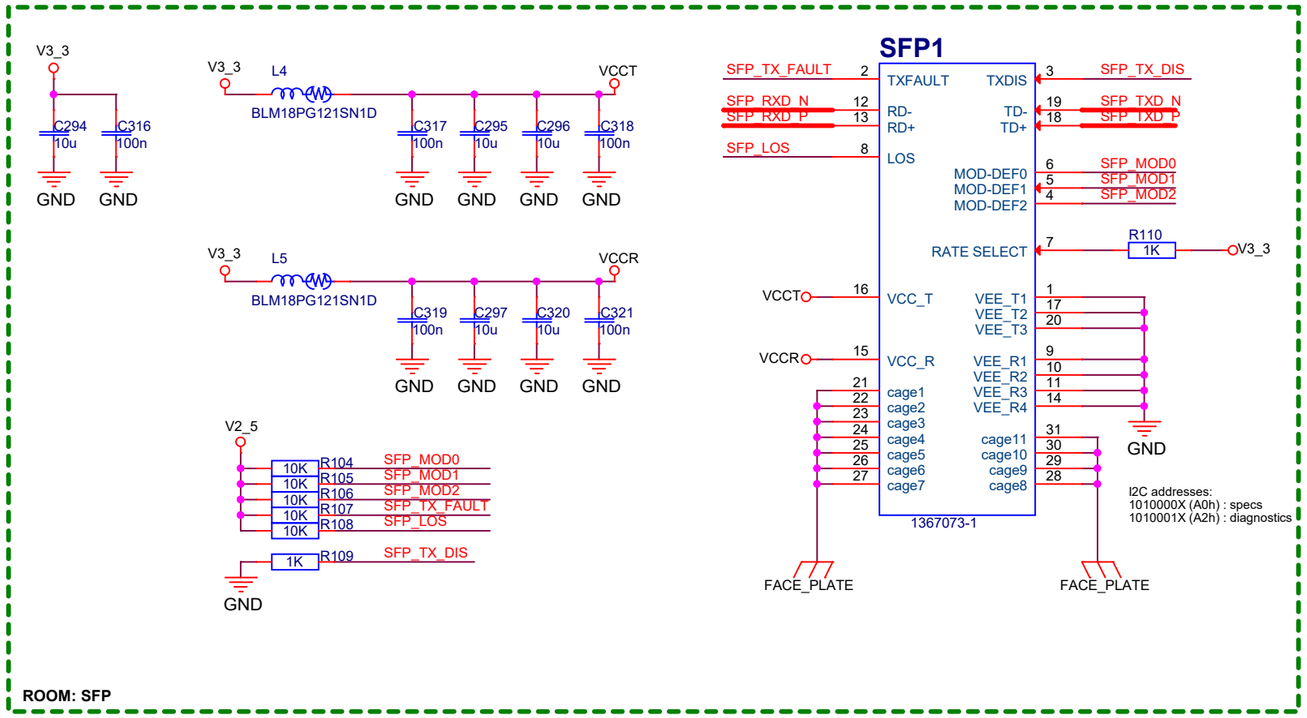
WRDAC2

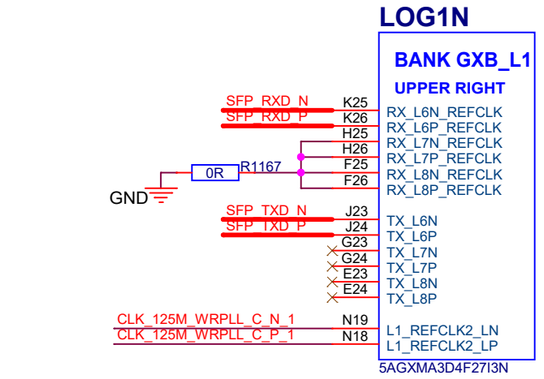


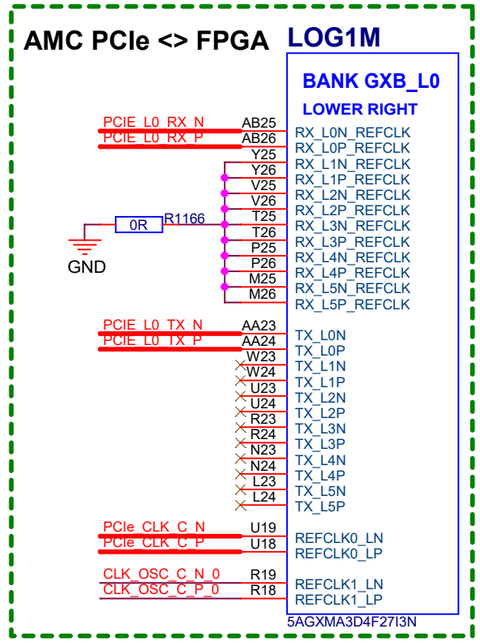
Title	Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. B
		SHEET 8 OF 17	

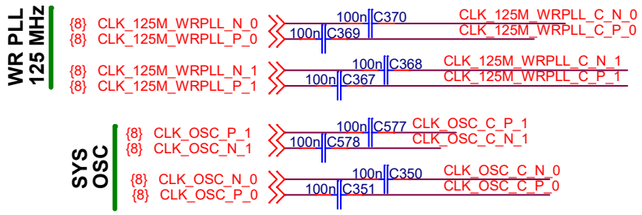
Fiber SFP, PCIe <> FPGA connections

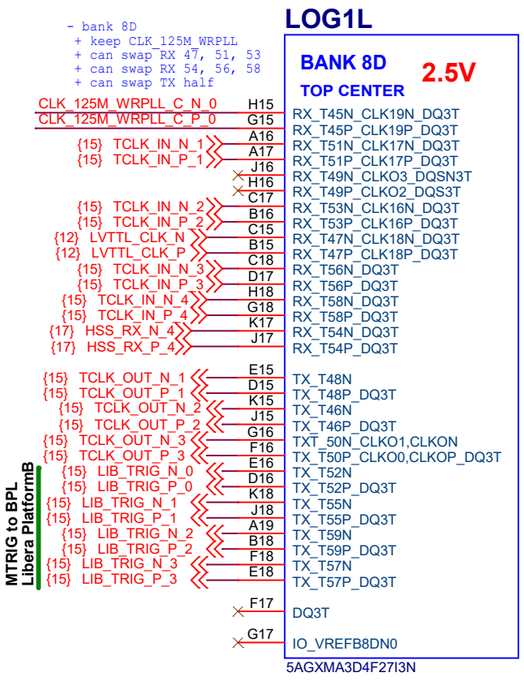
IMPORTANT!
Hi speed Gigabit lines
100R differential

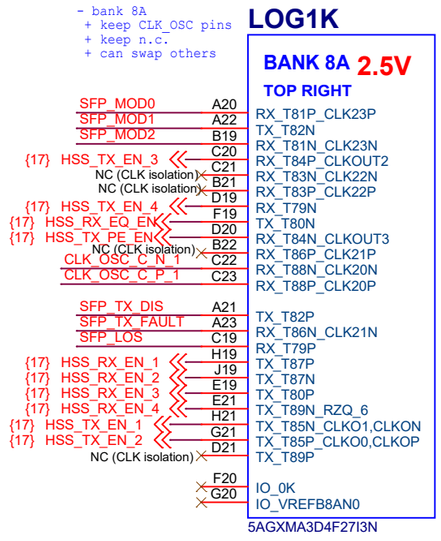


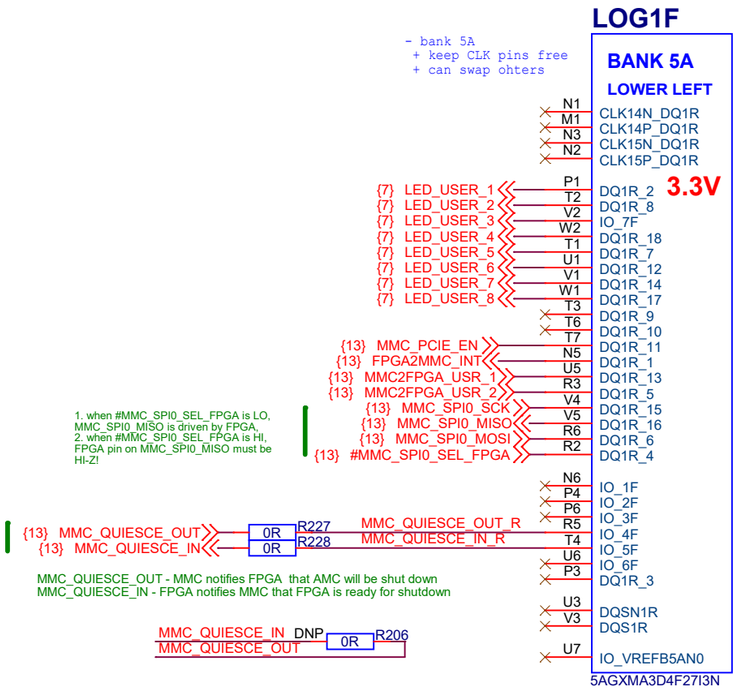






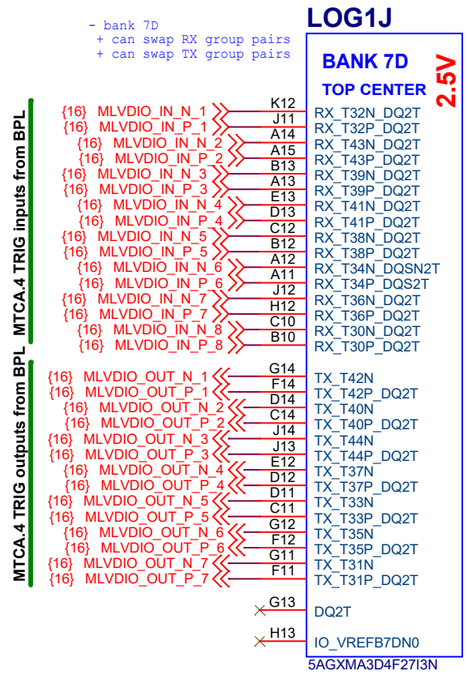






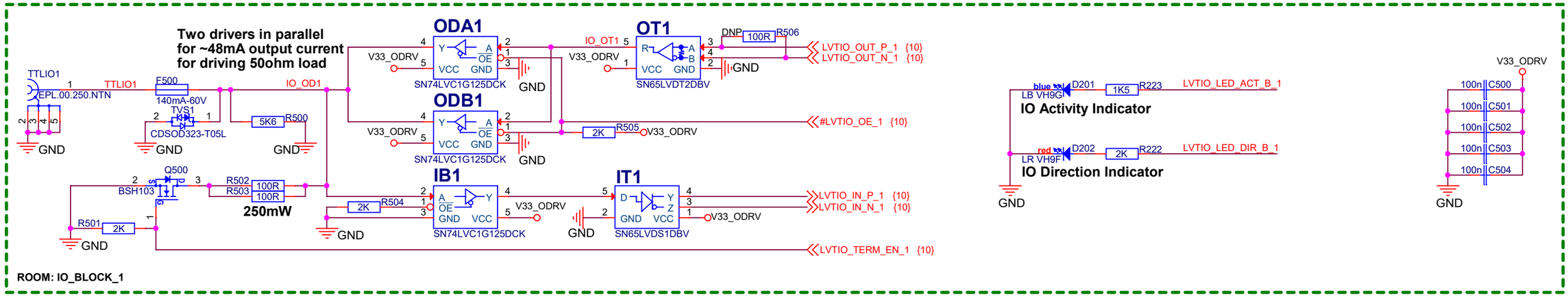
Title	Fiber SFP, PCIe <> FPGA connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. B
		SHEET 9 OF 17	

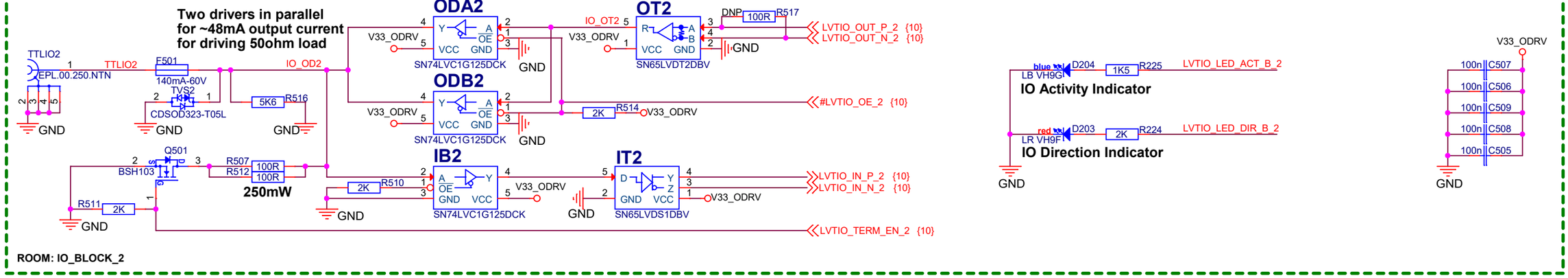
IO block power supply, FPGA <> IO block connections

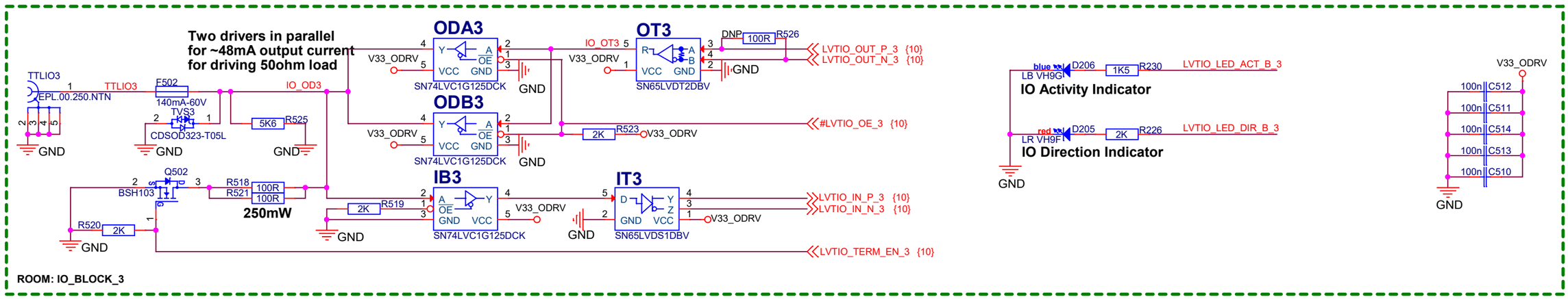


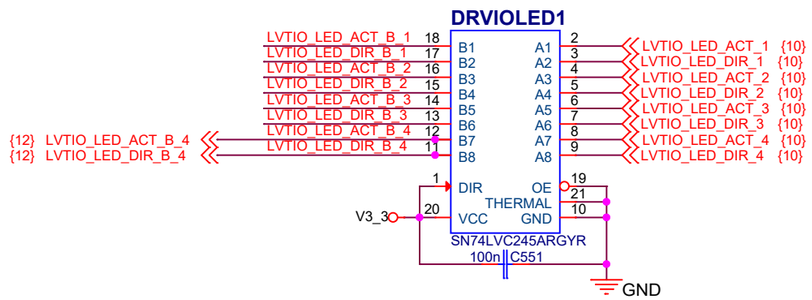
Title	IO block power supply, FPGA <> IO block connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 10 OF 17

LVTTL IO blocks 1-3



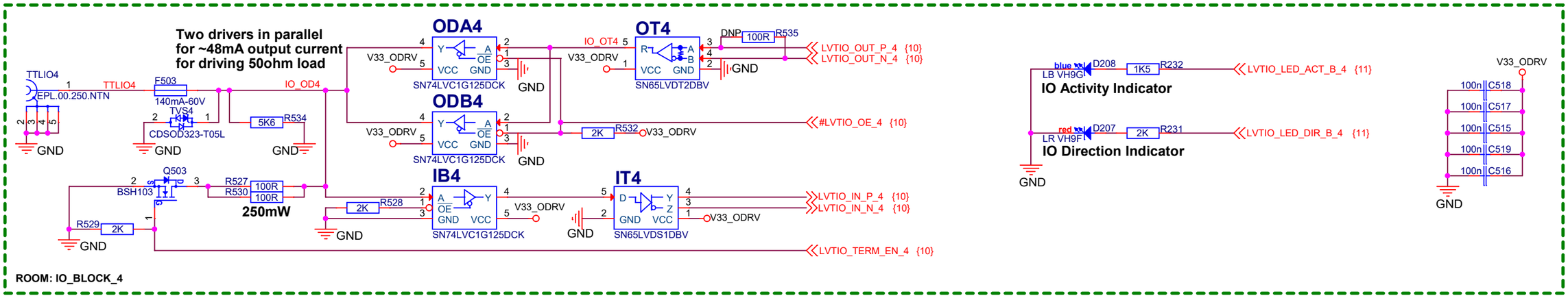


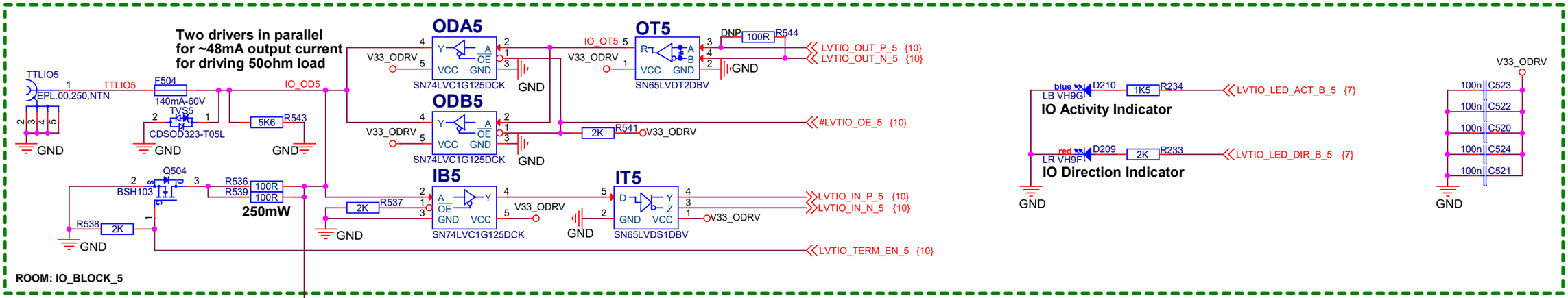


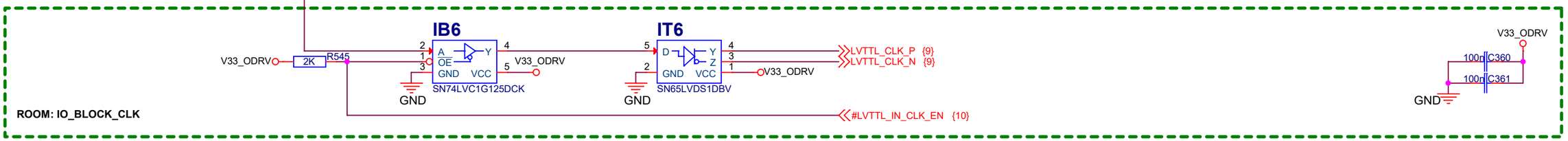


Title	LVTTL IO blocks 1-3		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 11 OF 17	

LVTTL IO blocks 4-5, IO CLOCK input







Title	LVTTL IO blocks 4-5, IO CLOCK input		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 12 OF 17

MMC, IPMI

MMC user push button

PBM1, PBM2 — KMR223G-LFG

#MMC_PB_2 used as MMC reset

ROOM: MMC_PBS_LEDS

MMC user LEDs

#MMC_ULED_1 — LT QH9G DU2

USB <> UART for MMC console (on the front panel if possible)

USBCON2 — ZX62-B-5PA(11) FACE_PLATE

DUSB2 — TPD6E05U06RVZR

IC1 — FT230XQ

IC4, IC5 — SN74LVC1G97DCK

ROOM: MMC_USB

PMX1

TPS2112APW

MP power MUX:
- in crate: V33_MP_BPL > 0.8V
  out = V33_MP_BPL
- not in crate, on AUX:
  V33_MP_BPL (0V) < 0.8V
  out = V3_3

MVREF1

LM336-2V5

MMEM1

M25P80-VMN6P

MMC FW FLASH

JTAG1 MMC JTAG connector

FTSH-105-01-F-DV-K

DTV2 — TPD6E05U06RVZR

MMC local I2C bus: - temp sensors, FRU EEPROM

TS1, TS2 — LM73CIMK-0

MMEM2 — 24LC512I/MF

ROOM: MMC_TEMP_FRUMEM

IC2

SN74LVC1G97DCK

Force #IPMI_MMC_ENABLE low when FTRN powered from AUX power (not in the crate). Use Push-button for MMC reset.

Option to not use #IPMI_MMC_ENABLE for MMC reset

2-Input AND Gate With One Inverted Input (IN2):
If (NOT #IPMI_MMC_EN) = H and #MMC_PB_2 = H
 #MMC_RESET_CMB = H
else
 #MMC_RESET_CMB = L (active)

MRST1

TPS3823-33DBVT

ROOM: MMC_RST_EN

Resistor dividers for voltage sensors

ROOM: MMC_VOLT_RED_DIV

MTCA Extractor handle switch

SW1 — HDT0001

ROOM: MMC_HANDLE

MMC1A

LPC2138FBD64/01

CLI and Debug UART

TX and RX signal naming is refering to the MMC side

power voltage sensing - analog inputs

Test pads for I2C bus sniffing

MMC1B

LPC2138FBD64/01

JTRST# only from backplane, JTAG connector does not provide JTRST#

AMC geographical address from backplane

MMC1C

LPC2138FBD64/01

XTL2 — C1E-24.000-12-3050-R

IPMI/AMC status LEDs on the front panel QH - top (red), VH - side (blue, green,white)

ROOM: MMC_IPMI_LEDS

TURN ON for main power regulators, 2 use cases:
- when in crate, by MMC_DCDC_EN
- when on AUX power, DCDC converters are turned on by default, MMC is overriden

enable outputs of payload power converters

monitor status of payload power converters

PGOOD signals from each power converter are joined but still isolated (wired AND function). This way each PGOOD can still have its own LED indicator.

Title	MMC, IPMI		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. B
		SHEET 13 OF 17	

AMC backplane plug

IMPORTANT!
Hi speed Gigabit lines
100R differential

JTAG signals length from the AMCPLG1 connector to the JDRVx buffers is 100mm MAX!!!

AMCPLG1

	1	GND28	GND56	170		
AMC_PWR8	2	PWR8	TDI	169	JTDI_AMC_PLG	
#PS1	3	PS1#	TDO	168	JTDO_AMC_PLG	
V33_MP_BPL	4	MP	TRST#	167	#JTRST_AMC_PLG	
{13} IPMI_GA_0	5	GA0	TMS	166	JTMS_AMC_PLG	
	6	ETH100R	TCLK	165	JTCK_AMC_PLG	
	7	GND27	GND55	164		
	8	ETH100T	TX20+	163		
AMC_PWR7	9	PWR7	TX20-	162	MLVDIO_BPL_P_8 {16}	
	10	GND26	GND54	161	MLVDIO_BPL_N_8 {16}	
	11	TX0+	RX20+	160		
	12	TX0-	RX20-	159	MLVDIO_BPL_P_7 {16}	
	13	GND25	GND53	158	MLVDIO_BPL_N_7 {16}	
	14	RX0+	TX19+	157		
	15	RX0-	TX19-	156	MLVDIO_BPL_P_6 {16}	
	16	GND24	GND52	155	MLVDIO_BPL_N_6 {16}	
{13} IPMI_GA_1	17	GA1	RX19+	154		
AMC_PWR6	18	PWR6	RX19-	153	MLVDIO_BPL_P_5 {16}	
	19	GND23	GND51	152	MLVDIO_BPL_N_5 {16}	
	20	TX1+	TX18+	151		
	21	TX1-	TX18-	150	MLVDIO_BPL_P_4 {16}	
	22	GND22	GND50	149	MLVDIO_BPL_N_4 {16}	
	23	RX1+	RX18+	148		
	24	RX1-	RX18-	147	MLVDIO_BPL_P_3 {16}	
	25	GND21	GND49	146	MLVDIO_BPL_N_3 {16}	
{13} IPMI_GA_2	26	GA2	TX17+	145		
AMC_PWR5	27	PWR5	TX17-	144	MLVDIO_BPL_P_2 {16}	
	28	GND20	GND48	143	MLVDIO_BPL_N_2 {16}	
	29	TX2+	RX17+	142		
	30	TX2-	RX17-	141	MLVDIO_BPL_P_1 {16}	
	31	GND19	GND47	140	MLVDIO_BPL_N_1 {16}	
	32	RX2+	TX16+	139		
	33	RX2-	TX16-	138	TCLK_BPL_P_3 {15}	
	34	GND18	GND46	137	TCLK_BPL_N_3 {15}	
	35	TX3+	RX16+	136		
	36	TX3-	RX16-	135	TCLK_BPL_P_4 {15}	
	37	GND17	GND45	134	TCLK_BPL_N_4 {15}	
	38	RX3+	TX15+	133		
	39	RX3-	TX15-	132	HSS_TX_BPL_P_4 {17}	
	40	GND16	GND44	131	HSS_TX_BPL_N_4 {17}	
{13} #IPMI_MMC_ENABLE	41	ENABLE#	RX15+	130		
AMC_PWR4	42	PWR4	RX15-	129	HSS_RX_BPL_P_4 {17}	
	43	GND15	GND43	128	HSS_RX_BPL_N_4 {17}	
{9} PCIE_L0_TX_C_P	44	TX4+	TX14+	127		
{9} PCIE_L0_TX_C_N	45	TX4-	TX14-	126	HSS_TX_BPL_P_3 {17}	
	46	GND14	GND42	125	HSS_TX_BPL_N_3 {17}	
{9} PCIE_L0_RX_C_P	47	RX4+	RX14+	124		
{9} PCIE_L0_RX_C_N	48	RX4-	RX14-	123	HSS_RX_BPL_P_3 {17}	
	49	GND13	GND41	122	HSS_RX_BPL_N_3 {17}	
	50	TX5+	TX13+	121		
	51	TX5-	TX13-	120	HSS_TX_BPL_P_2 {17}	
	52	GND12	GND40	119	HSS_TX_BPL_N_2 {17}	
	53	RX5+	RX13+	118		
	54	RX5-	RX13-	117	HSS_RX_BPL_P_2 {17}	
	55	GND11	GND39	116	HSS_RX_BPL_N_2 {17}	
{13} IPMB_L_SCL	56	SCL_L	TX12+	115		
AMC_PWR3	57	PWR3	TX12-	114	HSS_TX_BPL_P_1 {17}	
	58	GND10	GND38	113	HSS_TX_BPL_N_1 {17}	
{15} M2_TRIG_P_0	59	TX6+	RX12+	112		
{15} M2_TRIG_N_0	60	TX6-	RX12-	111	HSS_RX_BPL_P_1 {17}	
	61	GND9	GND37	110	HSS_RX_BPL_N_1 {17}	
{15} M2_TRIG_P_1	62	RX6+	TX11+	109		
{15} M2_TRIG_N_1	63	RX6-	TX11-	108		
	64	GND8	GND36	107		
{15} M2_TRIG_P_2	65	TX7+	RX11+	106		
{15} M2_TRIG_N_2	66	TX7-	RX11-	105		
	67	GND7	GND35	104		
{15} M2_TRIG_P_3	68	RX7+	TX10+	103		
{15} M2_TRIG_N_3	69	RX7-	TX10-	102		
	70	GND6	GND34	101		
{13} IPMB_L_SDA	71	SDA_L	RX10+	100		
AMC_PWR2	72	PWR2	RX10-	99		
	73	GND5	GND33	98		
{15} TCLK_BPL_P_1	74	CLK1+	TX9+	97		
{15} TCLK_BPL_N_1	75	CLK1-	TX9-	96		
	76	GND4	GND32	95		
{15} TCLK_BPL_P_2	77	CLK2+	RX9+	94		
{15} TCLK_BPL_N_2	78	CLK2-	RX9-	93		
	79	GND3	GND31	92		
{9} PCIE_CLK_P	80	CLK3+	TX8+	91		
{9} PCIE_CLK_N	81	CLK3-	TX8-	90		
	82	GND2	GND30	89		
#PS0	83	PS0#	RX8+	88		
AMC_PWR1	84	PWR1	RX8-	87		
	85	GND1	GND29	86		

GND PCB_AMC_PLUG GND

AMC backplane plug is implemented on PCB!

MTCA.4 bidirectional triggers, gates (DC-coupled, transceivers with 3-State outputs)

MTCA.4 bidir low jitter clocks TCLKC, TCLKD (AC-coupled, 3-state outputs)

MTCA.4 trasnceivers (AC-coupled, buffers with 3-State outputs)

Libera Module 2 TRIGGERS (DC-coupled, 3-state outputs)

MTCA.4 bidir low jitter clocks TCLKA, TCLKB (AC-coupled, 3-state outputs)

V33_MP — 10K R1124 — DIP1 (MCEMR-02-T) — JTAGSW_SEL — JTAGSW_SEL {6,13} / MMC_I2C_SDA {13} — 33R R121 — GND

Pull-Down option for MMC pin P0.14 to put MMC in bootloader mode

V12_HOST

BLM18PG221SN1D	L8	AMC_PWR1
BLM18PG221SN1D	L9	AMC_PWR2
BLM18PG221SN1D	L10	AMC_PWR3
BLM18PG221SN1D	L11	AMC_PWR4
BLM18PG221SN1D	L12	AMC_PWR5
BLM18PG221SN1D	L13	AMC_PWR6
BLM18PG221SN1D	L14	AMC_PWR7
BLM18PG221SN1D	L15	AMC_PWR8

V33_MP_BPL — **Management Power from MTCA backplane** — DNP C376 10u — DNP C377 100n — GND

#PS1 — DSH2 — CMDSH2-3 — #PS0

AMC card presence detection. PS1 "shorted" to PS0 when card fully inserted into host.

AMCESD1

ESD discharge strip — BACKPLANE — SEG1 — 10M R182 — SEG2 — 10M R181 — GND — SEG3 — FACEPLATE — FACE_PLATE

J1

1 — S1731-46R — 2 — FACE_PLATE — GND

V33_MP — R1227 1K — red D211 LR VH9F — Q505 BSH103 (D, G, S) — JTAGSW_SEL — GND

Place LED on front panel!

JTDO_AMC_PLG — R1168 33R — JDRV1 (SN74LVC1G125DCK, 100n C391, V33_MP, GND) — JTDO_AMC

JDRV2 (SN74LVC125ARGY, 100n C388, GND, V33_MP)

JTDI_AMC_PLG	1A	1Y — JTDI_AMC
	1OE	
#JTRST_AMC_PLG	2A	2Y — #JTRST_AMC
	2OE	
JTMS_AMC_PLG	3A	3Y — JTMS_AMC
	3OE	
JTCK_AMC_PLG	4A	4Y — JTCK_AMC
	4OE	
	Thermal	
	GND	VCC — V33_MP

V33_MP — 10K R113 JTDI_AMC_PLG — 10K R118 JTMS_AMC_PLG — 10K R117 JTCK_AMC_PLG — 10K R120 #JTRST_AMC_PLG — GND

JTAG swithc for routing Backplane JTAG to MMC or CPLD/FPGA. Monitored by MMC.

JSW1 (MAX4948ETG+, GND1, GND2, Thermal, N.C., VCC, GND, 100n C251, V33_MP)

GND	23	6COM	6NO 24 — GND
			6NC 1
#JTRST_AMC	3	5COM	5NO 2 — #JTRST_MMC {13}
			5NC 4
JTCK_AMC	7	4COM	4NO 8 — JTCK_SR {6}
			4NC 9 — JTCK_MMC {13}
JTMS_AMC	11	3COM	3NO 10 — JTMS_SR {6}
			3NC 12 — JTMS_MMC {13}
JTDI_AMC	16	2COM	2NO 17 — JTDI_SR {6}
			2NC 15 — JTDI_MMC {13}
JTDO_AMC	20	1COM	1NO 19 — JTDO_RS {6}
			1NC 18 — JTDO_MMC {13}
{4,13} PRESENT_V12AUX	5	EN	CB 14 — JTAGSW_SEL

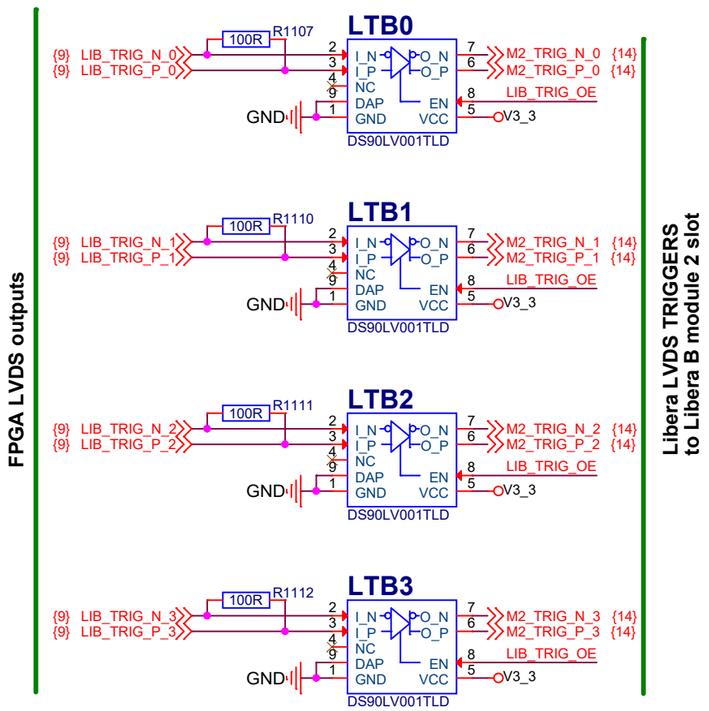
JTAG from BACKPLANE

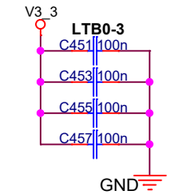
JTAG to MMC/FPGA-CPLD

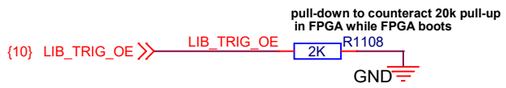
CB = L : BPL > MMC
CB = H : BPL > CPLD/FPGA

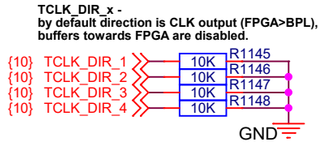
Title: AMC backplane plug			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. B
			SHEET 14 OF 17

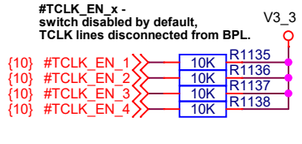
Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers

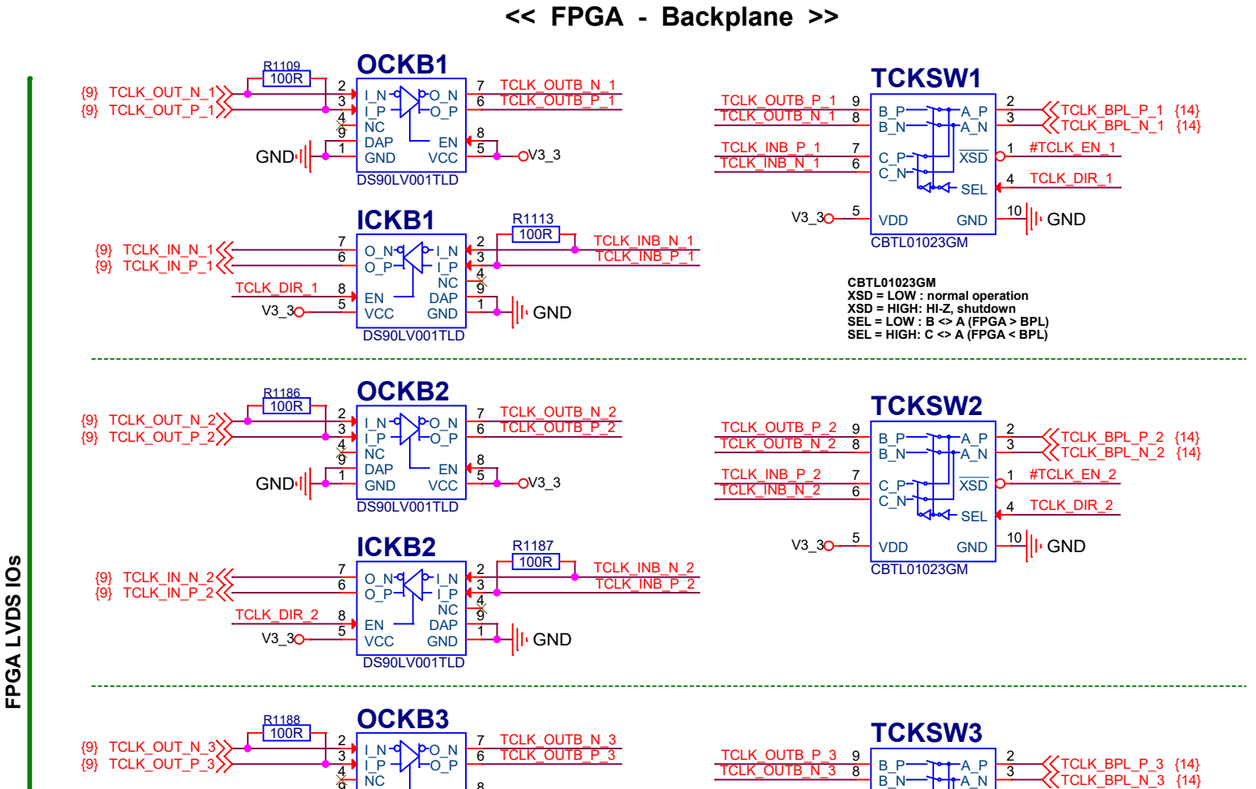


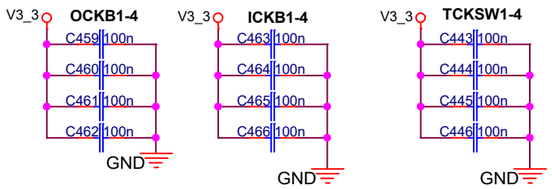












Title: Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. B
			SHEET 15 OF 17

Backplane buffers - MTCA.4 PORT 17-20 (M-LVDS triggers, clocks, gates)

Pull-down to counteract 20k pull-up in FPGA while FPGA boots.
This keeps MLVDS buffers powered down until FPGA gets in USER MODE.

{10} #MLVDIO_PDN — #MLVDIO_PDN — 2K — R359 — GND
{10} MLVDIO_FSEN — MLVDIO_FSEN

FPGA LVDS IOs

OTB1
{10} MLVDIO_OUT_P_1 (3), {10} MLVDIO_OUT_N_1 (4) → A, B; R (2); GND, VCC (1) → V3_3
5 → MLVDIO_OUT_1
SN65LVDT2DBV

OTB2
{10} MLVDIO_OUT_P_2 (3), {10} MLVDIO_OUT_N_2 (4) → A, B; R (2); GND, VCC (1) → V3_3
5 → MLVDIO_OUT_2
SN65LVDT2DBV

OTB3
{10} MLVDIO_OUT_P_3 (3), {10} MLVDIO_OUT_N_3 (4) → A, B; R (2); GND, VCC (1) → V3_3
5 → MLVDIO_OUT_3
SN65LVDT2DBV

OTB4
{10} MLVDIO_OUT_P_4 (3), {10} MLVDIO_OUT_N_4 (4) → A, B; R (2); GND, VCC (1) → V3_3
5 → MLVDIO_OUT_4
SN65LVDT2DBV

OTB5
{10} MLVDIO_OUT_P_5 (3), {10} MLVDIO_OUT_N_5 (4) → A, B; R (2); GND, VCC (1) → V3_3
5 → MLVDIO_OUT_5
SN65LVDT2DBV

OTB6
{10} MLVDIO_OUT_P_6 (3), {10} MLVDIO_OUT_N_6 (4) → A, B; R (2); GND, VCC (1) → V3_3
5 → MLVDIO_OUT_6
SN65LVDT2DBV

OTB7
{10} MLVDIO_OUT_P_7 (3), {10} MLVDIO_OUT_N_7 (4) → A, B; R (2); GND, VCC (1) → V3_3
5 → MLVDIO_OUT_7
SN65LVDT2DBV

OTB8
{10} MLVDIO_OUT_P_8 (3), {10} MLVDIO_OUT_N_8 (4) → A, B; R (2); GND, VCC (1) → V3_3
5 → MLVDIO_OUT_8
SN65LVDT2DBV

ITB1
{10} MLVDIO_IN_P_1 (4), {10} MLVDIO_IN_N_1 (3) → Y, Z; D (5); VCC, GND (2) → GND
V3_3 → MLVDIO_IN_1
SN65LVDS1DBV

ITB2
{10} MLVDIO_IN_P_2 (4), {10} MLVDIO_IN_N_2 (3) → Y, Z; D (5); VCC, GND (2) → GND
V3_3 → MLVDIO_IN_2
SN65LVDS1DBV

ITB3
{10} MLVDIO_IN_P_3 (4), {10} MLVDIO_IN_N_3 (3) → Y, Z; D (5); VCC, GND (2) → GND
V3_3 → MLVDIO_IN_3
SN65LVDS1DBV

ITB4
{10} MLVDIO_IN_P_4 (4), {10} MLVDIO_IN_N_4 (3) → Y, Z; D (5); VCC, GND (2) → GND
V3_3 → MLVDIO_IN_4
SN65LVDS1DBV

ITB5
{10} MLVDIO_IN_P_5 (4), {10} MLVDIO_IN_N_5 (3) → Y, Z; D (5); VCC, GND (2) → GND
V3_3 → MLVDIO_IN_5
SN65LVDS1DBV

ITB6
{10} MLVDIO_IN_P_6 (4), {10} MLVDIO_IN_N_6 (3) → Y, Z; D (5); VCC, GND (2) → GND
V3_3 → MLVDIO_IN_6
SN65LVDS1DBV

ITB7
{10} MLVDIO_IN_P_7 (4), {10} MLVDIO_IN_N_7 (3) → Y, Z; D (5); VCC, GND (2) → GND
V3_3 → MLVDIO_IN_7
SN65LVDS1DBV

ITB8
{10} MLVDIO_IN_P_8 (4), {10} MLVDIO_IN_N_8 (3) → Y, Z; D (5); VCC, GND (2) → GND
V3_3 → MLVDIO_IN_8
SN65LVDS1DBV

<< FPGA - Backplane >>

MTB1A
{10} MLVDIO_DE_4 (1) → MLVDIO_OUT_4 (35) → 1DE, 1D; 1A, 1B → 47 MLVDIO_BPL_P_4 {14}, 48 MLVDIO_BPL_N_4 {14}
MLVDIO_FSEN (39) → MLVDIO_IN_4 (36) → 1FSEN, 1R, 1RE (40) ← {10} #MLVDIO_RE_4
{10} MLVDIO_DE_3 (5) → MLVDIO_OUT_3 (32) → 2DE, 2D; 2A, 2B → 3 MLVDIO_BPL_P_3 {14}, 4 MLVDIO_BPL_N_3 {14}
MLVDIO_FSEN (41) → MLVDIO_IN_3 (33) → 2FSEN, 2R, 2RE (42) ← {10} #MLVDIO_RE_3
{10} MLVDIO_DE_2 (8) → MLVDIO_OUT_2 (28) → 3DE, 3D; 3A, 3B → 9 MLVDIO_BPL_P_2 {14}, 10 MLVDIO_BPL_N_2 {14}
MLVDIO_FSEN (20) → MLVDIO_IN_2 (29) → 3FSEN, 3R, 3RE (19) ← {10} #MLVDIO_RE_2
{10} MLVDIO_DE_1 (12) → MLVDIO_OUT_1 (25) → 4DE, 4D; 4A, 4B → 13 MLVDIO_BPL_P_1 {14}, 14 MLVDIO_BPL_N_1 {14}
MLVDIO_FSEN (22) → MLVDIO_IN_1 (26) → 4FSEN, 4R, 4RE (21) ← {10} #MLVDIO_RE_1
PDN (30) ← #MLVDIO_PDN
SN65MLVD040RGZ

MTB2A
{10} MLVDIO_DE_8 (1) → MLVDIO_OUT_8 (35) → 1DE, 1D; 1A, 1B → 47 MLVDIO_BPL_P_8 {14}, 48 MLVDIO_BPL_N_8 {14}
MLVDIO_FSEN (39) → MLVDIO_IN_8 (36) → 1FSEN, 1R, 1RE (40) ← {10} #MLVDIO_RE_8
{10} MLVDIO_DE_7 (5) → MLVDIO_OUT_7 (32) → 2DE, 2D; 2A, 2B → 3 MLVDIO_BPL_P_7 {14}, 4 MLVDIO_BPL_N_7 {14}
MLVDIO_FSEN (41) → MLVDIO_IN_7 (33) → 2FSEN, 2R, 2RE (42) ← {10} #MLVDIO_RE_7
{10} MLVDIO_DE_6 (8) → MLVDIO_OUT_6 (28) → 3DE, 3D; 3A, 3B → 9 MLVDIO_BPL_P_6 {14}, 10 MLVDIO_BPL_N_6 {14}
MLVDIO_FSEN (20) → MLVDIO_IN_6 (29) → 3FSEN, 3R, 3RE (19) ← {10} #MLVDIO_RE_6
{10} MLVDIO_DE_5 (12) → MLVDIO_OUT_5 (25) → 4DE, 4D; 4A, 4B → 13 MLVDIO_BPL_P_5 {14}, 14 MLVDIO_BPL_N_5 {14}
MLVDIO_FSEN (22) → MLVDIO_IN_5 (26) → 4FSEN, 4R, 4RE (21) ← {10} #MLVDIO_RE_5
PDN (30) ← #MLVDIO_PDN
SN65MLVD040RGZ

MTCA.4 M-LVDS TRIGGERS, GATES (PORT 17-20)

/RE and FSEN pins have internal pull-UP resistors.
DE and /PDN pin has internal pull-DOWN resistors.

MLVDIO_IN_1 — 10K — R1153
MLVDIO_IN_2 — 10K — R1154
MLVDIO_IN_3 — 10K — R1155
MLVDIO_IN_4 — 10K — R1156
MLVDIO_IN_5 — 10K — R1157
MLVDIO_IN_6 — 10K — R1158
MLVDIO_IN_7 — 10K — R1159
MLVDIO_IN_8 — 10K — R1160
GND

Define state when /RE is HI.

MTB1B
THP, 1GND, 2GND, 3GND, 4GND, 5GND, 6GND, 7GND, 8GND (49, 6, 7, 18, 23, 27, 31, 34, 38, 43) → GND
2NC, 1NC (44, 17)
1VCC, 2VCC, 3VCC, 4VCC, 5VCC, 6VCC, 7VCC, 8VCC (2, 11, 15, 16, 24, 37, 45, 46) → V3_3
C389 100n, C413 100n, C414 100n, C415 100n, C416 100n, C417 100n, C418 100n, C419 100n → GND
SN65MLVD040RGZ

MTB2B
THP, 1GND, 2GND, 3GND, 4GND, 5GND, 6GND, 7GND, 8GND (49, 6, 7, 18, 23, 27, 31, 34, 38, 43) → GND
2NC, 1NC (44, 17)
1VCC, 2VCC, 3VCC, 4VCC, 5VCC, 6VCC, 7VCC, 8VCC (2, 11, 15, 16, 24, 37, 45, 46) → V3_3
C390 100n, C420 100n, C421 100n, C422 100n, C423 100n, C424 100n, C425 100n, C426 100n → GND
SN65MLVD040RGZ

OTB1-8
V3_3 → C431 100n, C432 100n, C433 100n, C434 100n, C427 100n, C428 100n, C429 100n, C430 100n → GND

ITB1-8
V3_3 → C435 100n, C436 100n, C437 100n, C438 100n, C439 100n, C440 100n, C441 100n, C442 100n → GND

Title	Backplane buffers - MTCA.4 PORT 17-20 (M-LVDS triggers, clocks, gates)		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. B
			SHEET 16 OF 17

Backplane buffers - MTCA.4 PORT 12-15 (High Speed Serial)

{9} HSS_RX_EQ_EN → HSS_RX_EQ_EN
{9} HSS_TX_PE_EN → HSS_TX_PE_EN

FPGA BANK GXB L0, Gigabit Transceivers

<< FPGA - Backplane >>

MTCA.4 backplane PORTs 12-15,

BXT1

DS25CP102TSQ

{10} HSS_TX_P_2	IN0_P	OUT0_P	HSS_TX_BPL_P_2 {14} (C469 100n)
{10} HSS_TX_N_2	IN0_N	OUT0_N	HSS_TX_BPL_N_2 {14} (C470 100n)
{10} HSS_TX_P_1	IN1_P	OUT1_P	HSS_TX_BPL_P_1 {14} (C467 100n)
{10} HSS_TX_N_1	IN1_N	OUT1_N	HSS_TX_BPL_N_1 {14} (C468 100n)
	EQ	EN0	HSS_TX_EN_1
	SEL0	EN1	HSS_TX_EN_2
V3_3	SEL1	PE	HSS_TX_PE_EN
GND	GND	VCC	V3_3
GND	GNDDAP		

BXT2

DS25CP102TSQ

{10} HSS_TX_P_4	IN0_P	OUT0_P	HSS_TX_BPL_P_4 {14} (C489 100n)
{10} HSS_TX_N_4	IN0_N	OUT0_N	HSS_TX_BPL_N_4 {14} (C492 100n)
{10} HSS_TX_P_3	IN1_P	OUT1_P	HSS_TX_BPL_P_3 {14} (C487 100n)
{10} HSS_TX_N_3	IN1_N	OUT1_N	HSS_TX_BPL_N_3 {14} (C488 100n)
	EQ	EN0	HSS_TX_EN_3
	SEL0	EN1	HSS_TX_EN_4
V3_3	SEL1	PE	HSS_TX_PE_EN
GND	GND	VCC	V3_3
GND	GNDDAP		

BXR1

DS25CP102TSQ

{10} HSS_RX_P_2	OUT0_P	IN0_P	HSS_RX_BPL_P_2 {14} (C477 100n)
{10} HSS_RX_N_2	OUT0_N	IN0_N	HSS_RX_BPL_N_2 {14} (C478 100n)
{10} HSS_RX_P_1	OUT1_P	IN1_P	HSS_RX_BPL_P_1 {14} (C475 100n)
{10} HSS_RX_N_1	OUT1_N	IN1_N	HSS_RX_BPL_N_1 {14} (C476 100n)
{9} HSS_RX_EN_1	EN0	EQ	HSS_RX_EQ_EN
{9} HSS_RX_EN_2	EN1	SEL0	
	PE	SEL1	V3_3
V3_3	VCC	GND	GND
		GNDDAP	

BXR2

DS25CP102TSQ

{9} HSS_RX_P_4	OUT0_P	IN0_P	HSS_RX_BPL_P_4 {14} (C495 100n)
{9} HSS_RX_N_4	OUT0_N	IN0_N	HSS_RX_BPL_N_4 {14} (C496 100n)
{10} HSS_RX_P_3	OUT1_P	IN1_P	HSS_RX_BPL_P_3 {14} (C493 100n)
{10} HSS_RX_N_3	OUT1_N	IN1_N	HSS_RX_BPL_N_3 {14} (C494 100n)
{9} HSS_RX_EN_3	EN0	EQ	HSS_RX_EQ_EN
{9} HSS_RX_EN_4	EN1	SEL0	
	PE	SEL1	V3_3
V3_3	VCC	GND	GND
		GNDDAP	

PE - Transmit Pre-Emphasis select pin. There is a 20k pulldown resistor on this pin
EQ - Receive Equalization select pin. There is a 20k pulldown resistor on this pin.
SEL0, SEL1 - Switch configuration pins. There is a 20k pulldown resistor on this pin.

V3_3 — C526 100n, C527 100n, C528 100n, C529 100n — GND

{9} HSS_TX_EN_1	HSS_TX_EN_1	2K	R360
{9} HSS_TX_EN_2	HSS_TX_EN_2	2K	R361
{9} HSS_TX_EN_3	HSS_TX_EN_3	2K	R362
{9} HSS_TX_EN_4	HSS_TX_EN_4	2K	R363

GND

pull-down to counteract 20k pull-up in FPGA while FPGA boots

Title	Backplane buffers - MTCA.4 PORT 12-15 (High Speed Serial)		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. B
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