FAIR Timing Receiver AMC form factor - CSL_FTRN_AMC

Single width, mid-height

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DATE	REVISION DESCRIPTION	DRAWN	REV
01.09.2014	Initial version	dslavinec	A
19.09.2014	Flattened IO blocks	dslavinec	A
02.12.2014	Updates after QA review	dslavinec	A
16.04.2015	Added ADC clock generation and trigger signals to backplane, moved LVTTL_CLK, nRES and FPGA_RES to different FPGA pins	dslavinec	A
23.07.2015	removed ADC clocking page, only one set of triggers to backplane kept, incorporated changes from PMC (LED driving), added power mux for MMC	dslavinec	A
17.08.2015	added sheet 15 with MTCA.4 triggers and clocks to/from backplane	dslavinec	A
01.10.2015	MTCA.4 out clocks not connected to clk outputs, backplane buffers enable signals connected only to FPGA	dslavinec	A
27.11.2015	MTCA.4 connections to backplane finished, MMC PGOOD modified, relevant updates from PMC, MMC reset modified	dslavinec	A
09.12.2015	MTCA.4 HSS connections (backplane ports 12-15) moved from FPGA GXB banks to LVDS IOs	dslavinec	A
16.12.2015	libera triggers, MTCA.4 tclk and mlvdios moved to top FPGA banks	dslavinec	A

Value	Capatitors used
12p	0402, 50V, C0G, 1%
22p	0402, 50V, C0G, 1%
10n	0402, 25V, X7R, 10%
100n	0402, 25V, X7R, 10%
1u	0603, 16V, X7R, 10%
2.2u	1210, 100V, X7R, 10%
10u	1210, 25V, X7R, 10%
22u	1210, 10V, X7R, 10%
100u	1210, 10V, X5R, 20%

All resistors are SMD 0402, 63mW, 1% except where marked differently.

Components marked DNP (Do Not Place) are foreseen for testing purposes and should NOT be placed.

TOP layer

FM1 FIDUCIAL FM2 FIDUCIAL FM3 FIDUCIAL

BOTTOM layer

FM4 FIDUCIAL FM5 FIDUCIAL FM6 FIDUCIAL

DRAWN	Dušan Slavinec		01.09.2014
CHECKED	-		
APPROVED	-		

Title: CSL_FTRN_AMC

Size: A3 | Type: SE | DWG.NO. | REV. A

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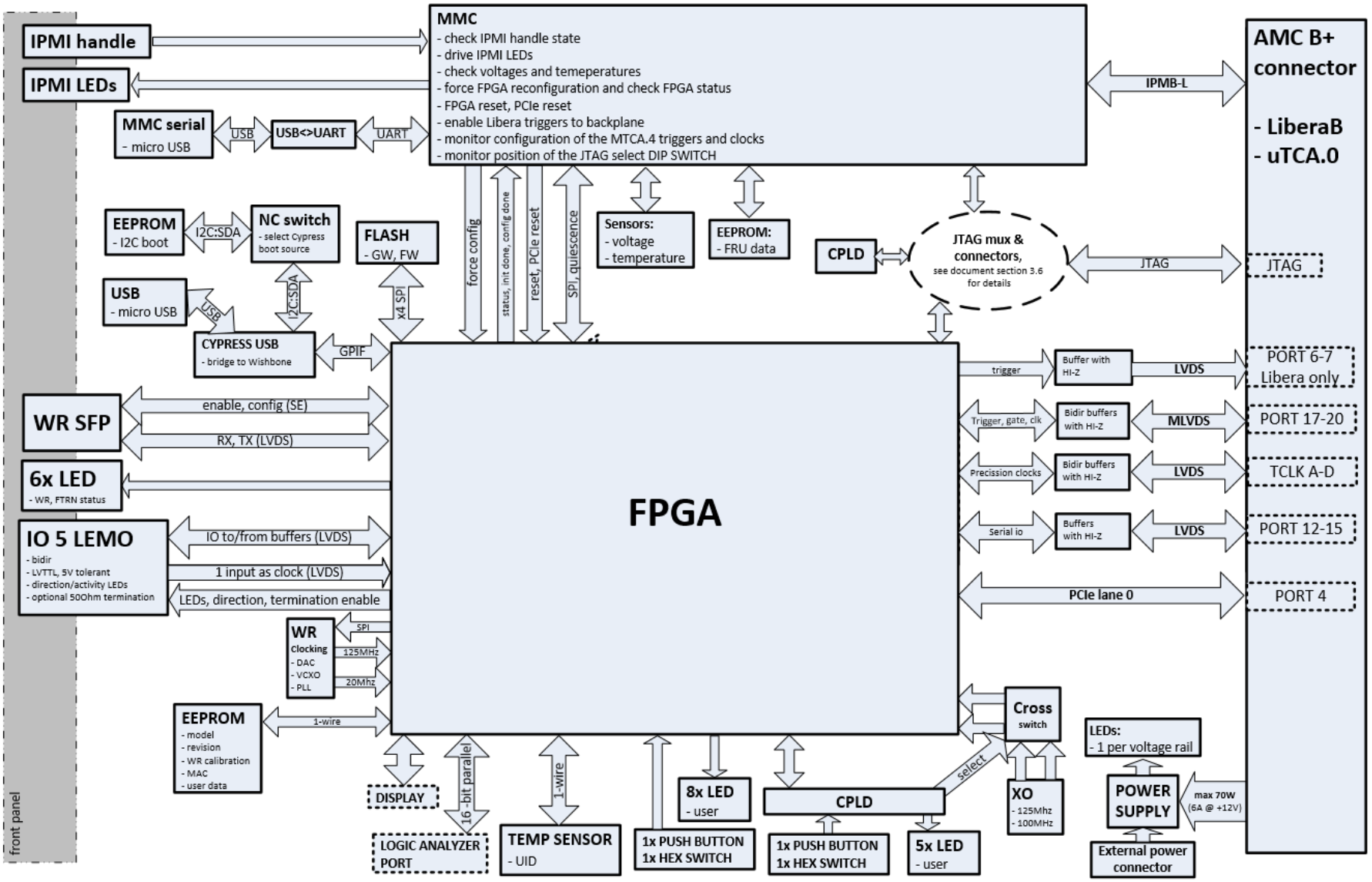
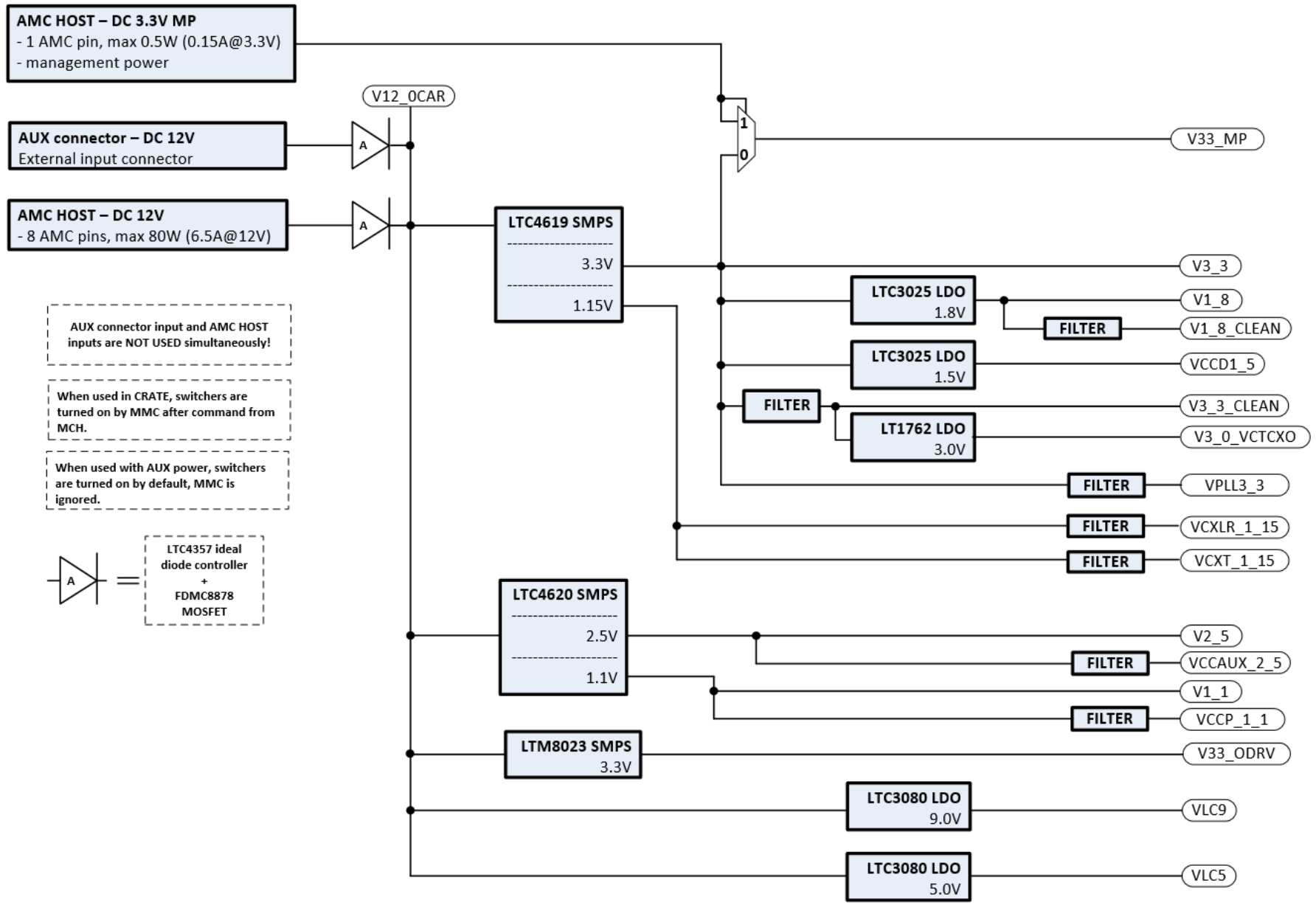
Block Diagram - FTRN, MMC



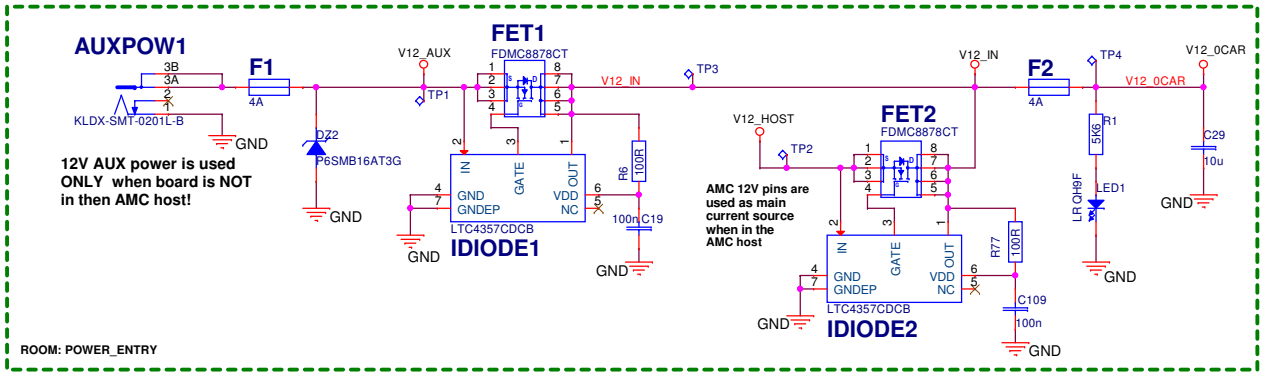
Title: Block Diagram - FTRN, MMC				
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC		REV. A
			SHEET 2 OF 17	

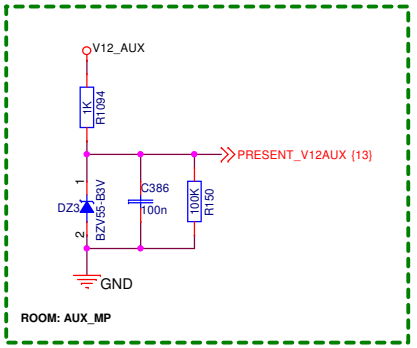
Power tree block scheme



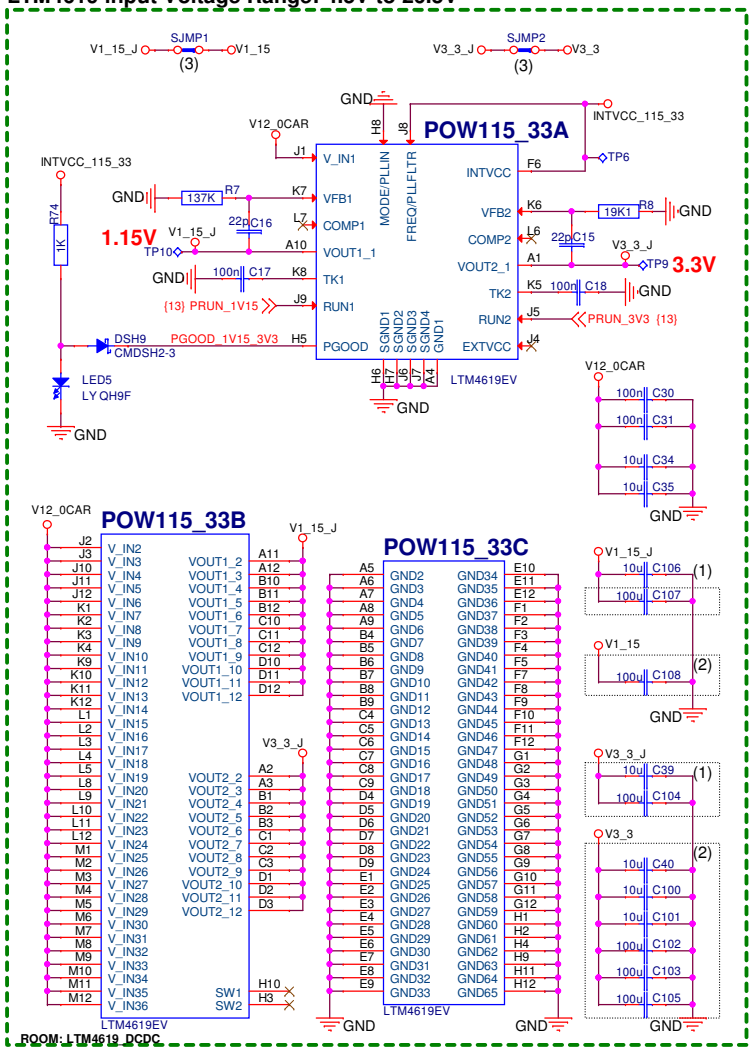
Title: Power tree block scheme				
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC		REV. A
			SHEET 3 OF 17	

Power entry and main DCDC power regulators

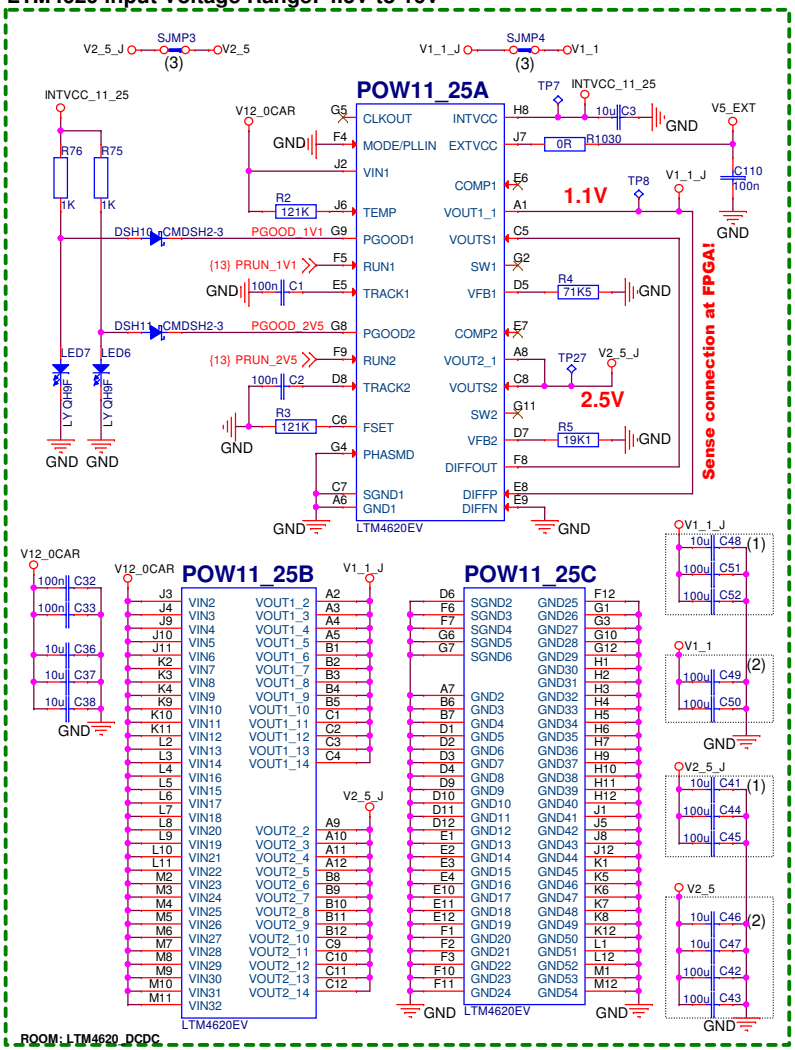




LTM4619 input Voltage Range: 4.5V to 26.5V



LTM4620 input Voltage Range: 4.5V to 16V



PGOOD_1V1 → PGOOD_1V1 {13}
PGOOD_2V5 → PGOOD_2V5 {13}
PGOOD_1V15_3V3 → PGOOD_1V15_3V3 {13}

PGOOD indicators to MMC

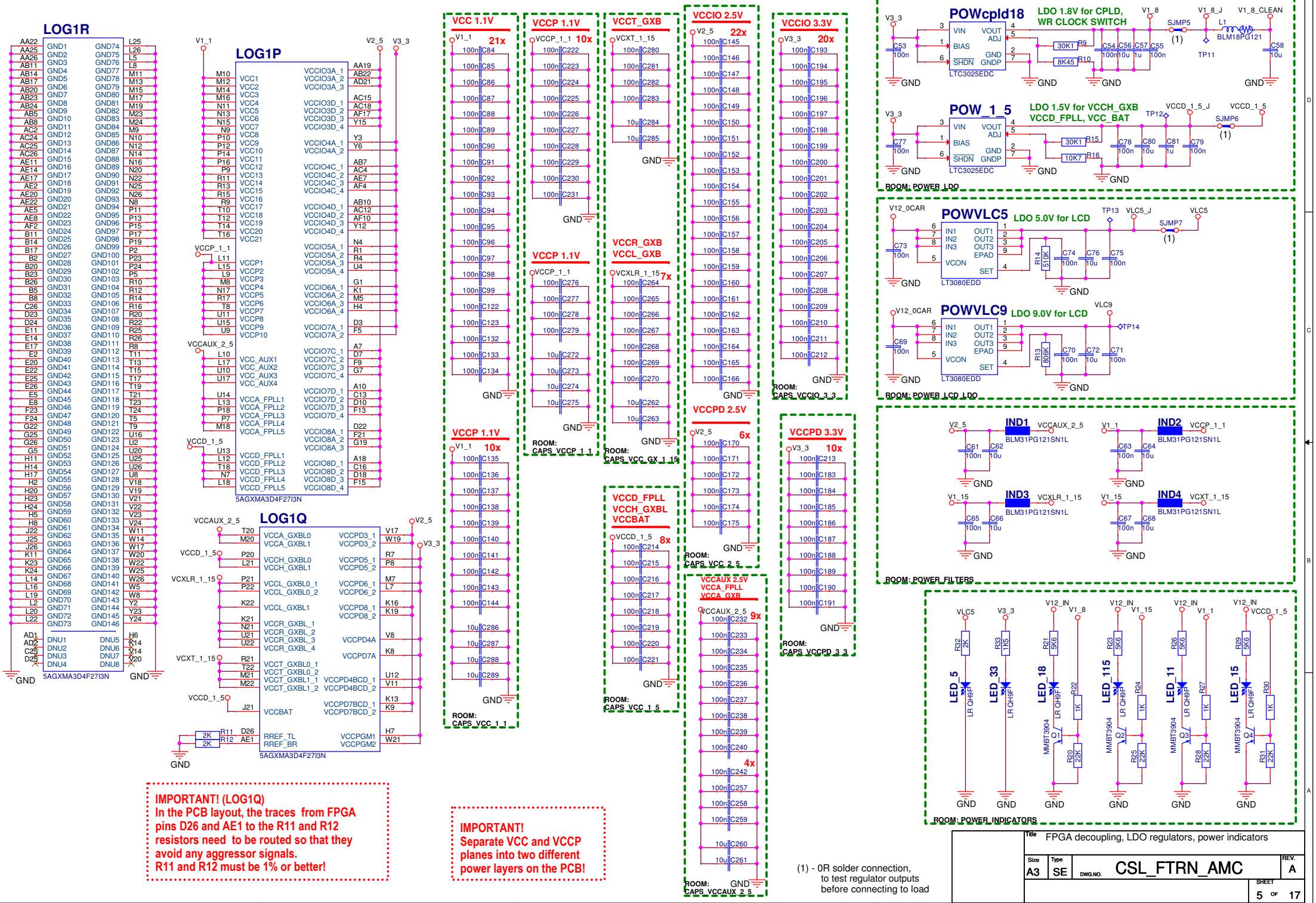
(1) - place capacitors on the regulator outputs

(2) - place capacitors away from the regulator outputs

(3) - 0R solder jumper, to test power regulator outputs before powering FPGA

Title: Power entry and main DCDC power regulators				
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A	
			SHEET 4 OF 17	

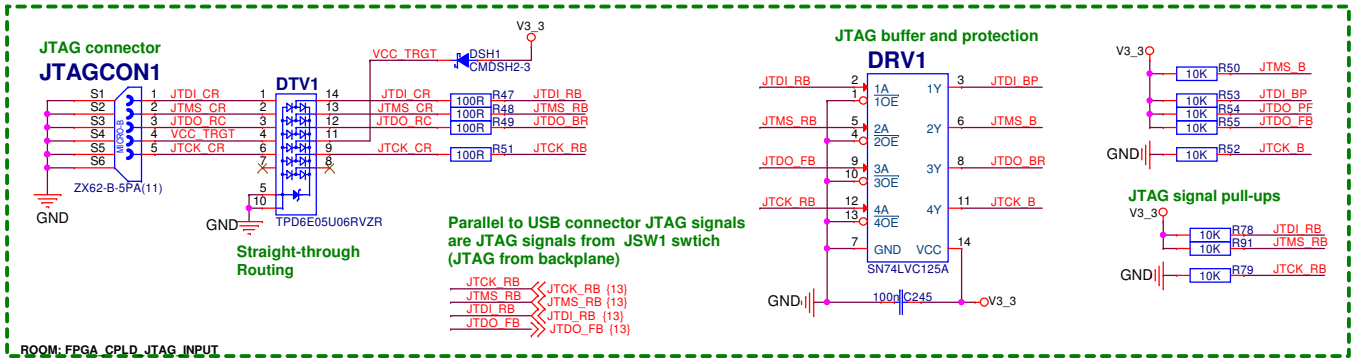
FPGA decoupling, LDO regulators, power indicators

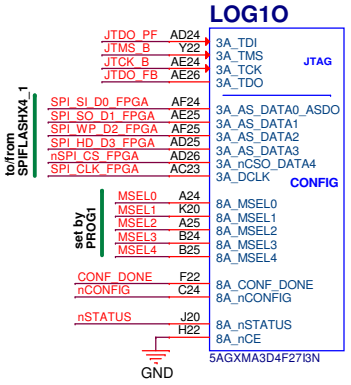


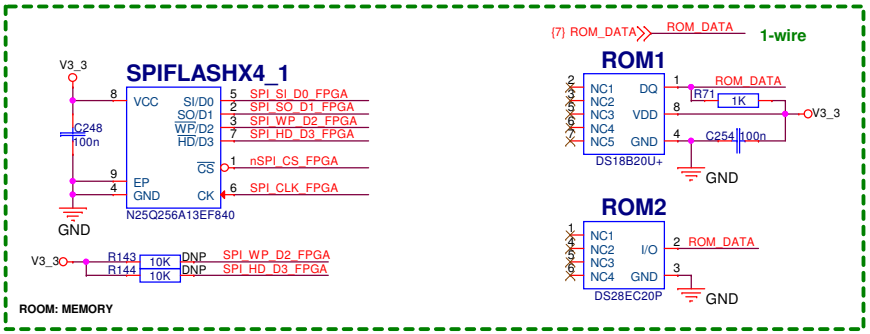
Title	FPGA decoupling, LDO regulators, power indicators		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 5 OF 17

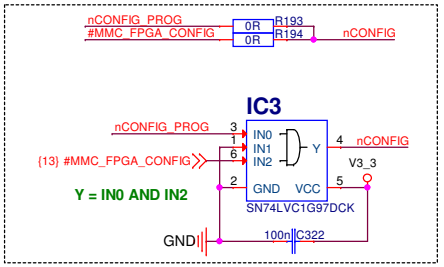
FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash

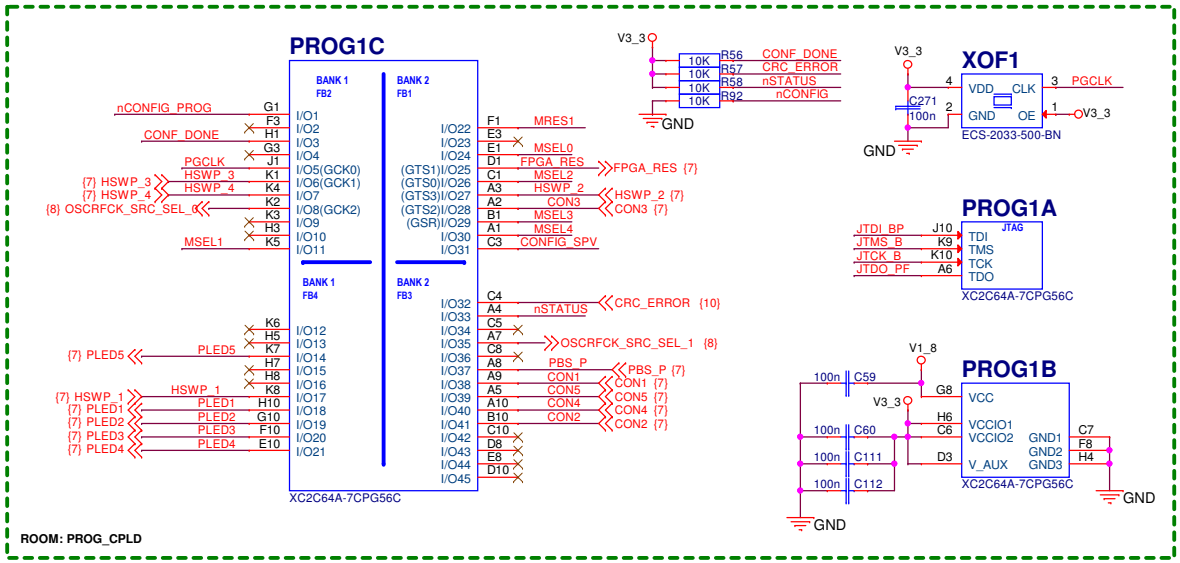
USB connector JTAG signals flow : C (connector) > R (resistor) > B (buffer) > P (PROG - CPLD) > F (FPGA) > B > C

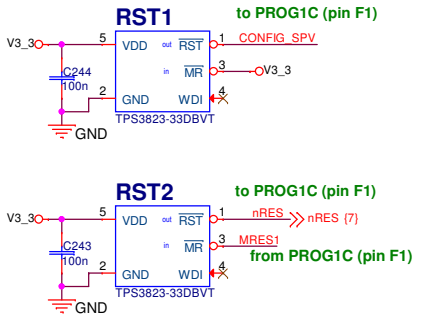












Title	FPGA and CPLD JTAG, FPGA gateware FLASH, User Flash		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 6 OF 17

User interface - USB, Display, push buttons, HEX switch, LEDs

DISPLAY LCD LED driver, connector

DIS1 — 91930-21121LF

DRV2 — SN74LVC125ARGY

ROOM: DISPLAY_CON_BLDRV

LOG1C

BANK 4A 3.3V

BOTTOM LEFT

5AGXMA3D4F27I3N

FPGA Push Button and HEX switch

PBF1 — KMR223G-LFG

HSF1 — P36S103

ROOM: FPGA_PB_HEXSW

CPLD Push Button and HEX switch

PBP1 — KMR223G-LFG

HSP1 — P36S103

ROOM: CPLD_PB_HEXSW

PROG status LEDs (on board)

ROOM: LEDS_PROG_STATUS

WR / FTRN STATUS LEDs (on front panel from FPGA)

DRVLED2 — SN74LVC245ARGYR

ROOM: LEDS_FTRN_STATUS

Logic analyzer connector

HPLA1 — 91930-21121LF

Logic Analyzer

USER LEDs (on board from FPGA)

DRVLED1 — SN74LVC245ARGYR

ROOM: LEDS_USER

LOG1D

BANK 4C 3.3V

BOTTOM LEFT

5AGXMA3D4F27I3N

LOG1G

BANK 6A 3.3V

UPPER LEFT

5AGXMA3D4F27I3N

USB bridge - USB 2.0

USBCON1 — ZX62-B-5PA(11)

DUSB1 — TPD6E05U06RVZR

XTL1 — C1E-24.000-12-3050-R

USB1A — CY7C68013A-56BAXC

USB1B — CY7C68013A-56BAXC

FLASHI2C1 — 24LC512I/MF

S1 — D3SH-B0L

USB <> FPGA interface

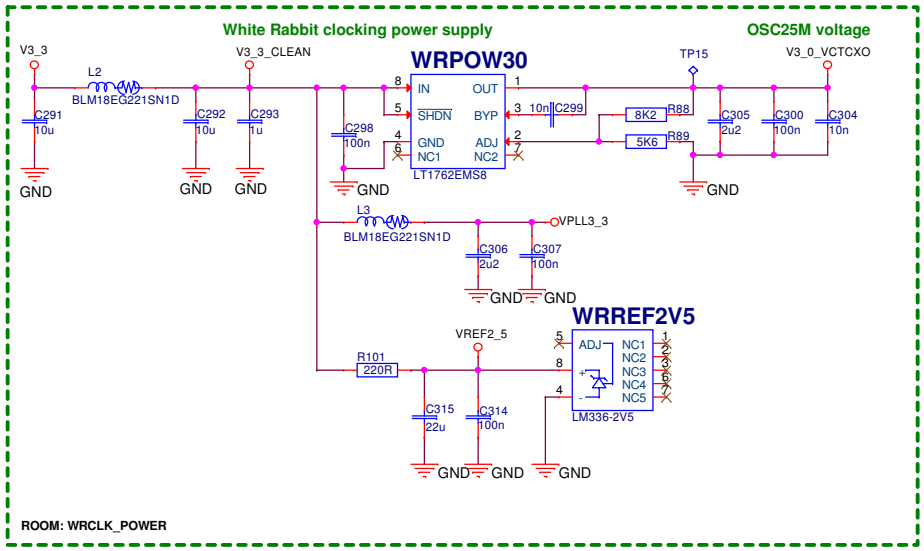
FPGA <> USB interface

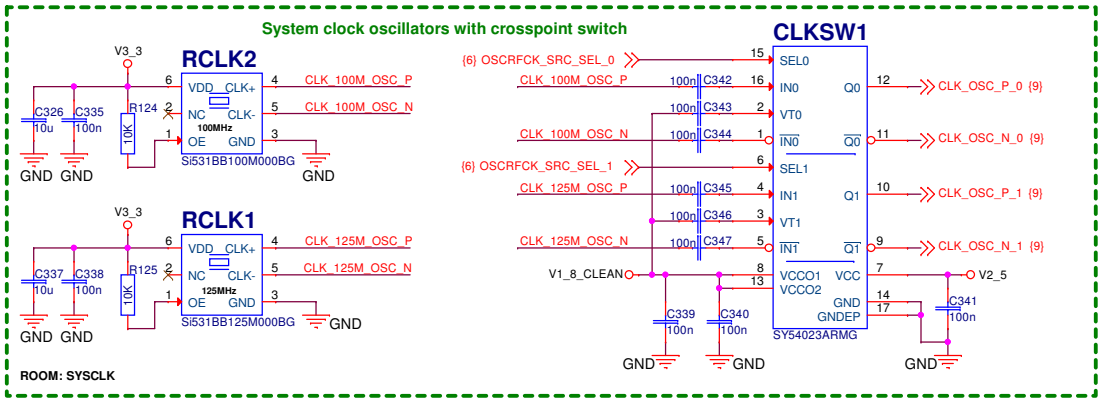
IMPORTANT! (USB1B)
Connect AGND to GND with as short a path as possible!

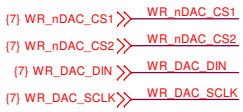
ROOM: USB_INTERFACE

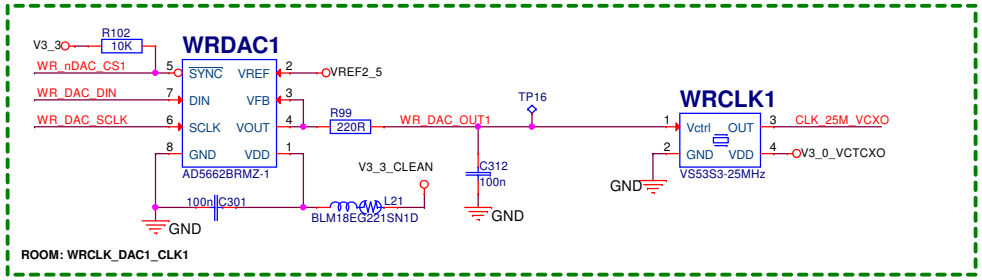
Title	User interface - USB, Display, push buttons, HEX switch, LEDs		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 7 OF 17

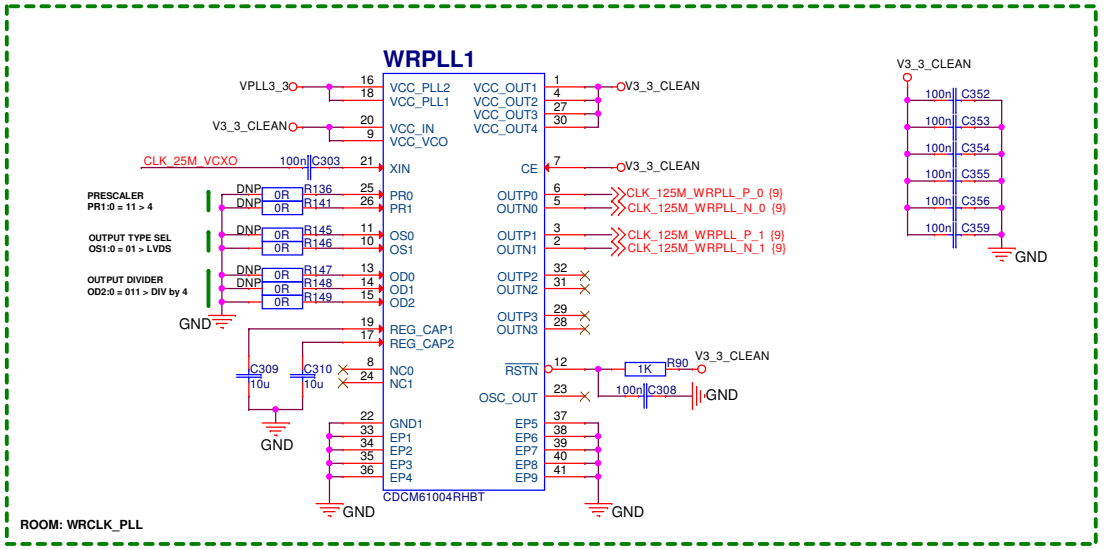
Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch

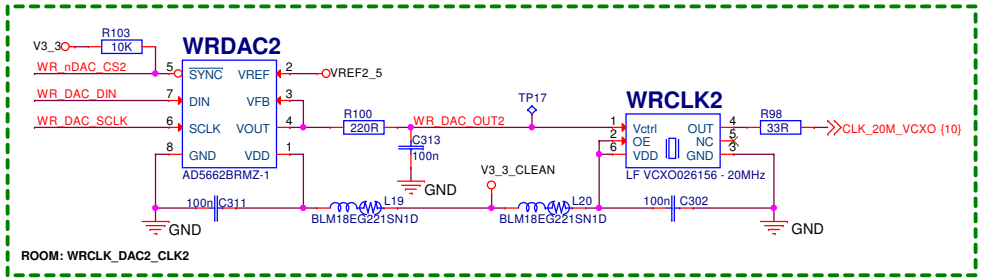






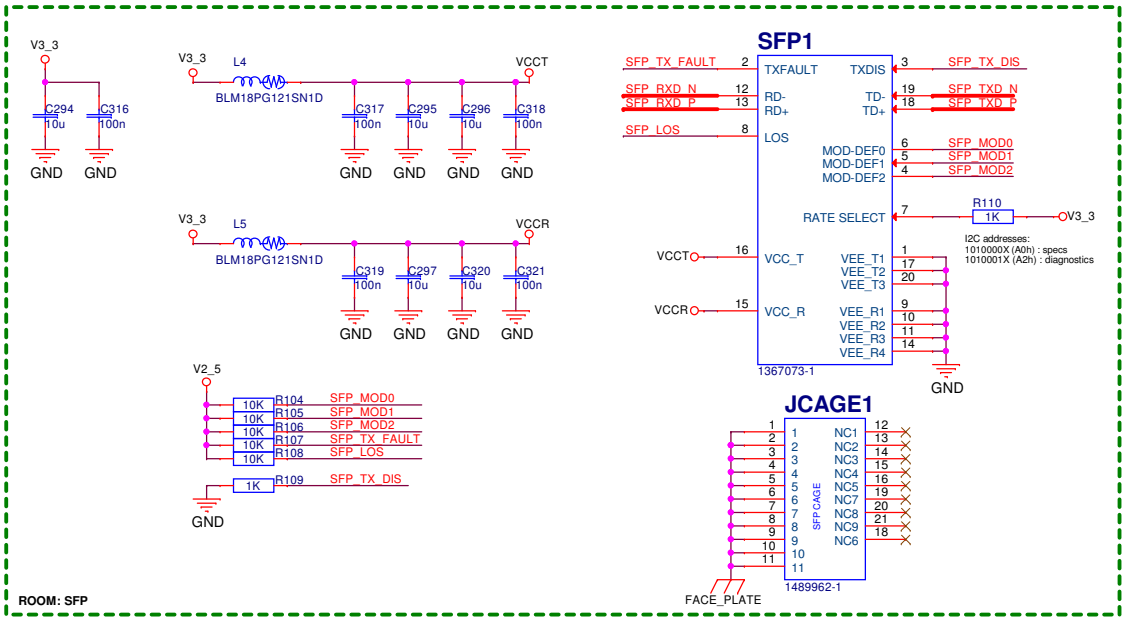




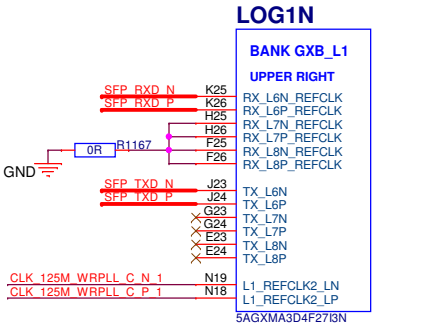


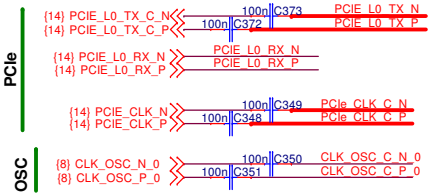
Title	Clocking: White Rabbit DAC, oscillators, PLL ; System clocks and clock crosspoint switch		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 8 OF 17

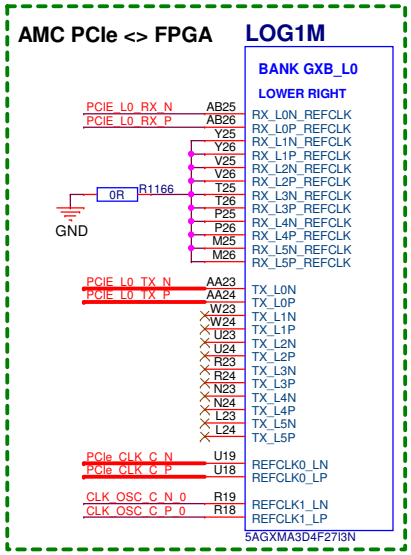
Fiber SFP, PCIe <> FPGA connections

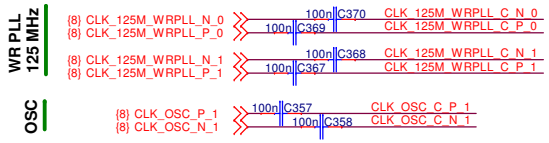


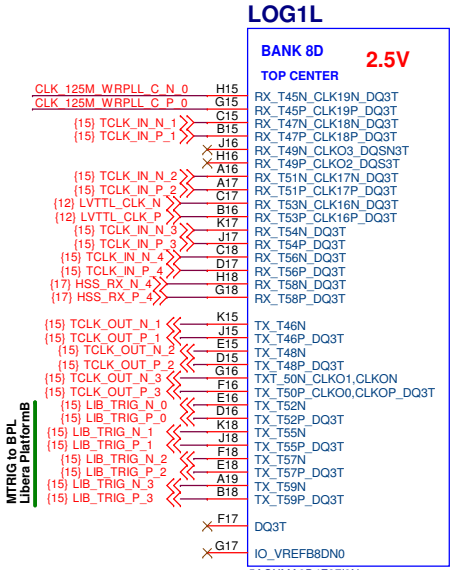
IMPORTANT!
Hi speed Gigabit lines
100R differential

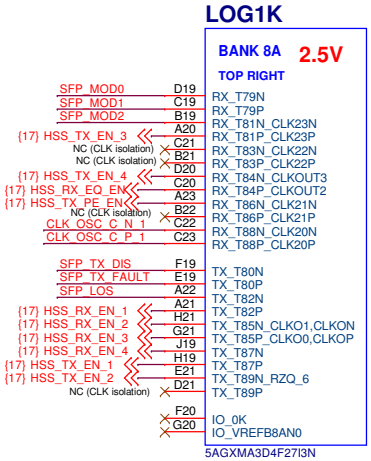


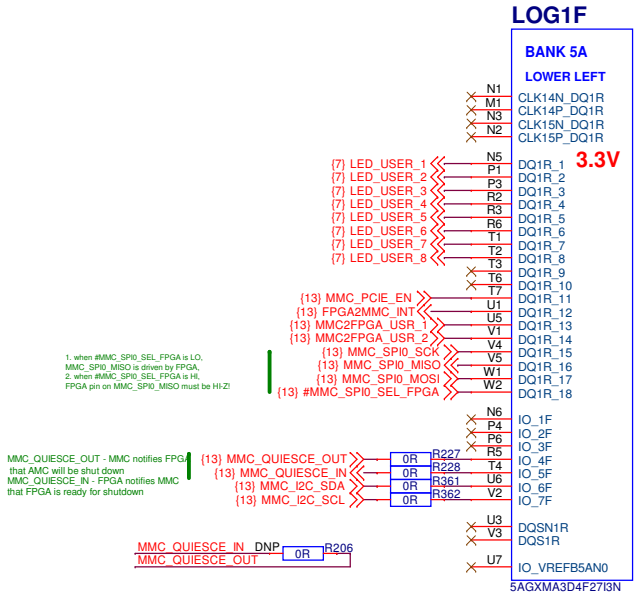








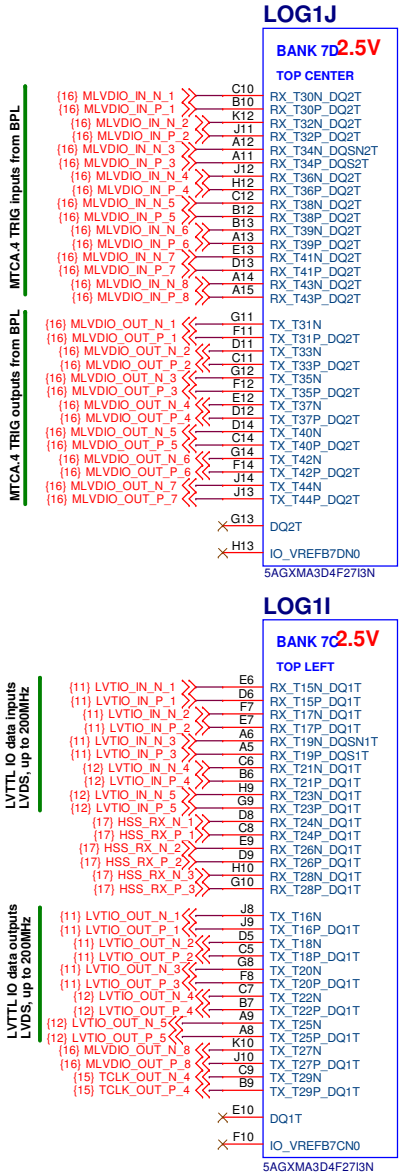


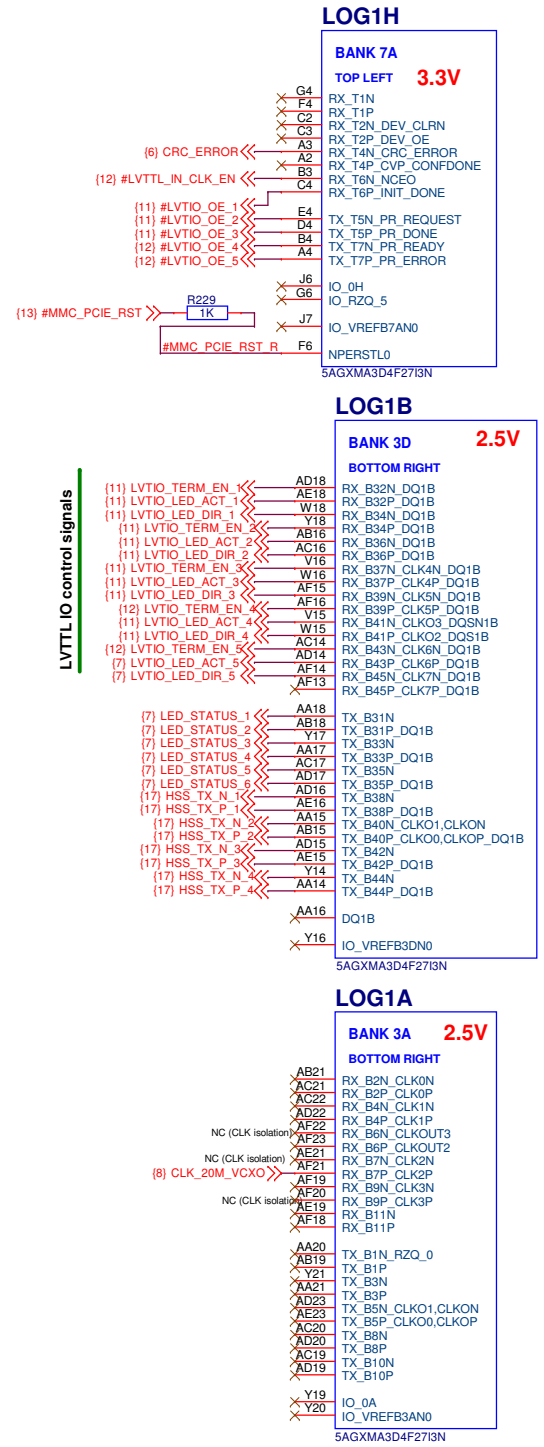


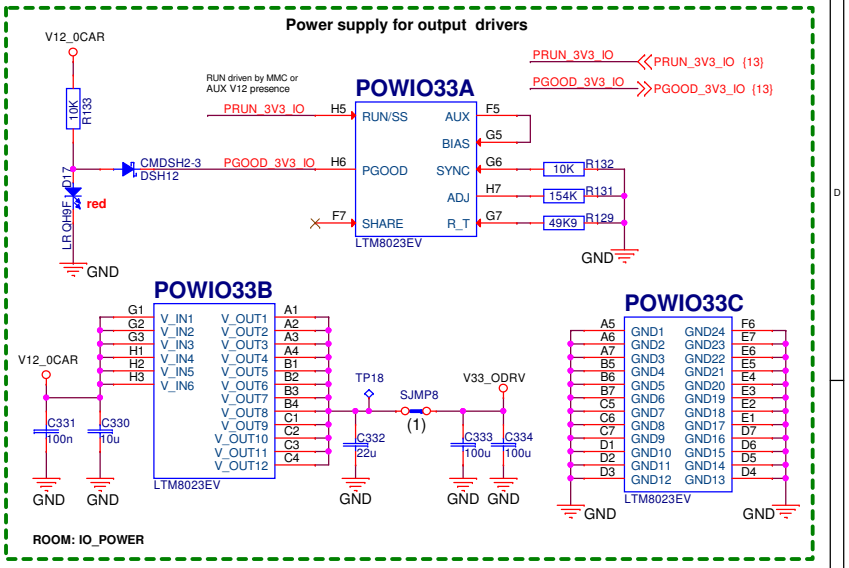
1. when #MMC_SPI0_SEL_FPGA is LO, MMC_SPI0_MISO is driven by FPGA,
2. when #MMC_SPI0_SEL_FPGA is HI, FPGA pin on MMC_SPI0_MISO must be HI-Z!

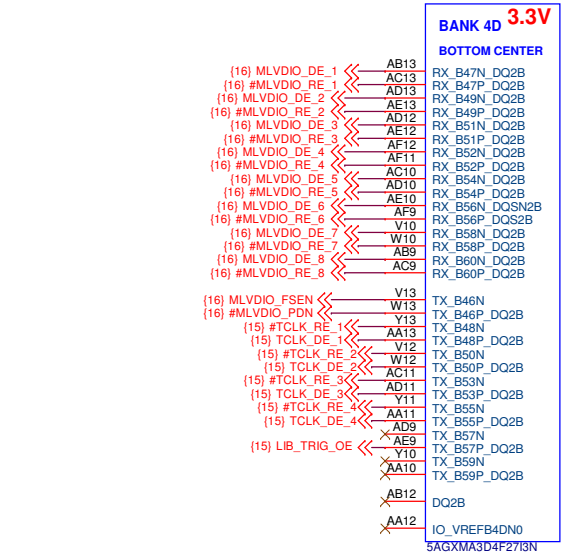
Title	Fiber SFP, PCIe <> FPGA connections		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
		SHEET 9 OF 17	

IO block power supply, FPGA <> IO block connections





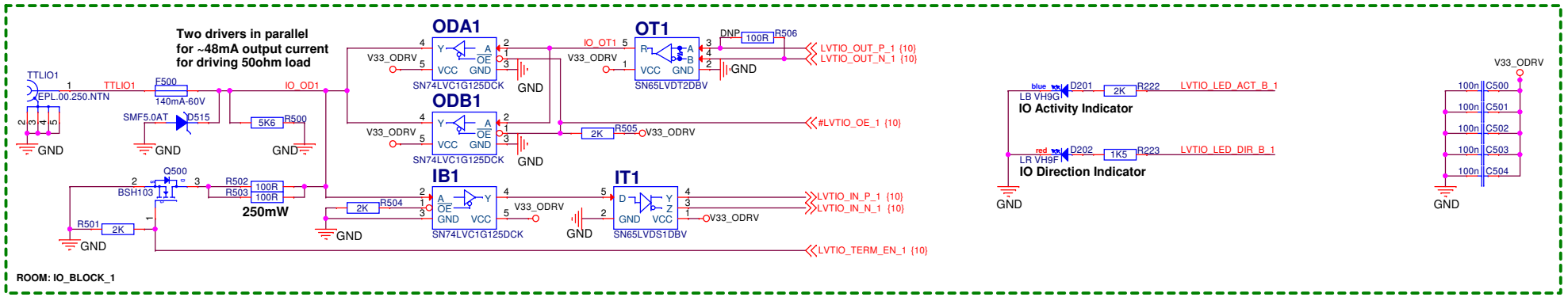


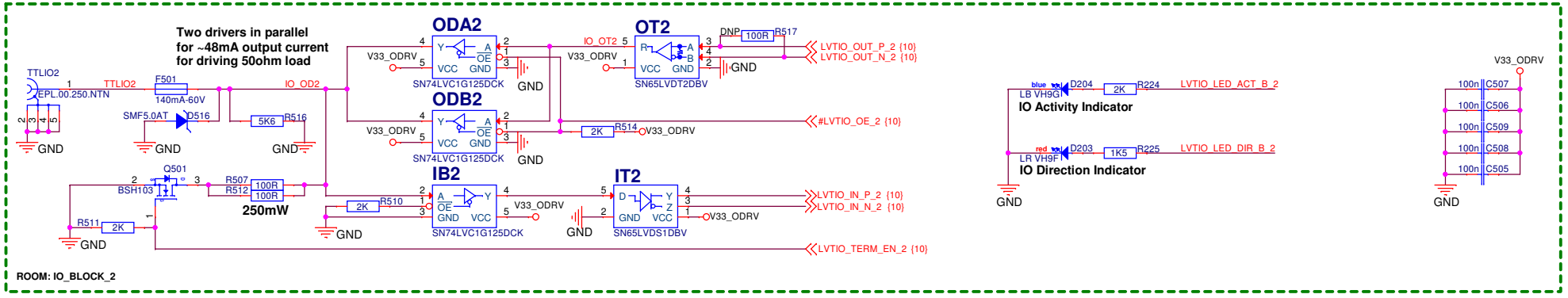


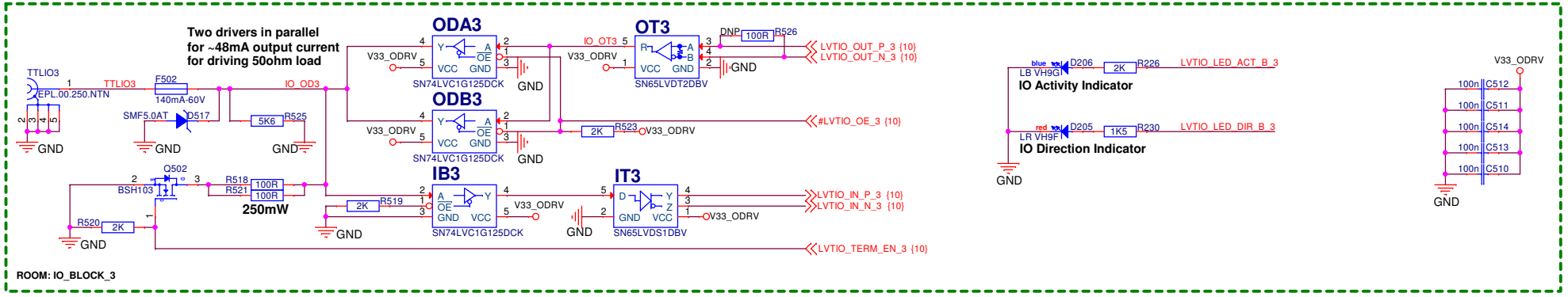
(1) - 0R solder connection,
to test regulator outputs
before connecting to load

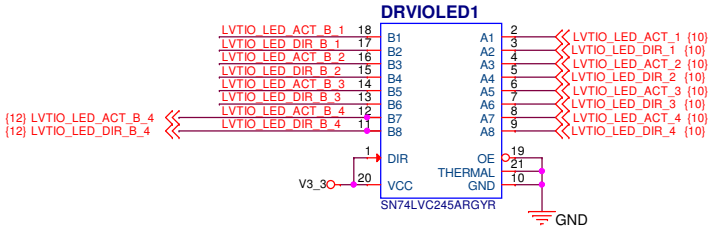
Title: IO block power supply, FPGA <> IO block connections			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 10 OF 17

LVTTL IO blocks 1-3



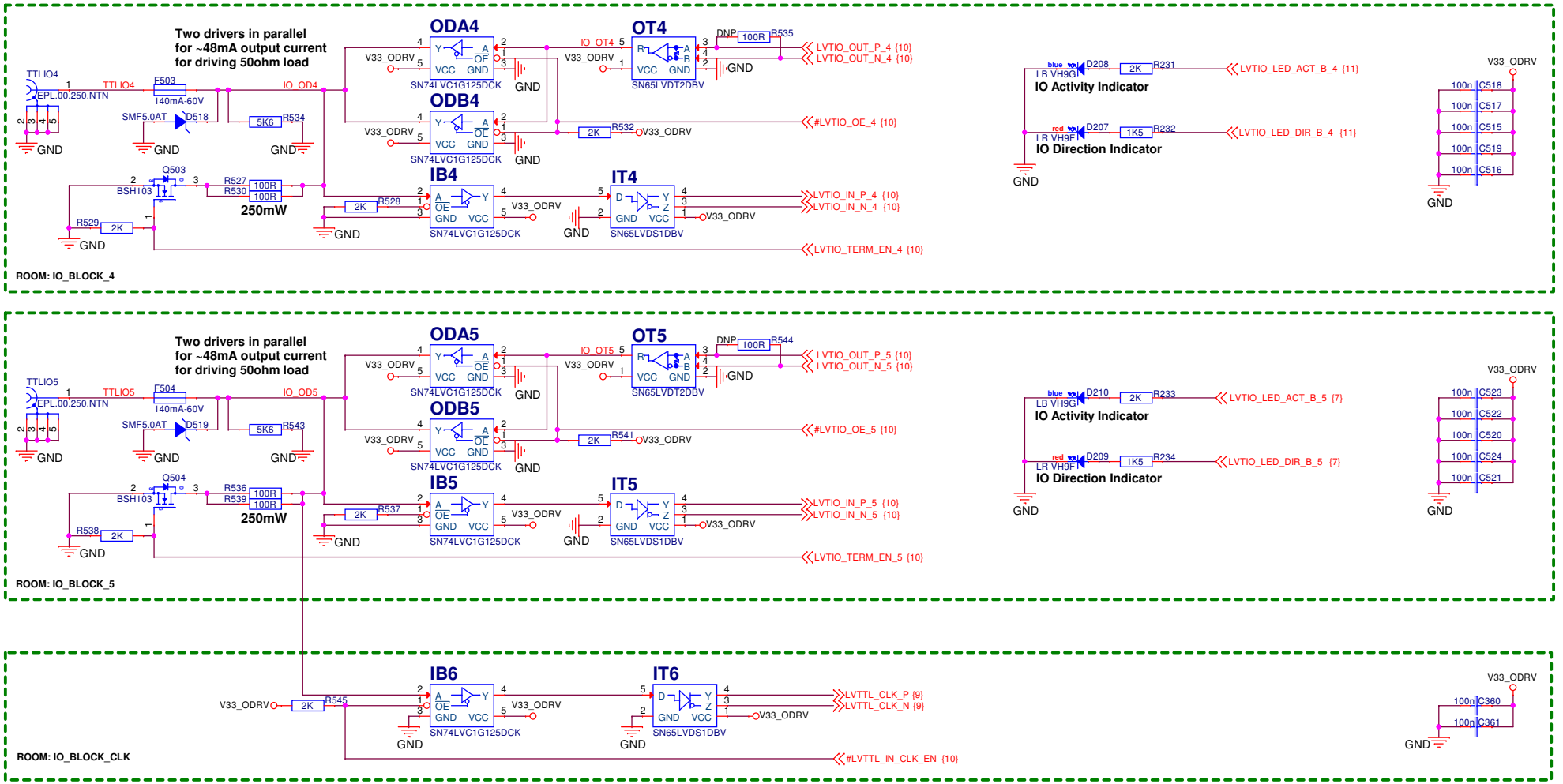




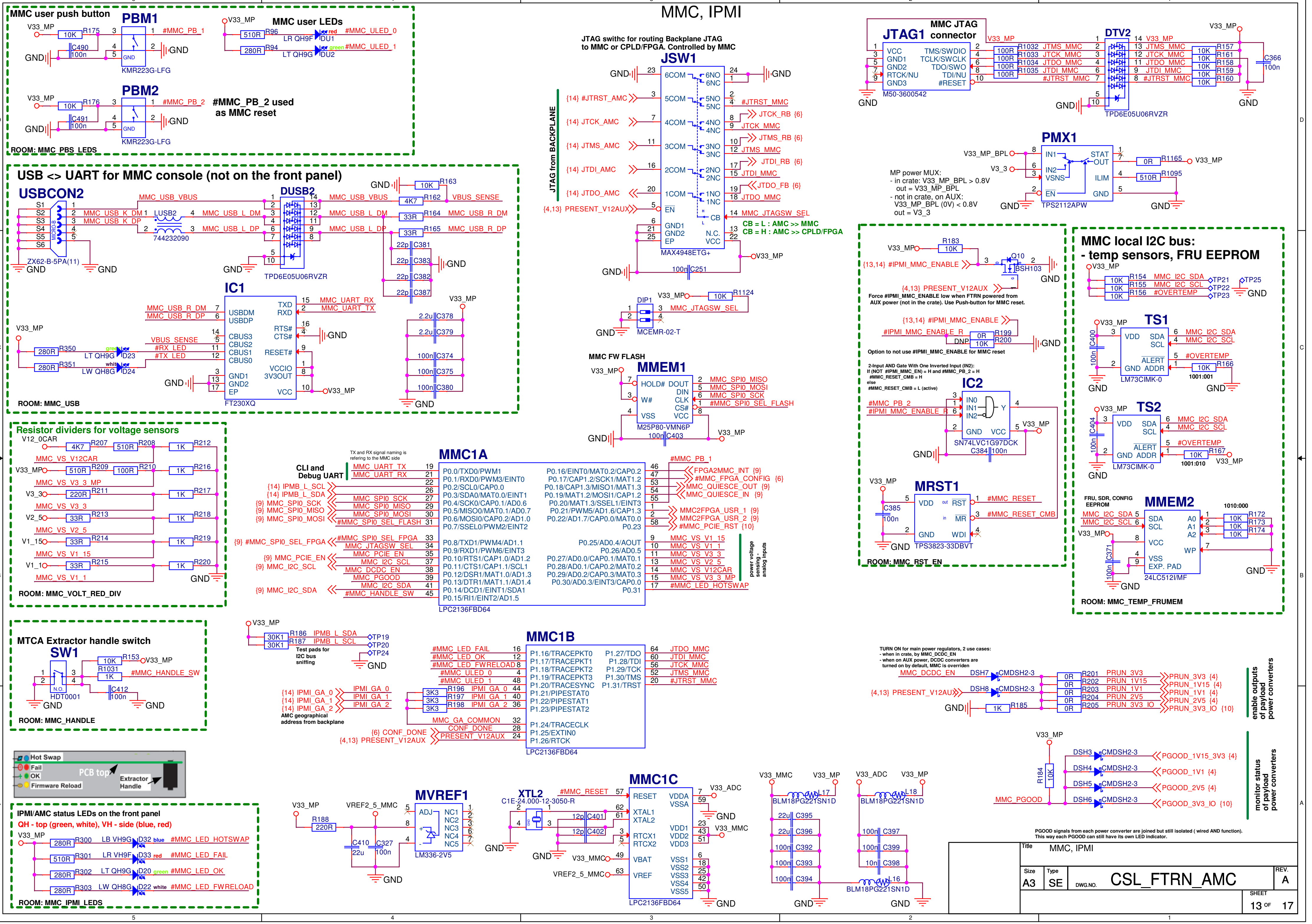


Title	LVTTL IO blocks 1-3		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 11 OF 17

LVTTL IO blocks 4-5, IO CLOCK input

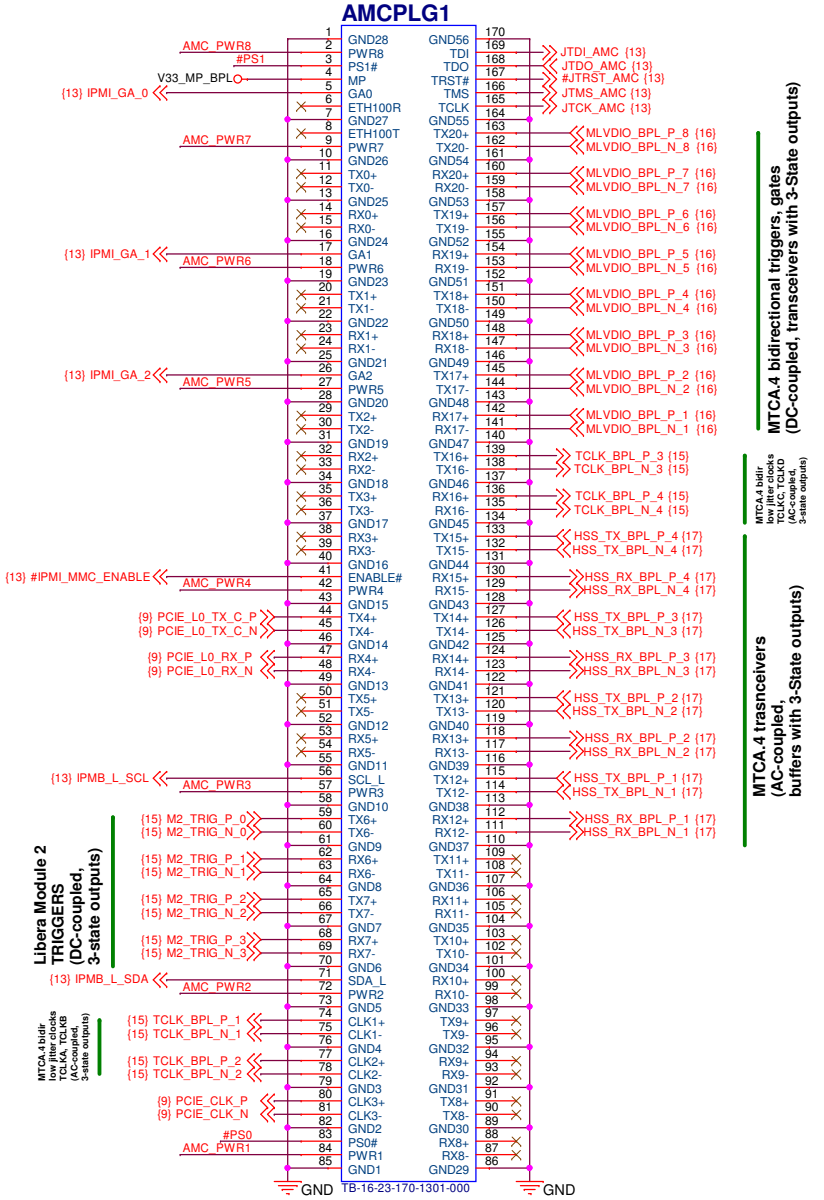


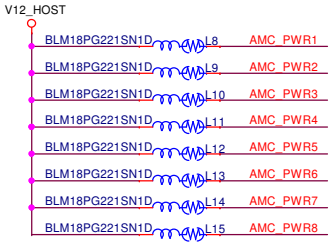
Title	LVTTL IO blocks 4-5, IO CLOCK input			
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC		REV. A
				SHEET 12 OF 17

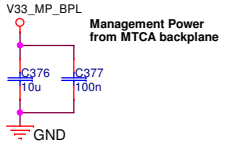


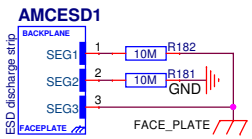
MMC, IPMI
MMC user push button
PBM1
PBM2
KMR223G-LFG
#MMC_PB_2 used as MMC reset
MMC user LEDs
ROOM: MMC_PBS_LEDS
USB <> UART for MMC console (not on the front panel)
USBCON2
DUSB2
ZX62-B-5PA(11)
744232090
TPD6E05U06RVZR
IC1
FT230XQ
ROOM: MMC_USB
JTAG swithc for routing Backplane JTAG to MMC or CPLD/FPGA. Controlled by MMC
JSW1
JTAG from BACKPLANE
MAX4948ETG+
CB = L : AMC >> MMC
CB = H : AMC >> CPLD/FPGA
DIP1
MCEMR-02-T
MMC FW FLASH
MMEM1
M25P80-VMN6P
JTAG1
MMC JTAG connector
M50-3600542
DTV2
TPD6E05U06RVZR
PMX1
TPS2112APW
MP power MUX:
- in crate: V33_MP_BPL > 0.8V
out = V33_MP_BPL
- not in crate, on AUX:
V33_MP_BPL (0V) < 0.8V
out = V3_3
Q10
BSH103
Force #IPMI_MMC_ENABLE low when FTRN powered from AUX power (not in the crate). Use Push-button for MMC reset.
Option to not use #IPMI_MMC_ENABLE for MMC reset
IC2
SN74LVC1G97DCK
MRST1
TPS3823-33DBVT
ROOM: MMC_RST_EN
MMC local I2C bus:
- temp sensors, FRU EEPROM
TS1
LM73CIMK-0
TS2
LM73CIMK-0
FRU, SDR, CONFIG EEPROM
MMEM2
24LC512I/MF
ROOM: MMC_TEMP_FRUMEM
Resistor dividers for voltage sensors
ROOM: MMC_VOLT_RED_DIV
MMC1A
LPC2136FBD64
CLI and Debug UART
power voltage sensing - analog inputs
MTCA Extractor handle switch
SW1
HDT0001
ROOM: MMC_HANDLE
Test pads for I2C bus sniffing
MMC1B
LPC2136FBD64
AMC geographical address from backplane
TURN ON for main power regulators, 2 use cases:
- when in crate, by MMC_DCDC_EN
- when on AUX power, DCDC converters are turned on by default, MMC is overriden
enable outputs of payload power converters
monitor status of payload power converters
PGOOD signals from each power converter are joined but still isolated (wired AND function). This way each PGOOD can still have its own LED indicator.
Hot Swap
Fail
OK
Firmware Reload
PCB top
Extractor Handle
IPMI/AMC status LEDs on the front panel
QH - top (green, white), VH - side (blue, red)
ROOM: MMC_IPMI_LEDS
MVREF1
LM336-2V5
XTL2
C1E-24.000-12-3050-R
MMC1C
LPC2136FBD64
Title MMC, IPMI
Size A3
Type SE
DWG.NO. CSL_FTRN_AMC
REV. A
SHEET 13 OF 17

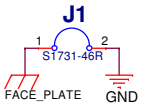
AMC backplane plug

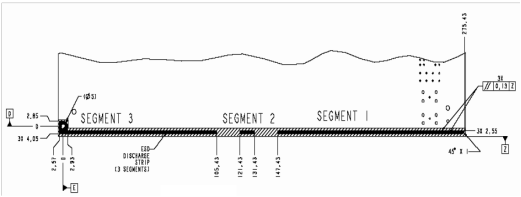






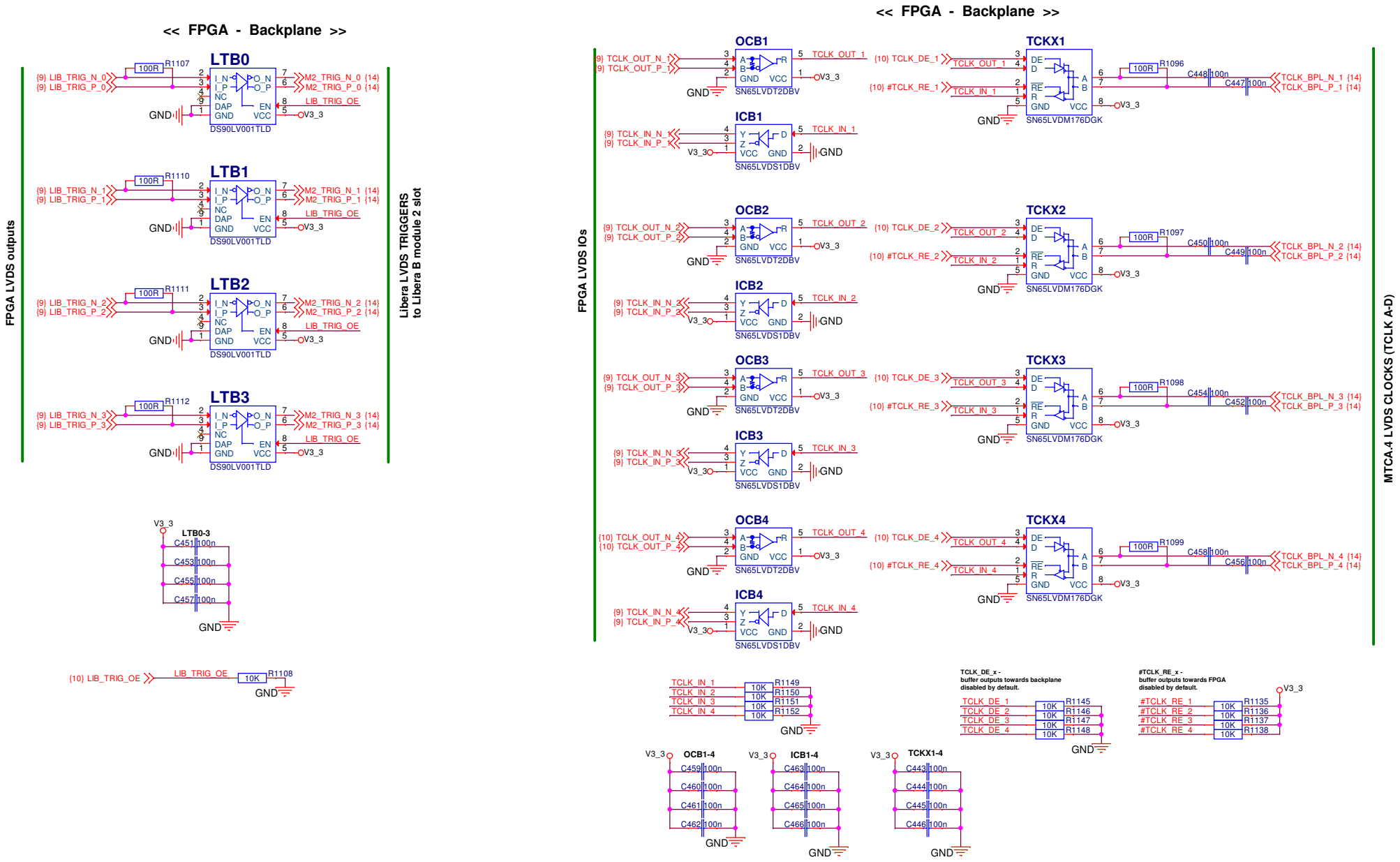






Title: AMC backplane plug			
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 14 OF 17

Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers



Title	Backplane buffers - MTCA.4 TCLK A-D, Libera B triggers		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 15 OF 17

Backplane buffers - MTCA.4 PORT 17-20 (M-LVDS triggers, clocks, gates)

FPGA LVDS IOs

{10} MLVDIO_FSEN → MLVDIO_FSEN

{10} #MLVDIO_PDN → #MLVDIO_PDN

OTB1

{10} MLVDIO_OUT_P_1 / {10} MLVDIO_OUT_N_1 → MLVDIO_OUT_1

SN65LVDT2DBV

OTB2

{10} MLVDIO_OUT_P_2 / {10} MLVDIO_OUT_N_2 → MLVDIO_OUT_2

SN65LVDT2DBV

OTB3

{10} MLVDIO_OUT_P_3 / {10} MLVDIO_OUT_N_3 → MLVDIO_OUT_3

SN65LVDT2DBV

OTB4

{10} MLVDIO_OUT_P_4 / {10} MLVDIO_OUT_N_4 → MLVDIO_OUT_4

SN65LVDT2DBV

OTB5

{10} MLVDIO_OUT_P_5 / {10} MLVDIO_OUT_N_5 → MLVDIO_OUT_5

SN65LVDT2DBV

OTB6

{10} MLVDIO_OUT_P_6 / {10} MLVDIO_OUT_N_6 → MLVDIO_OUT_6

SN65LVDT2DBV

OTB7

{10} MLVDIO_OUT_P_7 / {10} MLVDIO_OUT_N_7 → MLVDIO_OUT_7

SN65LVDT2DBV

OTB8

{10} MLVDIO_OUT_P_8 / {10} MLVDIO_OUT_N_8 → MLVDIO_OUT_8

SN65LVDT2DBV

ITB1

{10} MLVDIO_IN_P_1 / {10} MLVDIO_IN_N_1 → MLVDIO_IN_1

SN65LVDS1DBV

ITB2

{10} MLVDIO_IN_P_2 / {10} MLVDIO_IN_N_2 → MLVDIO_IN_2

SN65LVDS1DBV

ITB3

{10} MLVDIO_IN_P_3 / {10} MLVDIO_IN_N_3 → MLVDIO_IN_3

SN65LVDS1DBV

ITB4

{10} MLVDIO_IN_P_4 / {10} MLVDIO_IN_N_4 → MLVDIO_IN_4

SN65LVDS1DBV

ITB5

{10} MLVDIO_IN_P_5 / {10} MLVDIO_IN_N_5 → MLVDIO_IN_5

SN65LVDS1DBV

ITB6

{10} MLVDIO_IN_P_6 / {10} MLVDIO_IN_N_6 → MLVDIO_IN_6

SN65LVDS1DBV

ITB7

{10} MLVDIO_IN_P_7 / {10} MLVDIO_IN_N_7 → MLVDIO_IN_7

SN65LVDS1DBV

ITB8

{10} MLVDIO_IN_P_8 / {10} MLVDIO_IN_N_8 → MLVDIO_IN_8

SN65LVDS1DBV

<< FPGA - Backplane >>

MTB1A

{10} MLVDIO_DE_1 / MLVDIO_OUT_1 / MLVDIO_FSEN / MLVDIO_IN_1 / {10} #MLVDIO_RE_1

{10} MLVDIO_DE_2 / MLVDIO_OUT_2 / MLVDIO_FSEN / MLVDIO_IN_2 / {10} #MLVDIO_RE_2

{10} MLVDIO_DE_3 / MLVDIO_OUT_3 / MLVDIO_FSEN / MLVDIO_IN_3 / {10} #MLVDIO_RE_3

{10} MLVDIO_DE_4 / MLVDIO_OUT_4 / MLVDIO_FSEN / MLVDIO_IN_4 / {10} #MLVDIO_RE_4

1DE 1D 1A 1B 1FSEN 1R 1RE → MLVDIO_BPL_P_1 {14} / MLVDIO_BPL_N_1 {14}

2DE 2D 2A 2B 2FSEN 2R 2RE → MLVDIO_BPL_P_2 {14} / MLVDIO_BPL_N_2 {14}

3DE 3D 3A 3B 3FSEN 3R 3RE → MLVDIO_BPL_P_3 {14} / MLVDIO_BPL_N_3 {14}

4DE 4D 4A 4B 4FSEN 4R 4RE → MLVDIO_BPL_P_4 {14} / MLVDIO_BPL_N_4 {14}

PDN ← #MLVDIO_PDN

SN65MLVD040RGZ

MTB2A

{10} MLVDIO_DE_5 / MLVDIO_OUT_5 / MLVDIO_FSEN / MLVDIO_IN_5 / {10} #MLVDIO_RE_5

{10} MLVDIO_DE_6 / MLVDIO_OUT_6 / MLVDIO_FSEN / MLVDIO_IN_6 / {10} #MLVDIO_RE_6

{10} MLVDIO_DE_7 / MLVDIO_OUT_7 / MLVDIO_FSEN / MLVDIO_IN_7 / {10} #MLVDIO_RE_7

{10} MLVDIO_DE_8 / MLVDIO_OUT_8 / MLVDIO_FSEN / MLVDIO_IN_8 / {10} #MLVDIO_RE_8

1DE 1D 1A 1B 1FSEN 1R 1RE → MLVDIO_BPL_P_5 {14} / MLVDIO_BPL_N_5 {14}

2DE 2D 2A 2B 2FSEN 2R 2RE → MLVDIO_BPL_P_6 {14} / MLVDIO_BPL_N_6 {14}

3DE 3D 3A 3B 3FSEN 3R 3RE → MLVDIO_BPL_P_7 {14} / MLVDIO_BPL_N_7 {14}

4DE 4D 4A 4B 4FSEN 4R 4RE → MLVDIO_BPL_P_8 {14} / MLVDIO_BPL_N_8 {14}

PDN ← #MLVDIO_PDN

SN65MLVD040RGZ

MTCA.4 M-LVDS TRIGGERS, GATES (PORT 17-20)

/RE and FSEN pins have internal pull-UP resistors.
DE and /PDN pin has internal pull-DOWN resistors.

MLVDIO_IN_1 … MLVDIO_IN_8 — 10K — R1153 … R1160 — GND

Define state when /RE is HI.

MTB1B

1GND 2GND 3GND 4GND 5GND 6GND 7GND 8GND 9GND
1VCC 2VCC 3VCC 4VCC 5VCC 6VCC
2NC 1NC

V3_3 — C389 C413 C414 C415 C416 C417 C418 C419 100n — GND

SN65MLVD040RGZ

MTB2B

1GND 2GND 3GND 4GND 5GND 6GND 7GND 8GND 9GND
1VCC 2VCC 3VCC 4VCC 5VCC 6VCC
2NC 1NC

V3_3 — C390 C420 C421 C422 C423 C424 C425 C426 100n — GND

SN65MLVD040RGZ

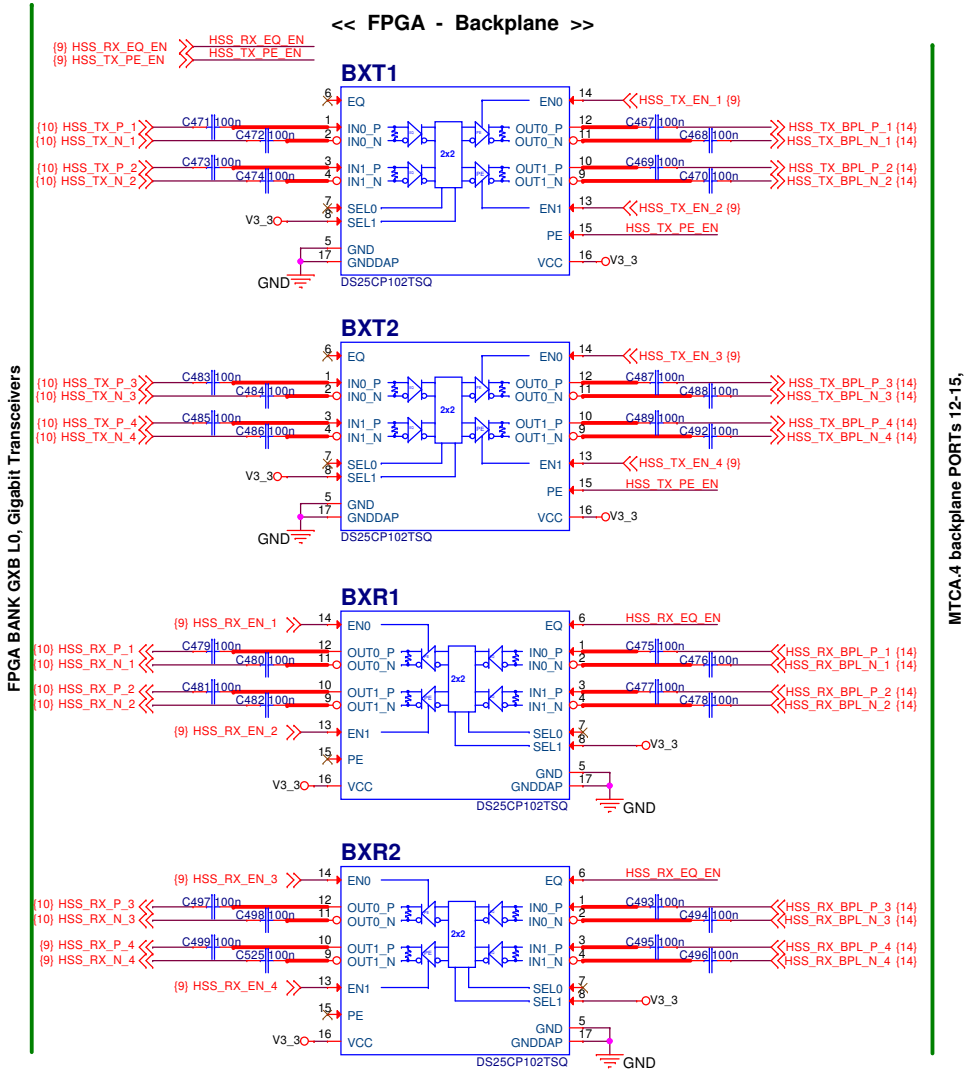
V3_3 — OTB1-8 — C431 C432 C433 C434 C427 C428 C429 C430 100n — GND

V3_3 — ITB1-8 — C435 C436 C437 C438 C439 C440 C441 C442 100n — GND

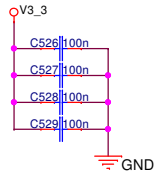
Title	Backplane buffers - MTCA.4 PORT 17-20 (M-LVDS triggers, clocks, gates)		
Size A3	Type SE	DWG.NO. CSL_FTRN_AMC	REV. A
			SHEET 16 OF 17

Backplane buffers - MTCA.4 PORT 12-15 (High Speed Serial)

IMPORTANT!
Hi speed Gigabit lines
100R differential



PE - Transmit Pre-Emphasis select pin. There is a 20k pulldown resistor on this pin
EQ - Receive Equalization select pin. There is a 20k pulldown resistor on this pin.
SEL0, SEL1 - Switch configuration pins. There is a 20k pulldown resistor on this pin.



Title: Backplane buffers - MTCA.4 PORT 12-15 (High Speed Serial)				
Size: A3	Type: SE	DWG.NO. CSL_FTRN_AMC	REV. A	
			SHEET 17 OF 17	