SVEC → SVEC7 Redesign

Technical specification

Tomasz Włostowski/CERN
Date: 12/16/2019
Last Updated: 06/04/2020

1. Introduction

This document describes the changes to the SVEC card design (EDA-02530-V3-0) that will lead to its successor, the SVEC7.

Rationale: the original SVEC design has a insufficient memory bandwidth to handle even modest gigasample ADC cards (such as 1GSPS/8bits/channel). The primary goal is to increase the memory performance by using a 64-bit SO-DIMM DDR3 module and a faster FPGA (Kintex-7 compared to Spartan-6).

Important features **added** in SVEC7 with respect to the original SVEC design:
- Faster memory (DDR3 SODIMM @ 64 bits/1600 MHz)
- Faster and bigger FPGA (Kintex-7)
- Gigabit links up to 6 Gbps (4 x GTX for FMC1, 1 x GTX for FMC2, 2 x Front Panel, 1 x WR)
- Programmable Vadj shared between both slots (1.8/2.5/3.3 V)

Important features **dropped** with respect to the original SVEC design:
- No parallel USB interface
- No LVDS in P2 (only 3.3v single-ended – a limitation of the 7 series FPGAs)
- No SSTL/HSTL in FMC connectors (not used by most FMCs)

2. List of changes

2.1. The FPGA

Change the FPGA to XC7K160T-2FBG676 (C or I variant)

2.2. Removal of unused/legacy features

- Remove the parallel USB interface (IC37 and components around).
- Leave only the CP2103 UART (IC17)
- Remove J1 and J16 (stand-alone power port).

2.3. DDR memory

- Remove the discrete DDR chips (IC28, IC4)
- Change the DDR memory to a DDR SO-DIMM module socket (no ECC)
- Use the pin assignment in the provided constraint file (`syn/common/svec7/ddr.xdc`)
- Can pin swap data pins within the byte groups
- Connect the SPD I2C interface to a 3.3V bank (see the constraint files)

2.4. Flash memory

Add a separate flash for bitstream storage for the AFPGA connected to Xilinx's boot SPI interface. This flash must be also connected to the SFPGA, so that the bootloader can access it.

2.5. VME interface

We don't have enough pins for a full VME interface in the AFPGA, therefore the SVEC7 will use a low pin count inter-FPGA link to tunnel the VME traffic through the SFPGA. The pins are described in the table below:

Signals	Count	I/O Standard	Function	Direction
sfpga_tx_o	5	SSTL15	AFPGA Tx Data out	AFPGA → SFPGA
sfpga_rx_i	5	SSTL15	AFPGA Rx Data in	SFPGA → AFPGA
sfpga_clk_p_o	1	DIFF_SSTL15	SFPGA clock, positive	AFPGA → SFPGA
sfpga_clk_n_o	1	DIFF_SSTL15	SFPGA clock, negative	AFPGA → SFPGA

All pins use the SSTL15 I/O standard, reusing the power supply/Vref of the DDR3 memory. Please use the supplied XDC file for the pin assignment in the AFPGA. On the SFPGA side, power an entire bank from 1.5V and supply the 0.75V Vref. All singals must be terminated on the far side (check Xilinx UG471). The 1.5V SFPGA bank can be also used for DIP switches (SWITCH0..1, NOGA0..5) and debug LEDs. The RSVD lines between the AFPGA and SFPGA can be dropped.

2.6. Slow I/O

In order to further reduce the number of required pins in the AFPGA, some of the slow I/Os of the SVEC will be moved to an I/O expander. Use the 74LV595/74LV166 shift registers as the I/O expanders an connect them to the the ioexp_ pins of the AFPGA.

Signals	Direction (relative to AFPGA)	Purpose	Notes
fmc0_prsnt_m2c_n_i fmc1_prsnt_m2c_n_i	In	FMC0/1 presence detect	
sfp_mod_def0_i	In	SFP presence detect	
sfp_rate_select_o	Out	SFP data rate select	
sfp_tx_fault_i	In	SFP trasmit fault	
sfp_tx_disable_o	Out	SFP transmit disable	
sfp_los_i	In	SFP loss-of-signal detect	
pcbrev_i[5]	In	PCB revision	5 lines
dbg_led_n[4]	Out	Debug LEDs	4 lines
fpgpio2_a2b_o	Out	Front panel GPIO2 direction	
fpgpio1_a2b_o	Out	Front panel GPIO1 direction	
fpgpio34_a2b_o	Out	Front panel GPIO3/4 direction	
term_en_o[4]	Out	Front panel GPIO1..4	4 lines

		termination enable	
fmc0_pg_i fmc1_pg_i	In	FMC power good	2 lines
si57x_oe_o	Out	Si57x oscillator output enable	
fp_led_line_oen_o[2]	Out	LED matrix drive	2 lines
fp_led_line_o[2]	Out	LED matrix drive	2 lines
fp_led_column_o[4]	Out	LED matrix drive	4 lines
ps_fmc_en_12v_o	Out	P12V_FMC load switch	Put in a separate shift register with a separate load input (ioexp_rclk_power_o)
ps_fmc_en_3v3_o	Out	P3V3_FMC load switch	
ps_fmc_en_vadj_o	Out	Vadj regulator enable	
ps_fmc_vadj_sel_1v8_o	Out	Vadj select 1.8V	
ps_fmc_vadj_sel_3v3_o	Out	Vadj select 3.3V	
ps_fmc_vadj_sel_2v5_o	Out	Vadj select 2.5V	
fp_pushbutton_i	In	Front panel button	

2.7. Power supply

- Put a load switch on +3.3V and +12V on both FMC slots allowing the FPGA to switch on/off the payload FMC voltages. Each voltage has to be controlled separately (2 enable lines).
- Allow adjusting IC9 regulator output voltages and on/off state, the voltage has to be controlled from the AFPGA. The user should be able to choose the Vadj from the set of predefined values: +1.8V, +2.5V, +3.3V. By default Vadj should be OFF. Both slots share the same Vadj.
- Adapt supply voltages for the Kintex-7 FPGA (1.0 Vcore/1.2V VGtx)

2.8. FMC Connectors.

- Replace FMC1 connector with a HPC connector. Allocate 4 GTX channels to FMC1 HPC gigabit pins.

2.9. GTX transceivers

Bank	**Channel**	**Purpose**
115	REFCLK0	125 MHz WR clock (from CDCM61004) clk_125m_gtx_i
115	REFCLK1	FMC2 dp_clk_m2c
115	0	WR SFP
115	1	FMC2 (LPC) gigabit link
115	2	GTP1 front panel connector
115	3	GTP2 front panel connector
116	REFCLK0	FMC1 dp_clk_m2c
116	REFCLK1	PLL 125 MHz clock, if available

116	0, 1, 2, 3	FMC1 (HPC) gigabit links, x4

- GTX bank swapping is permitted (confirm this with CERN during layout to check if P&R is happy)
- GTX intra-bank clock and channel swapping is permitted (confirm, please)

2.10. FPGA bank assignment

I/O bank	Voltage	Purpose	Notes
32, 33, 34	1.5 V	DDR3 controller & SFPGA link	Connect Vref/VRN/VRP pins!
14	3.3V	Misc I/O	Requires termination resistor on LVDS inputs
16	3.3V	Misc I/O, mostly P2	Requires termination resistor on LVDS inputs
12, 13, 15	Vadj	FMC I/O	No Vref needed (due to lack of pins).

Swapping within banks (14, 16) and (12, 13, 15) is allowed, except for the clock lines or signals connected to global/regional clock input.

Swapping in the DDR3 bank is allowed within byte groups (i.e. within DQ[0..7], DQ[8..15] etc)

3. Appendixes

SVEC7 HDL repository: https://www.ohwr.org/project/svec/tree/tom-svec7-test

XDC files with pin assignment: `hdl/syn/common/svec7 subdirectory`