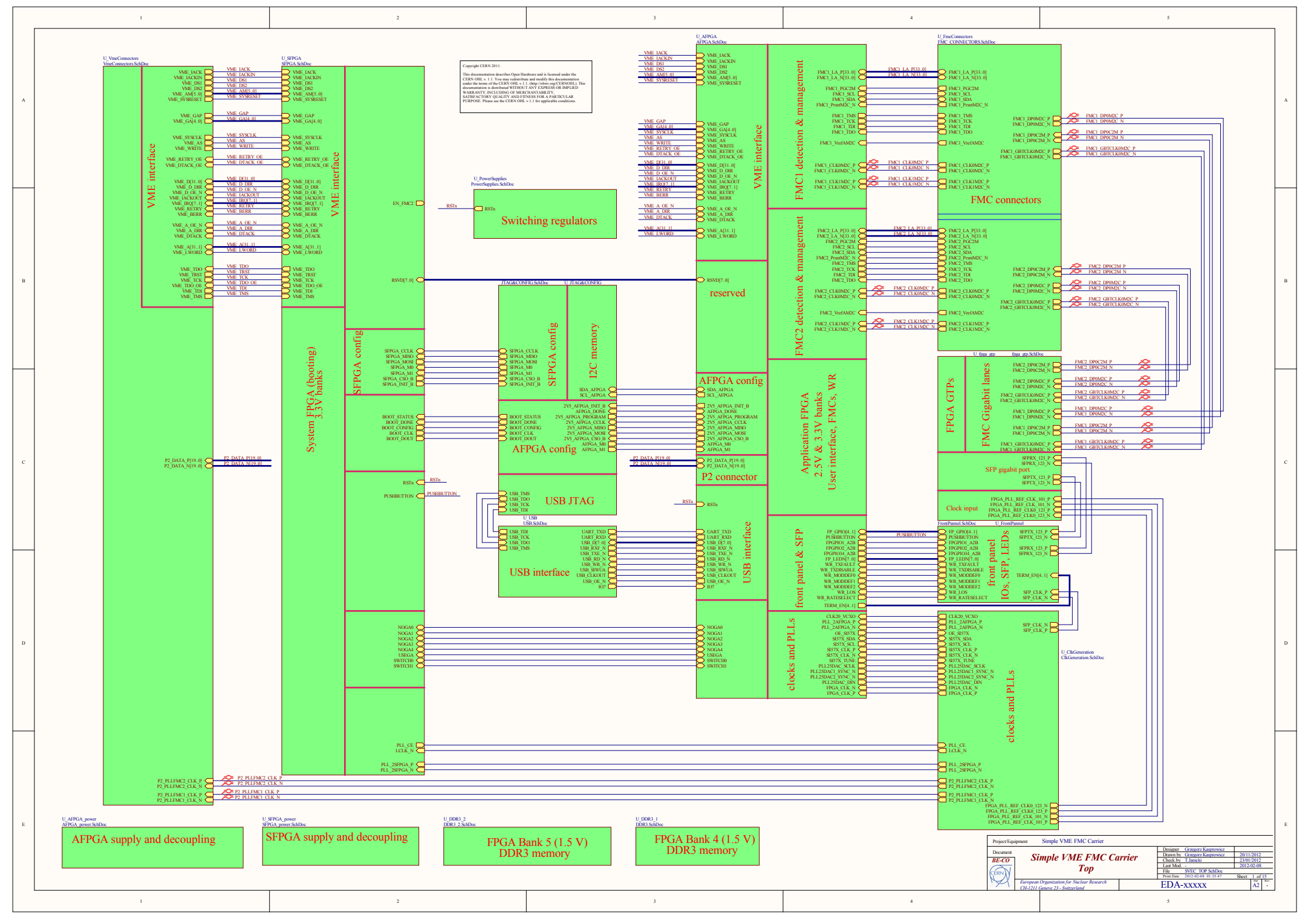
U_VmeConnectors
VmeConnectors.SchDoc
U_SFPGA
SFPGA.SchDoc
VME interface
System FPGA (booting)
3.3V banks
SFPGA config
U_AFPGA
AFPGA.SchDoc
VME interface
reserved
AFPGA config
P2 connector
USB interface
front panel & SFP
clocks and PLLs
Application FPGA
2.5V & 3.3V banks
User interface, FMCs, WR
U_FmcConnectors
FMC_CONNECTORS.SchDoc
FMC1 detection & management
FMC2 detection & management
FMC connectors
FPGA GTPs
FMC Gigabit lanes
U_fpga_gtp
fpga_gtp.SchDoc
SFP gigabit port
Clock input
U_FrontPannel
FrontPannel.SchDoc
front panel
IOs, SFP, LEDs
U_ClkGeneration
ClkGeneration.SchDoc
U_PowerSupplies
PowerSupplies.SchDoc
Switching regulators
JTAG&CONFIG.SchDoc
U_JTAG&CONFIG
I2C memory
U_USB
USB.SchDoc
U_AFPGA_power
AFPGA_power.SchDoc
AFPGA supply and decoupling
U_SFPGA_power
SFPGA_power.SchDoc
SFPGA supply and decoupling
U_DDR3_2
DDR3_2.SchDoc
FPGA Bank 5 (1.5 V)
DDR3 memory
U_DDR3_1
DDR3.SchDoc
FPGA Bank 4 (1.5 V)
DDR3 memory
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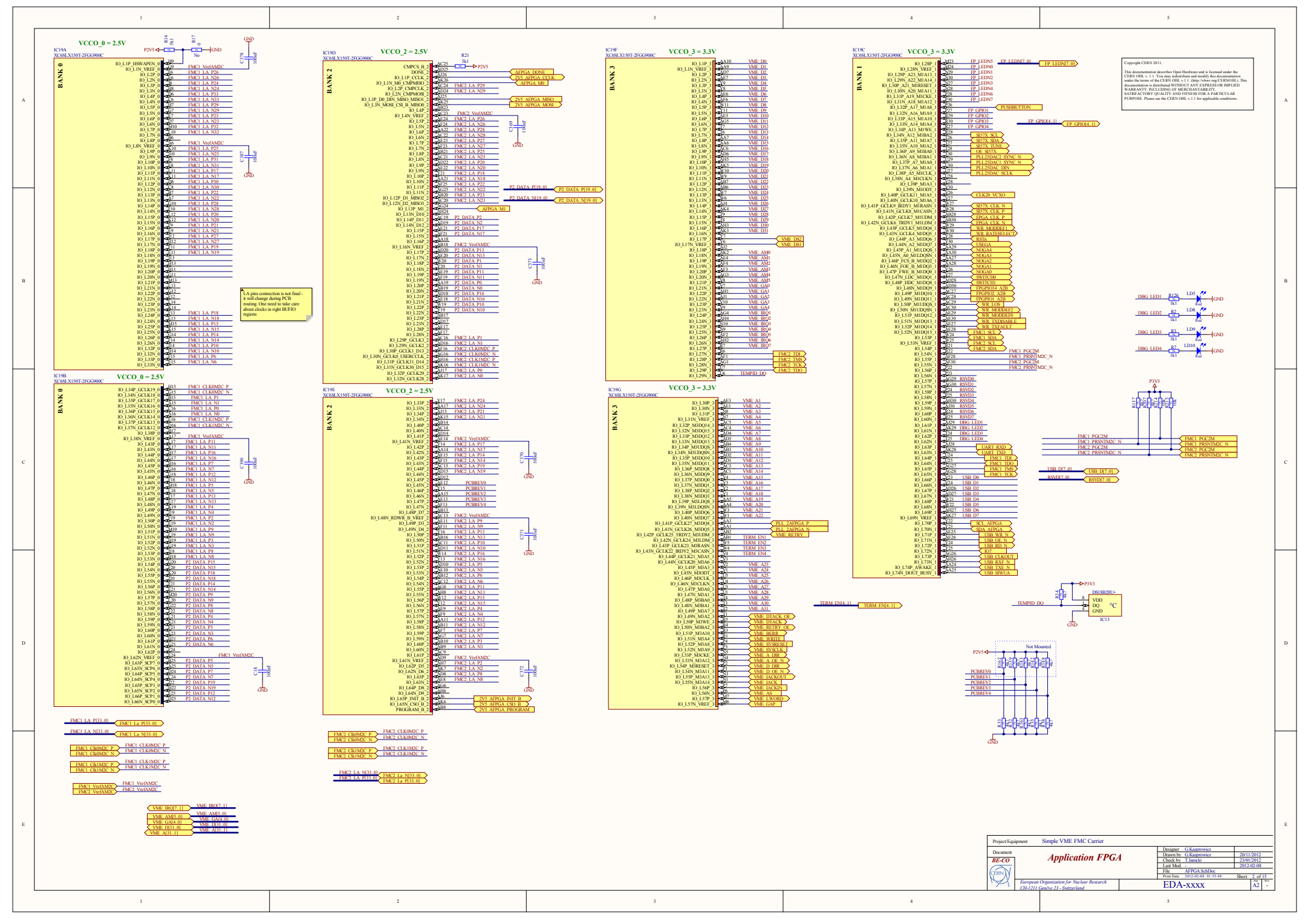
Project/Equipment
Simple VME FMC Carrier
Document
Simple VME FMC Carrier
Top
BE-CO
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer Grzegorz Kasprowicz
Drawn by Grzegorz Kasprowicz
Check by T_Jarocki
Last Mod.
File SVEC_TOP.SchDoc
Print Date 2012-02-08 01:55:47
20/11/2012
23/01/2012
2012-02-08
Sheet 1 of 15
EDA-xxxxx
A2


VCCO_0 = 2.5V
IC19A
XC6SLX150T-2FGG900C
BANK 0
VCCO_0 = 2.5V
IC19B
XC6SLX150T-2FGG900C
BANK 0
VCCO_2 = 2.5V
IC19D
XC6SLX150T-2FGG900C
BANK 2
VCCO_2 = 2.5V
IC19E
XC6SLX150T-2FGG900C
BANK 2
VCCO_3 = 3.3V
IC19F
XC6SLX150T-2FGG900C
BANK 3
VCCO_3 = 3.3V
IC19G
XC6SLX150T-2FGG900C
BANK 3
VCCO_3 = 3.3V
IC19C
XC6SLX150T-2FGG900C
BANK 1
LA pins connection is not final - it will change during PCB routing. One need to take care about clocks in right BUFIO regions
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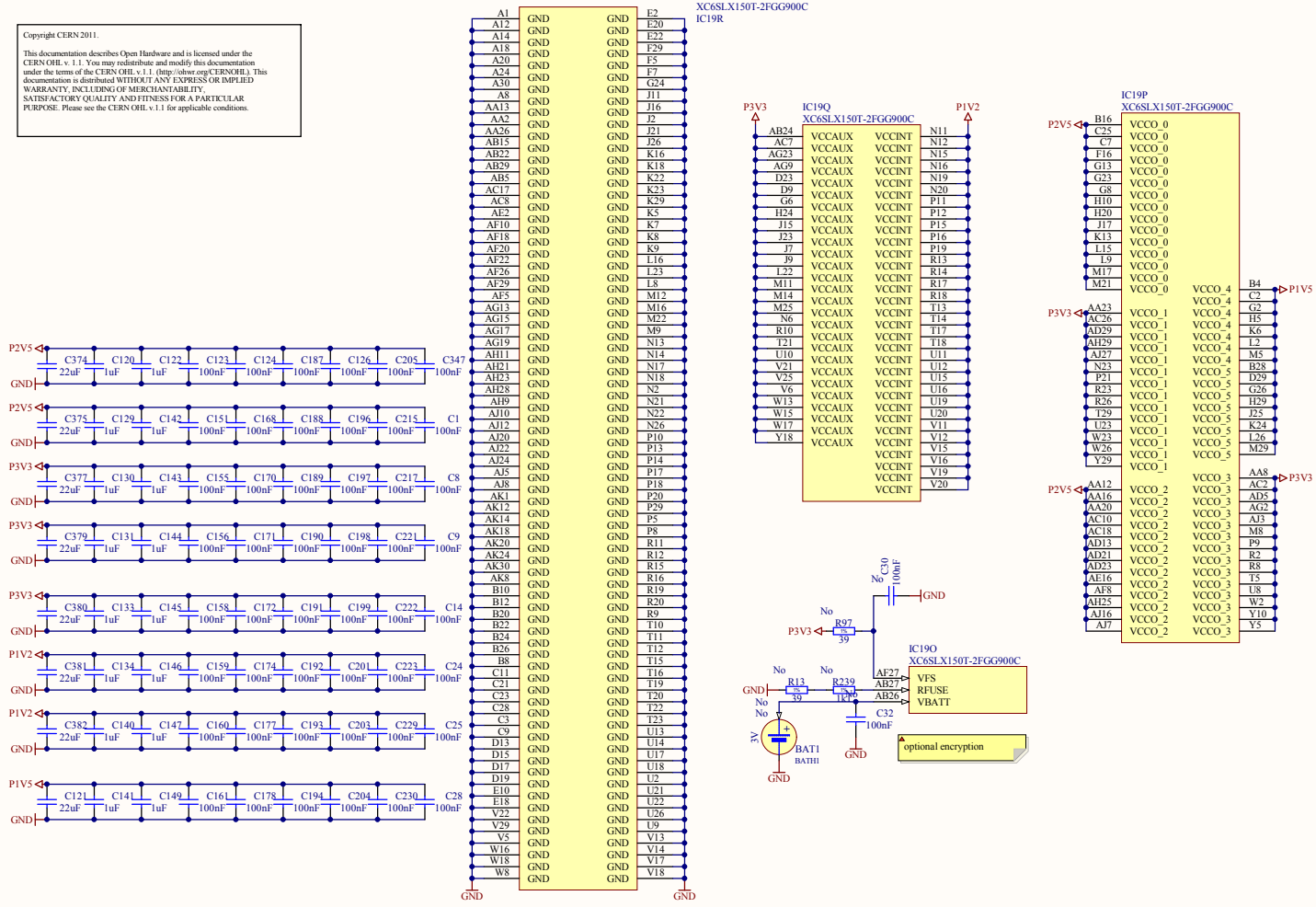
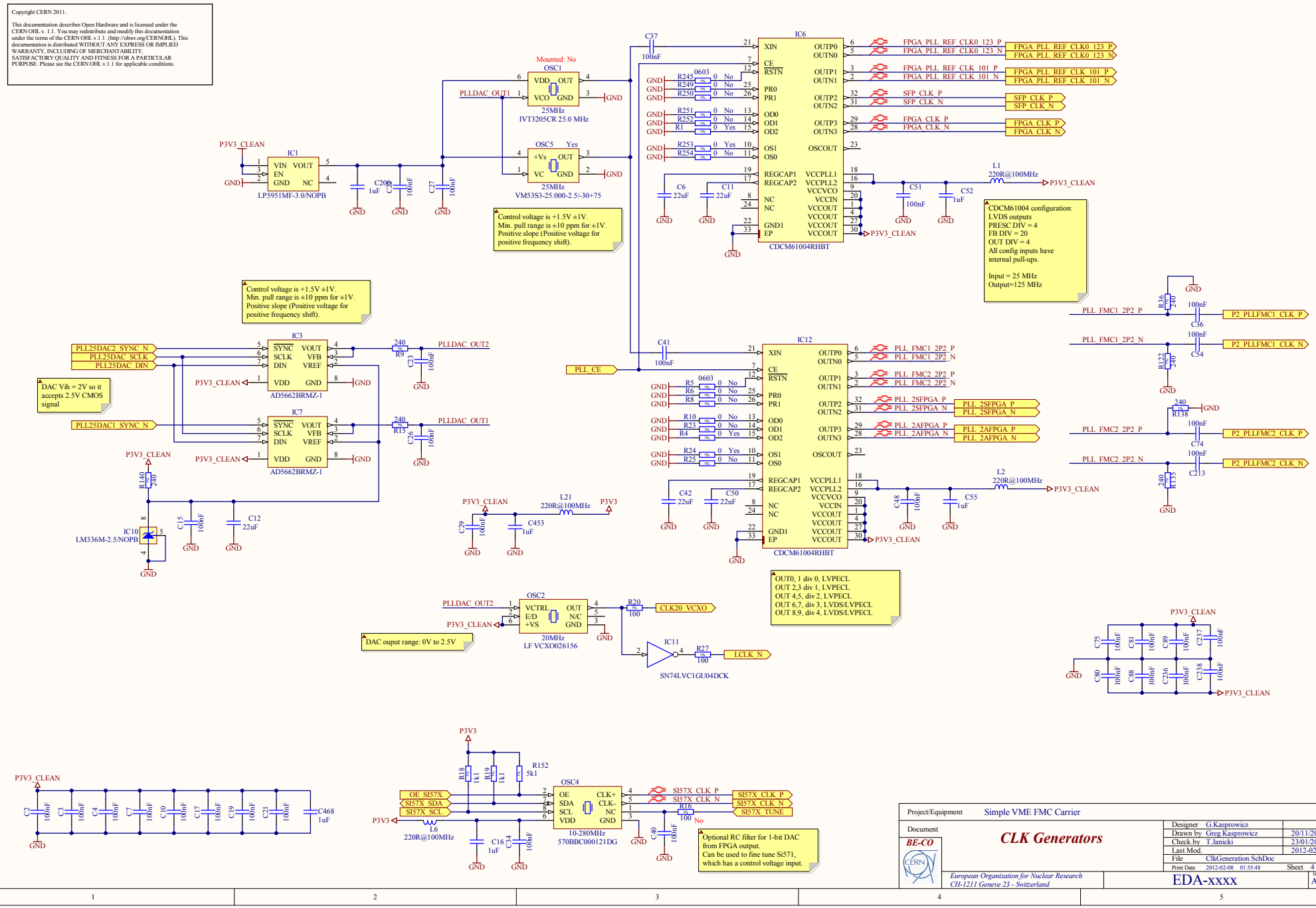
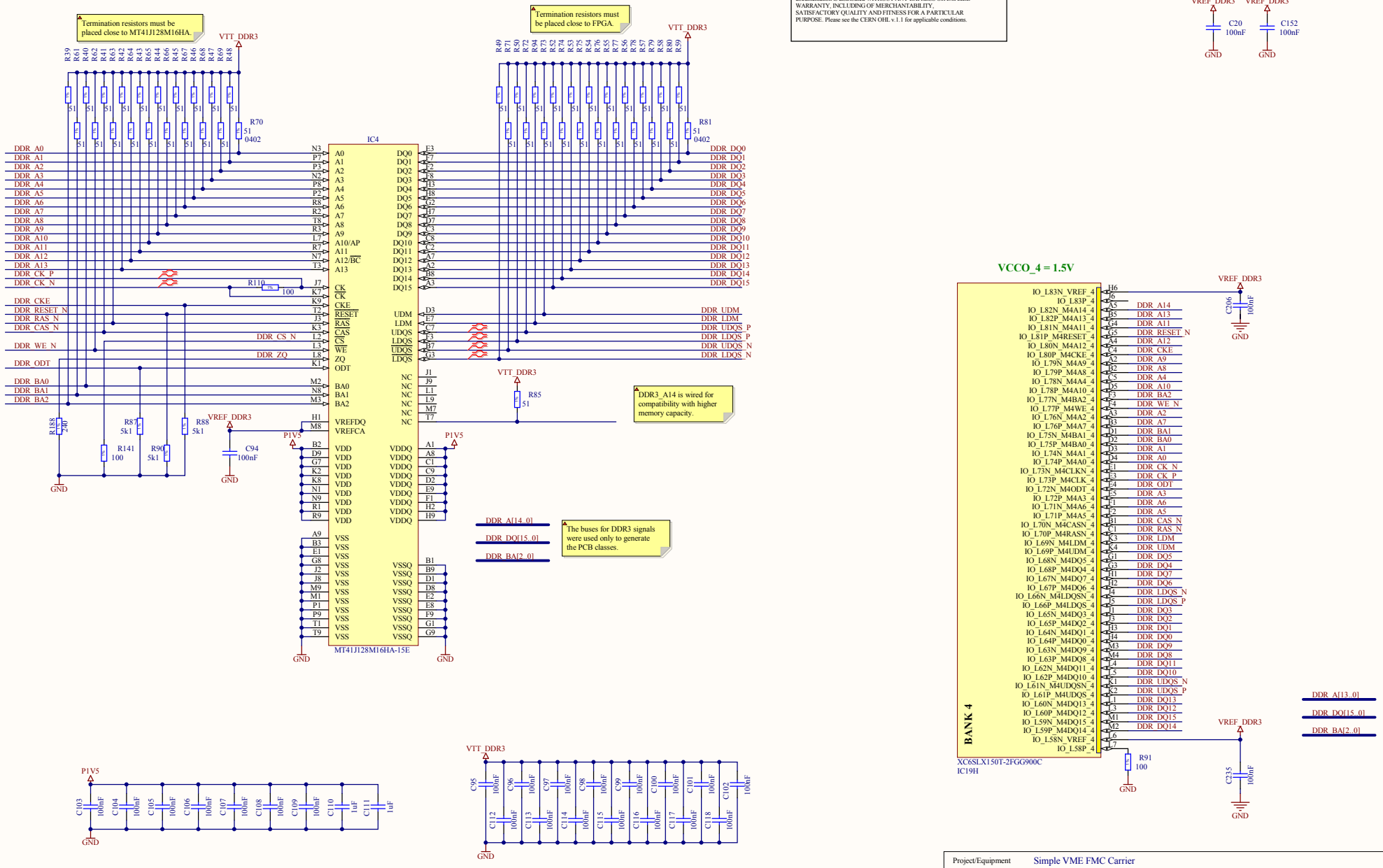
Project/Equipment
Simple VME FMC Carrier
Document
Application FPGA
Designer G.Kasprowicz 20/11/2012
Drawn by G.Kasprowicz 23/01/2012
Check by T.Jarocki
Last Mod. 2012-02-08
File AFPGA.SchDoc
Print Date 2012-02-08 01:55:48
Sheet 2 of 15
EDA-xxxx
A2
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland



Project/Equipment	Simple VME FMC Carrier		
Document	**Application FPGA power supply**	Designer G.Kasprowicz	
		Drawn by Greg Kasprowicz	20/11/2012
		Check by T.Janicki	23/01/2012
		Last Mod.	2012-02-07
		File AFPGA_power.SchDoc	
		Print Date 2012-02-08 01:55:48	Sheet 3 of 15
BE-CO	European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-xxxx	Size A3 / Rev -



Project/Equipment	Simple VME FMC Carrier		
Document	**CLK Generators**	Designer G.Kasprowicz	
BE-CO		Drawn by Greg Kasprowicz	20/11/2012
		Check by T.Janicki	23/01/2012
		Last Mod.	2012-02-08
		File ClkGeneration.SchDoc	
		Print Date 2012-02-08 01:55:48	Sheet 4 of 15
European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-xxxx	Size A3	Rev -



Project/Equipment	Simple VME FMC Carrier
Document	DDR3 memory - bank 4 -
Designer	G.Kasprowicz
Drawn by	G.Kasprowicz 20/11/2012
Check by	T.Janicki 23/01/2012
Last Mod.	- 2012-02-07
File	DDR3.SchDoc
Print Date	2012-02-08 01:55:48
Sheet	5 of 15
Size	A3
Rev	-
	EDA-xxxx

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European Organization for Nuclear Research
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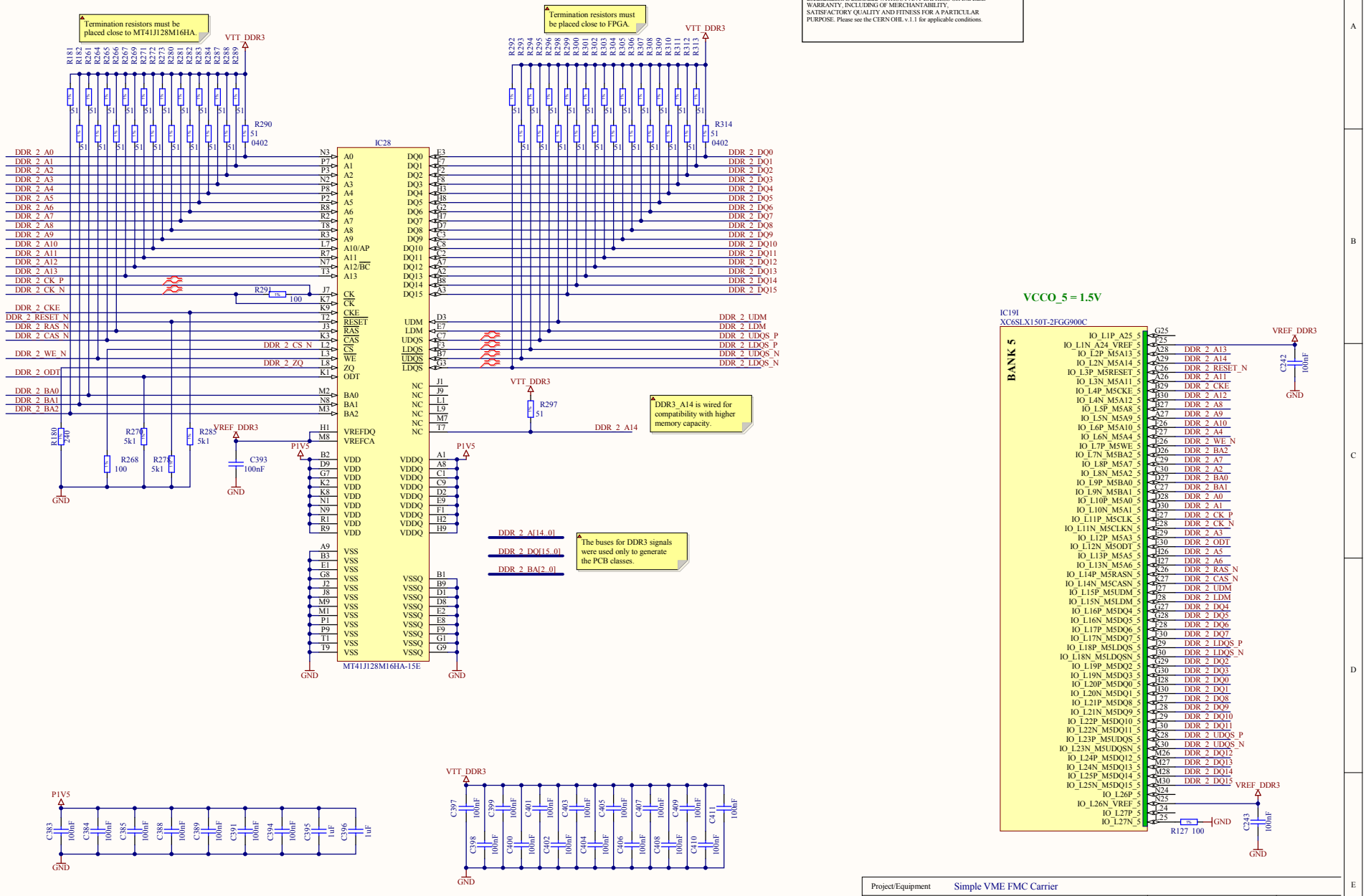
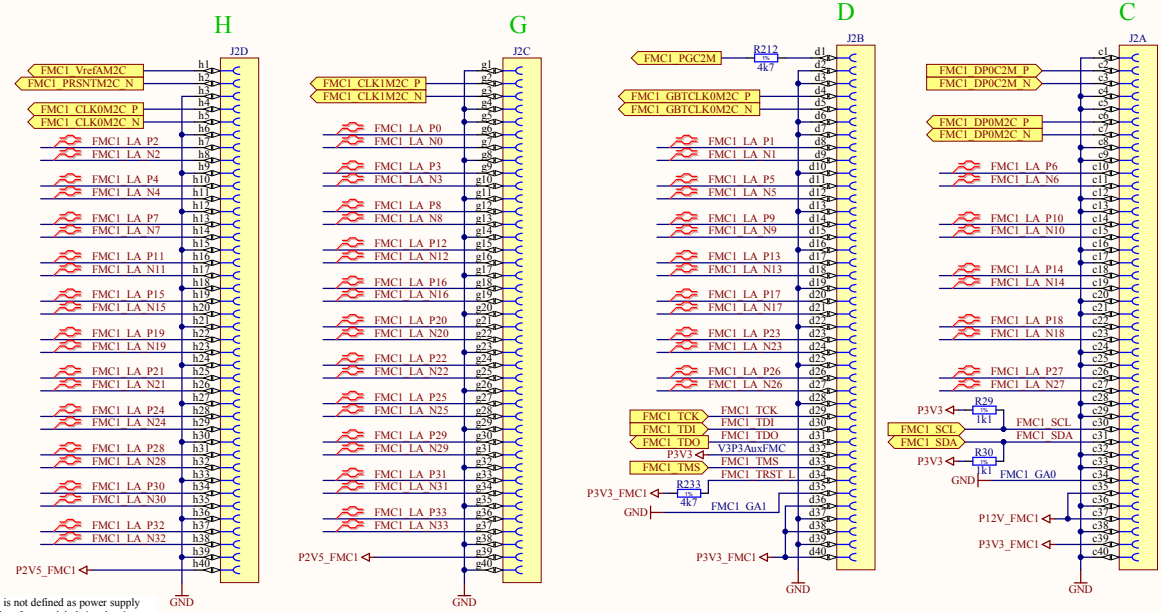


Project/Equipment	Simple VME FMC Carrier		
Document	DDR3 memory - bank 5 -	Designer G.Kasprowicz	
		Drawn by G.Kasprowicz	20/11/2012
		Check by T.Janicki	23/01/2012
		Last Mod. -	2012-02-08
		File DDR3_2.SchDoc	
		Print Date 2012-02-08 01:55:49	Sheet 6 of 15
BE-CO	European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-xxxx	Size A3 / Rev -

FMC slot 1



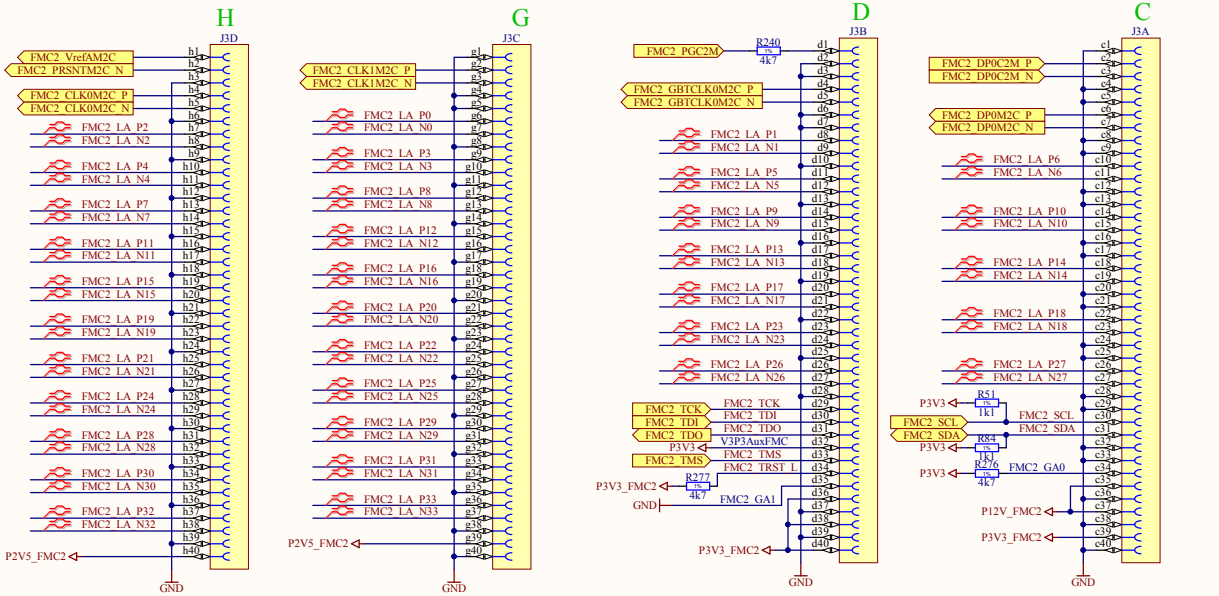
VAdj is not defined as power supply and therefore as global signal as it might differ for the 2 FMC

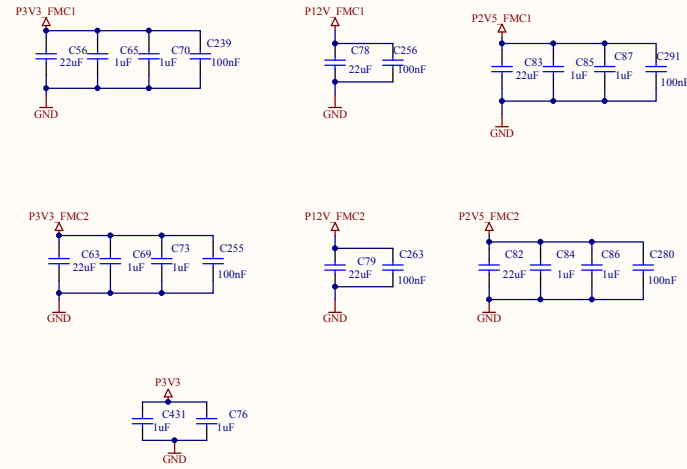
FMC1_LaP and FMC1_LaN are 100ohms diff. pairs

NB: the LVDS pairs must have a differential impedence of 100 ohm and be routed with no skew between the P and the N lines. The skew between the various La pairs should be kept as low as possible.

FMC2_LaP and FMC2_LaN are 100ohms diff. pairs

FMC slot 2





Project/Equipment	Simple VME FMC Carrier		
Document	**FMC Connector**	Designer G.Kasprowicz	
		Drawn by Greg Kasprowicz	20/11/2012
		Check by T.Janicki	23/01/2012
		Last Mod.	2012-02-08
		File FMC_CONNECTORS.SchDoc	
		Print Date 2012-02-08 01:55:49	Sheet 7 of 15
BE-CO	European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-xxxx	Size A3 / Rev -

Power: GTPs power plane, and signal plane should be separated by a ground plane from any signal passing close.

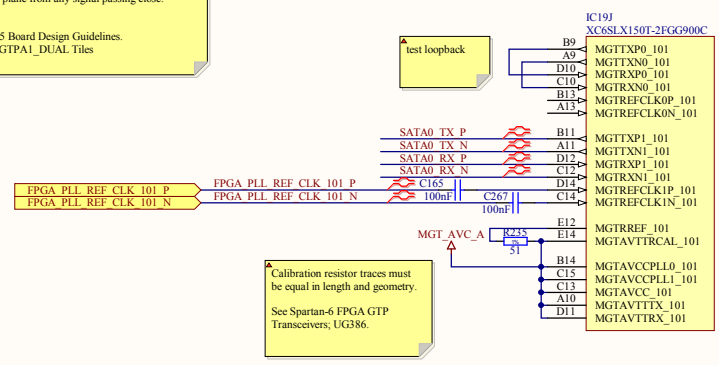
The capacitor bank recomended for decoupling is described in:
Xilinx user guide Spartan-6 FPGA GTP Transceivers (ug386.pdf). Chapter 5 Board Design Guidelines.
Check Table 5-2: Recommended Minimum Decoupling for Spartan-6 FPGA GTPA1_DUAL Tiles
and Figure 5-11: Stackup for GTP Power and Signal Layers.

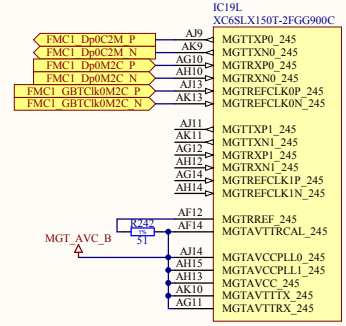
test loopback

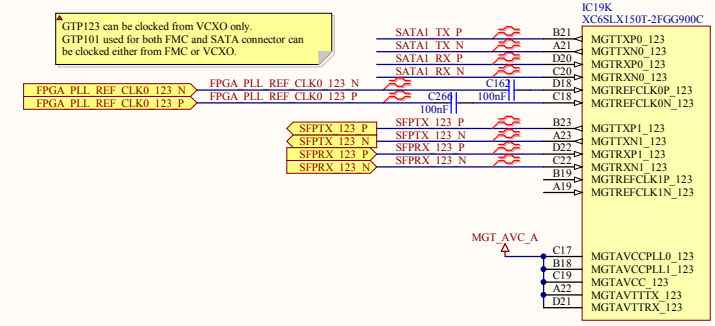
Calibration resistor traces must be equal in length and geometry.

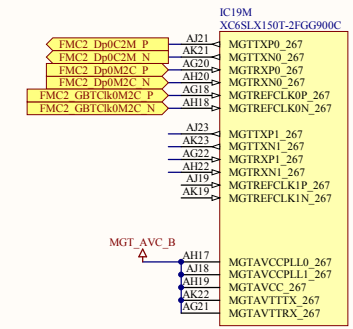
See Spartan-6 FPGA GTP Transceivers; UG386.

GTP123 can be clocked from VCXO only.
GTP101 used for both FMC and SATA connector can be clocked either from FMC or VCXO.

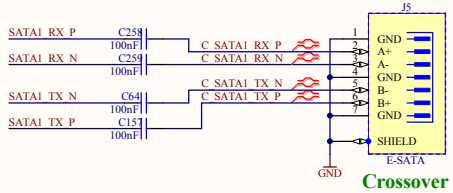




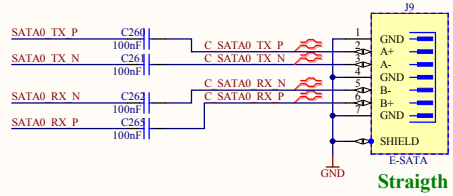




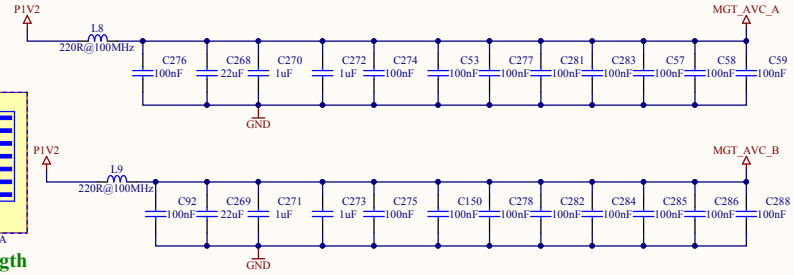
SATA connectors



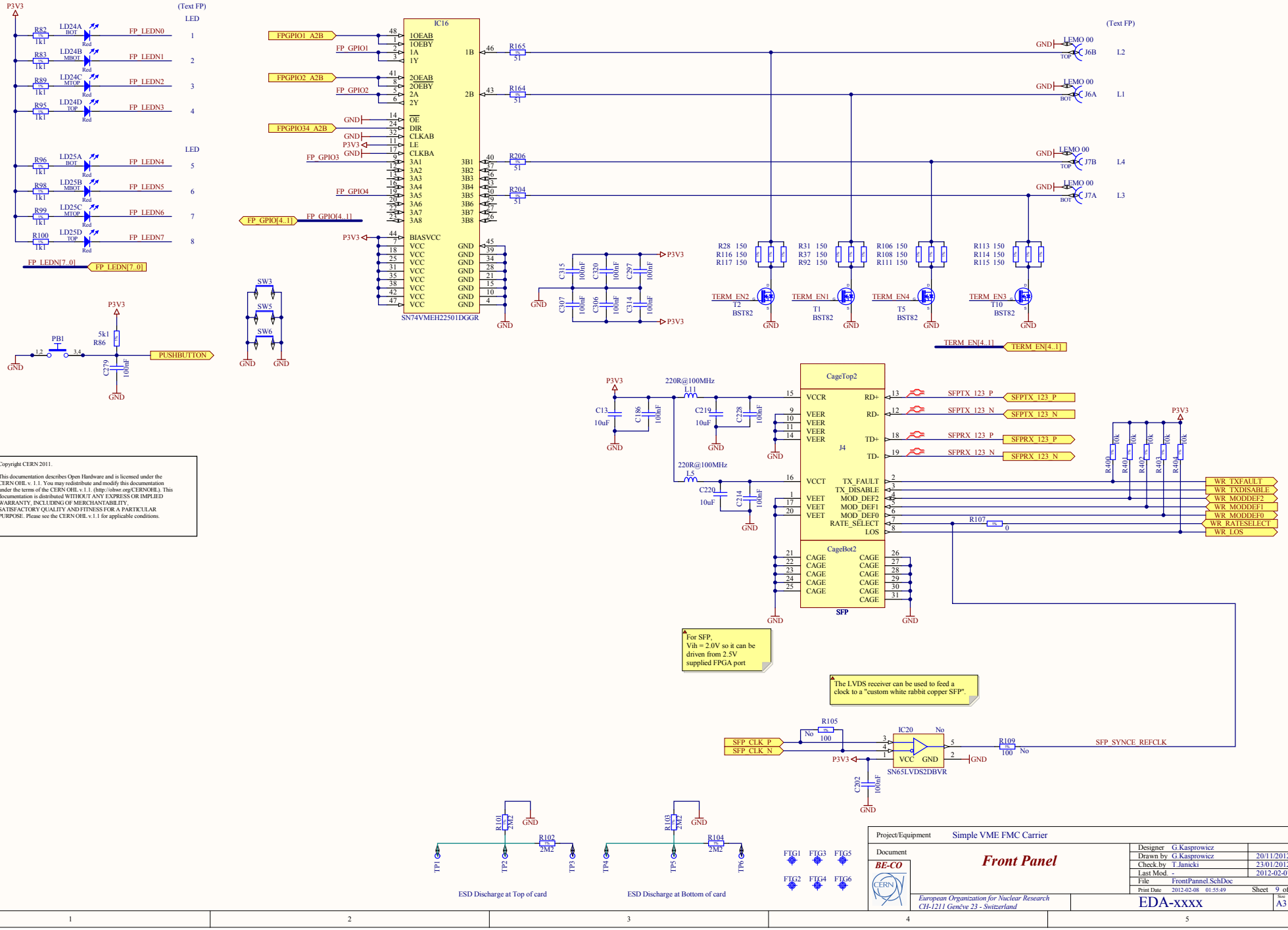
Crossover



Straigth



Project/Equipment	Simple VME FMC Carrier		
Document	**GTP and SATA**	Designer G.Kasprowicz	
BE-CO		Drawn by Greg Kasprowicz	20/11/2012
		Check by T.Janicki	23/01/2012
		Last Mod.	2012-02-07
		File FPGA_GTP.SchDoc	
		Print Date 2012-02-08 01:55:49	Sheet 8 of 15
European Organization for Nuclear Research, CH-1211 Geneve 23 - Switzerland	EDA-xxxx	Size A3	Rev -



Project/Equipment: Simple VME FMC Carrier

Document: **Front Panel**

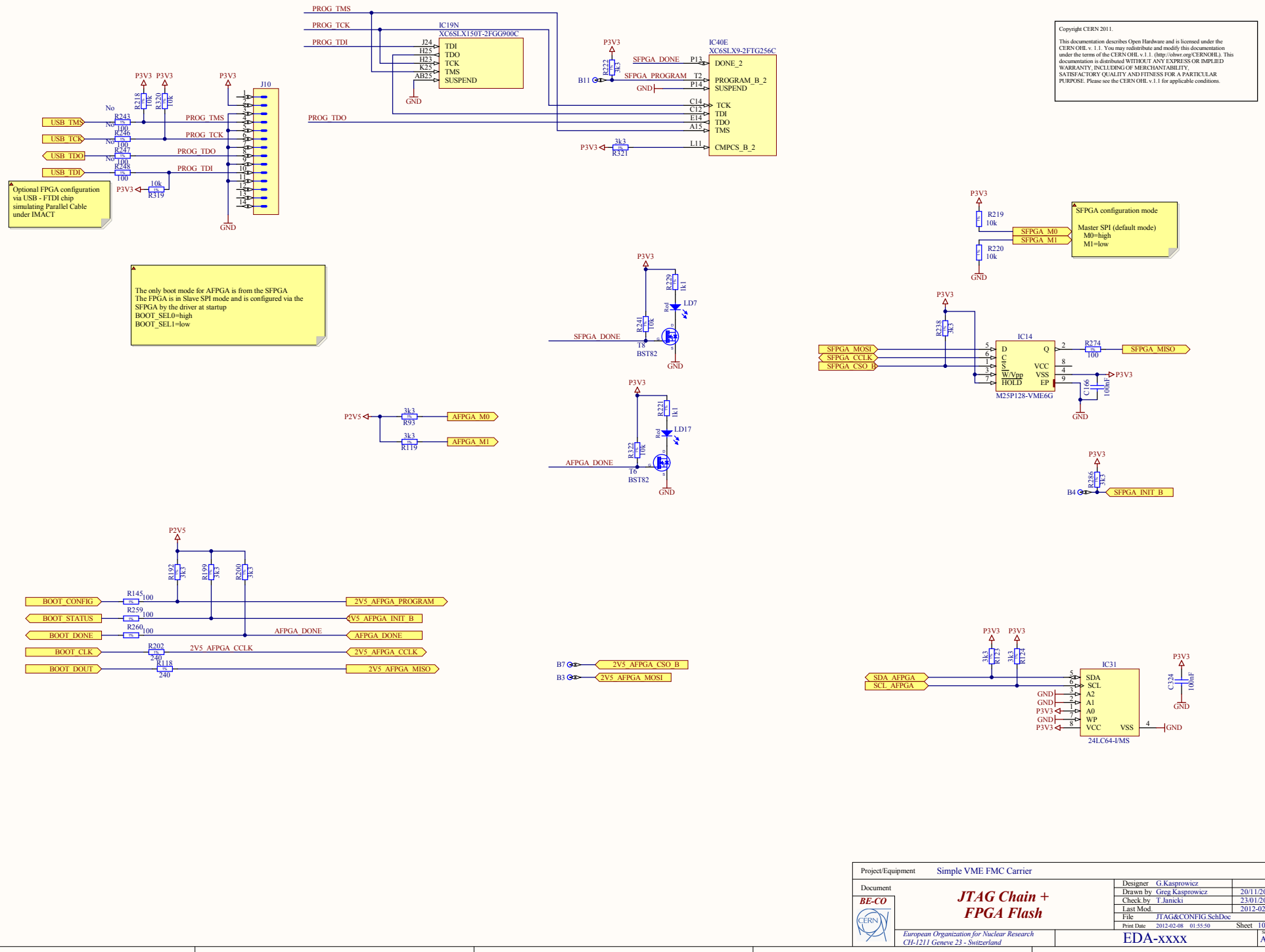
BE-CO

Designer	G.Kasprowicz	
Drawn by	G.Kasprowicz	20/11/2012
Check by	T.Janicki	23/01/2012
Last Mod.	-	2012-02-07
File	FrontPannel.SchDoc	
Print Date	2012-02-08 01:55:49	Sheet 9 of 15

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

EDA-xxxx

Size A3 | Rev -



Project/Equipment	Simple VME FMC Carrier	
Document	JTAG Chain + FPGA Flash	
BE-CO	Designer G.Kasprowicz	
	Drawn by Greg Kasprowicz	20/11/2012
	Check by T.Janicki	23/01/2012
	Last Mod.	2012-02-08
	File JTAG&CONFIG.SchDoc	
	Print Date 2012-02-08 01:55:50	Sheet 10 of 15
European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-xxxx	Size A3 / Rev -

Vref = 0.765V
Vout / Vref = 1.53V
tolerance = 1%Vout / Vref = 2.000
(Vout / Vref) - 1 = 1.000 = R1 / R2

R1 = 100.0?	R2 = 100.0?	Ir = 7.650mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 110.0?	R2 = 110.0?	Ir = 6.955mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 120.0?	R2 = 120.0?	Ir = 6.375mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 130.0?	R2 = 130.0?	Ir = 5.885mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 150.0?	R2 = 150.0?	Ir = 5.100mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 160.0?	R2 = 160.0?	Ir = 4.781mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 180.0?	R2 = 180.0?	Ir = 4.250mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 200.0?	R2 = 200.0?	Ir = 3.825mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 220.0?	R2 = 220.0?	Ir = 3.477mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 240.0?	R2 = 240.0?	Ir = 3.188mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 270.0?	R2 = 270.0?	Ir = 2.833mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 300.0?	R2 = 300.0?	Ir = 2.550mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 330.0?	R2 = 330.0?	Ir = 2.318mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 360.0?	R2 = 360.0?	Ir = 2.125mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 390.0?	R2 = 390.0?	Ir = 1.962mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 430.0?	R2 = 430.0?	Ir = 1.779mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%
R1 = 470.0?	R2 = 470.0?	Ir = 1.628mA	Vout = 1.530V	R1/R2 = 1.000	Rerror = 0.00%

Power estimation:

P1V2
AFPGA 3A
SFPGA 500mA

P1V5
AFPGA 1A + 2x DDR3 (max 2x 530mW)
(http://download.micron.com/pdf/technotes/ddr3/TN41_01DDR3%20Power.pdf)
estimated power from P1V5 is about 1.5A

P2V5
AFPGA 2A

P2V5_FMC1
FMC slot 2A (HPC - 4A, LPC - 2A)

P2V5_FMC2
FMC slot 2A (HPC - 4A, LPC - 2A)

P3V3_FMC1
FMC slot 2A

Vref = 0.765V
Vout / Vref = 1.2V
tolerance = 1%Vout / Vref = 1.569
(Vout / Vref) - 1 = 0.569 = R1 / R2

R1 = 220.0?	R2 = 390.0?	Ir = 1.962mA	Vout = 1.197V	R1/R2 = 0.564	Rerror = 0.80%
R1 = 390.0?	R2 = 680.0?	Ir = 1.125mA	Vout = 1.204V	R1/R2 = 0.574	Rerror = 0.86%
R1 = 430.0?	R2 = 750.0?	Ir = 1.020mA	Vout = 1.204V	R1/R2 = 0.573	Rerror = 0.83%
R1 = 470.0?	R2 = 820.0?	Ir = 0.933mA	Vout = 1.203V	R1/R2 = 0.573	Rerror = 0.80%
R1 = 620.0?	R2 = 1100.0?	Ir = 0.695mA	Vout = 1.196V	R1/R2 = 0.564	Rerror = 0.88%
R1 = 680.0?	R2 = 1200.0?	Ir = 0.638mA	Vout = 1.199V	R1/R2 = 0.567	Rerror = 0.34%
R1 = 910.0?	R2 = 1600.0?	Ir = 0.478mA	Vout = 1.200V	R1/R2 = 0.569	Rerror = 0.02%

Vref = 0.765V
Vout / Vref = 2.5V
tolerance = 1%Vout / Vref = 3.268
(Vout / Vref) - 1 = 2.268 = R1 / R2

R1 = 2700.0?	R2 = 1200.0?	Ir = 0.638mA	Vout = 2.486V	R1/R2 = 2.250	Rerror = 0.79%
R1 = 3600.0?	R2 = 1600.0?	Ir = 0.478mA	Vout = 2.486V	R1/R2 = 2.250	Rerror = 0.79%
R1 = 6800.0?	R2 = 3000.0?	Ir = 0.255mA	Vout = 2.499V	R1/R2 = 2.267	Rerror = 0.06%
R1 = 7500.0?	R2 = 3300.0?	Ir = 0.232mA	Vout = 2.504V	R1/R2 = 2.273	Rerror = 0.21%
R1 = 8200.0?	R2 = 3600.0?	Ir = 0.213mA	Vout = 2.508V	R1/R2 = 2.278	Rerror = 0.43%

LAYOUT NOTES:
· Place the input capacitor close to the top switching FET. The output current loop should also be kept as small as possible.
· Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions Kelvin connections should be brought from the output to the feedback pin (FBx) of the device.
· Make a single point connection from the signal ground to power ground
· Do not allow switching current to flow under the device

DC/DC calculations,Voripple=30mV
2.5V,Imax=5.4A, L=1uH, Rtrip = 5670, C=50uF, ILpeak=3.75
1.2V,Imax=4A, L=1uH, Rtrip=4200,C=80,ILpeak=6A
2.5V,Imax=4A, L=1uH, Rtrip = 4200, C=80uF, ILpeak=6
1.5V,Imax=4A, L=1uH, Rtrip=4200, C=33uF,ILpeak=6A

2.5V 6A supply for FMCs

2.5V 2,5A, supply of AFPGA IO for FMCs

1.5V 1.7A, supply of DDR memories, DDR IO bank

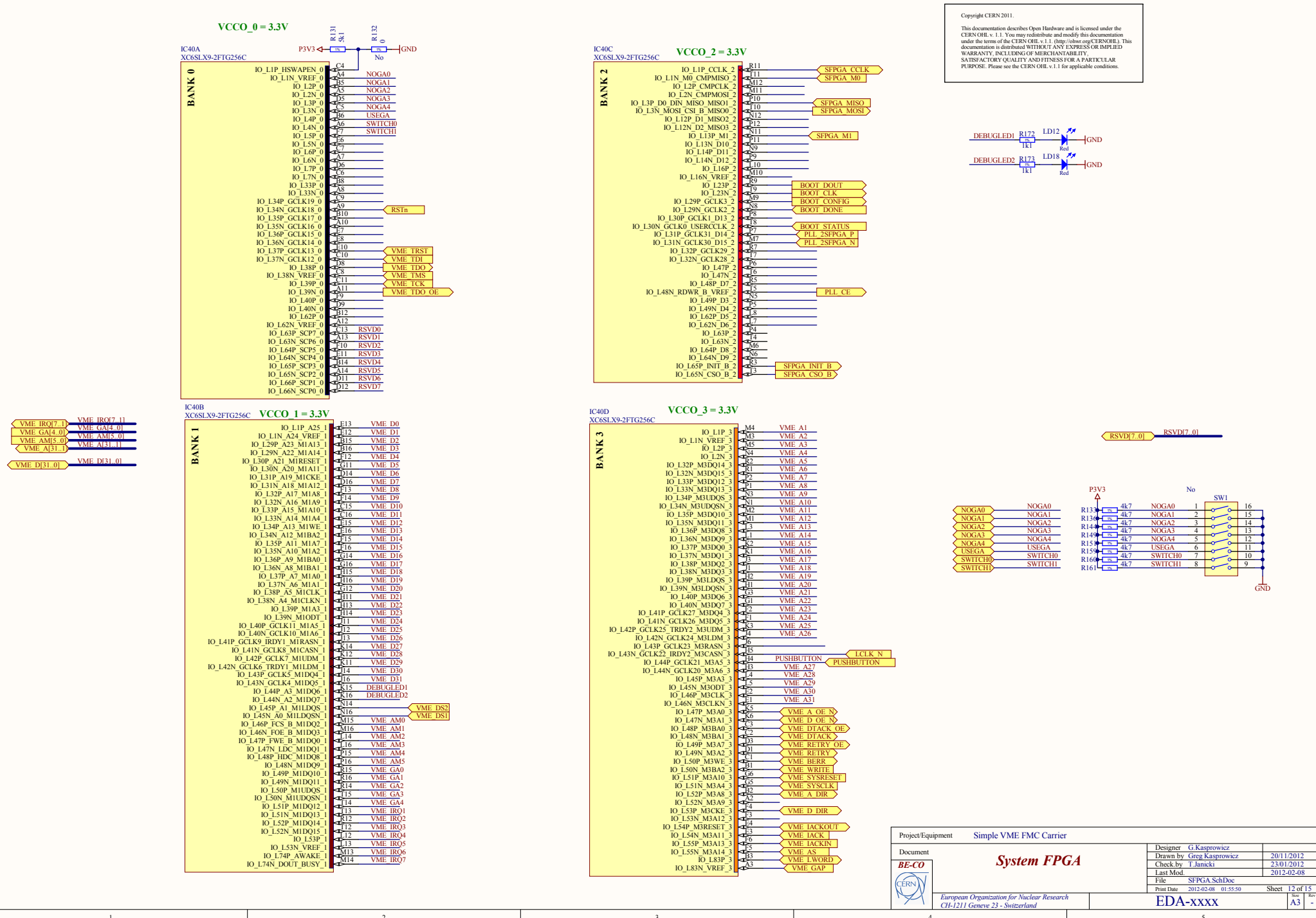
1.2V 4A, supply of FPGA cores

Project/Equipment	Simple PCIe Carrier Board
Document	Switching power supply
Designer	GK, MC, TW, EB, PAS
Drawn by	Greg Kasprowicz 10/07/2010
Check by	MC, TW, EB 11/05/2011
Last Mod.	TW, MC 2012-02-08
File	PowerSupplies.SchDoc
Print Date	2012-02-08 01:55:50 Sheet 11 of 15
Size	A3
Rev	-

BE-CO

European Organization for Nuclear Research
CH-1211 Geneve 23 - SwitzerLA Pd

EDA-02189-V4-0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IC40A
XC6SLX9-2FTG256C
BANK 0
R131 5k1
R132 0
P3V3
GND
No
IO_L1P_HSWAPEN_0
IO_L1N_VREF_0
IO_L2P_0
IO_L2N_0
IO_L3P_0
IO_L3N_0
IO_L4P_0
IO_L4N_0
IO_L5P_0
IO_L5N_0
IO_L6P_0
IO_L6N_0
IO_L7P_0
IO_L7N_0
IO_L33P_0
IO_L33N_0
IO_L34P_GCLK19_0
IO_L34N_GCLK18_0
IO_L35P_GCLK17_0
IO_L35N_GCLK16_0
IO_L36P_GCLK15_0
IO_L36N_GCLK14_0
IO_L37P_GCLK13_0
IO_L37N_GCLK12_0
IO_L38P_0
IO_L38N_VREF_0
IO_L39P_0
IO_L39N_0
IO_L40P_0
IO_L40N_0
IO_L62P_0
IO_L62N_VREF_0
IO_L63P_SCP7_0
IO_L63N_SCP6_0
IO_L64P_SCP5_0
IO_L64N_SCP4_0
IO_L65P_SCP3_0
IO_L65N_SCP2_0
IO_L66P_SCP1_0
IO_L66N_SCP0_0
NOGA0
NOGA1
NOGA2
NOGA3
NOGA4
USEGA
SWITCH0
SWITCH1
RSTn
VME_TRST
VME_TDI
VME_TDO
VME_TMS
VME_TCK
VME_TDO_OE
RSVD0
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
IC40B
XC6SLX9-2FTG256C
VCCO_1 = 3.3V
BANK 1
IO_L1P_A25_1
IO_L1N_A24_VREF_1
IO_L29P_A23_M1A13_1
IO_L29N_A22_M1A14_1
IO_L30P_A21_M1RESET_1
IO_L30N_A20_M1A11_1
IO_L31P_A19_M1CKE_1
IO_L31N_A18_M1A12_1
IO_L32P_A17_M1A8_1
IO_L32N_A16_M1A9_1
IO_L33P_A15_M1A10_1
IO_L33N_A14_M1A4_1
IO_L34P_A13_M1WE_1
IO_L34N_A12_M1BA2_1
IO_L35P_A11_M1A7_1
IO_L35N_A10_M1A2_1
IO_L36P_A9_M1BA0_1
IO_L36N_A8_M1BA1_1
IO_L37P_A7_M1A0_1
IO_L37N_A6_M1A1_1
IO_L38P_A5_M1CLK_1
IO_L38N_A4_M1CLKN_1
IO_L39P_M1A3_1
IO_L39N_M1ODT_1
IO_L40P_GCLK11_M1A5_1
IO_L40N_GCLK10_M1A6_1
IO_L41P_GCLK9_IRDY1_M1RASN_1
IO_L41N_GCLK8_M1CASN_1
IO_L42P_GCLK7_M1UDM_1
IO_L42N_GCLK6_TRDY1_M1LDM_1
IO_L43P_GCLK5_M1DQ4_1
IO_L43N_GCLK4_M1DQ5_1
IO_L44P_A3_M1DQ6_1
IO_L44N_A2_M1DQ7_1
IO_L45P_A1_M1LDQS_1
IO_L45N_A0_M1LDQSN_1
IO_L46P_FCS_B_M1DQ2_1
IO_L46N_FOE_B_M1DQ3_1
IO_L47P_FWE_B_M1DQ0_1
IO_L47N_LDC_M1DQ1_1
IO_L48P_HDC_M1DQ8_1
IO_L48N_M1DQ9_1
IO_L49P_M1DQ10_1
IO_L49N_M1DQ11_1
IO_L50P_M1UDQS_1
IO_L50N_M1UDQSN_1
IO_L51P_M1DQ12_1
IO_L51N_M1DQ13_1
IO_L52P_M1DQ14_1
IO_L52N_M1DQ15_1
IO_L53P_1
IO_L53N_VREF_1
IO_L74P_AWAKE_1
IO_L74N_DOUT_BUSY_1
VME_D0
VME_D1
VME_D2
VME_D3
VME_D4
VME_D5
VME_D6
VME_D7
VME_D8
VME_D9
VME_D10
VME_D11
VME_D12
VME_D13
VME_D14
VME_D15
VME_D16
VME_D17
VME_D18
VME_D19
VME_D20
VME_D21
VME_D22
VME_D23
VME_D24
VME_D25
VME_D26
VME_D27
VME_D28
VME_D29
VME_D30
VME_D31
DEBUGLED1
DEBUGLED2
VME_DS2
VME_DS1
VME_AM0
VME_AM1
VME_AM2
VME_AM3
VME_AM4
VME_AM5
VME_GA0
VME_GA1
VME_GA2
VME_GA3
VME_GA4
VME_IRQ1
VME_IRQ2
VME_IRQ3
VME_IRQ4
VME_IRQ5
VME_IRQ6
VME_IRQ7
VME_IRQ[7..1]
VME_GA[4..0]
VME_AM[5..0]
VME_A[31..1]
VME_D[31..0]
IC40C
XC6SLX9-2FTG256C
VCCO_2 = 3.3V
BANK 2
IO_L1P_CCLK_2
IO_L1N_M0_CMPMISO_2
IO_L2P_CMPCLK_2
IO_L2N_CMPMOSI_2
IO_L3P_D0_DIN_MISO_MISO1_2
IO_L3N_MOSI_CSI_B_MISO0_2
IO_L12P_D1_MISO2_2
IO_L12N_D2_MISO3_2
IO_L13P_M1_2
IO_L13N_D10_2
IO_L14P_D11_2
IO_L14N_D12_2
IO_L16P_2
IO_L16N_VREF_2
IO_L23P_2
IO_L23N_2
IO_L29P_GCLK3_2
IO_L29N_GCLK2_2
IO_L30P_GCLK1_D13_2
IO_L30N_GCLK0_USERCCLK_2
IO_L31P_GCLK31_D14_2
IO_L31N_GCLK30_D15_2
IO_L32P_GCLK29_2
IO_L32N_GCLK28_2
IO_L47P_2
IO_L47N_2
IO_L48P_D7_2
IO_L48N_RDWR_B_VREF_2
IO_L49P_D3_2
IO_L49N_D4_2
IO_L62P_D5_2
IO_L62N_D6_2
IO_L63P_2
IO_L63N_2
IO_L64P_D8_2
IO_L64N_D9_2
IO_L65P_INIT_B_2
IO_L65N_CSO_B_2
SFPGA_CCLK
SFPGA_M0
SFPGA_MISO
SFPGA_MOSI
SFPGA_M1
BOOT_DOUT
BOOT_CLK
BOOT_CONFIG
BOOT_DONE
BOOT_STATUS
PLL_2SFPGA_P
PLL_2SFPGA_N
PLL_CE
SFPGA_INIT_B
SFPGA_CSO_B
IC40D
XC6SLX9-2FTG256C
VCCO_3 = 3.3V
BANK 3
IO_L1P_3
IO_L1N_VREF_3
IO_L2P_3
IO_L2N_3
IO_L32P_M3DQ14_3
IO_L32N_M3DQ15_3
IO_L33P_M3DQ12_3
IO_L33N_M3DQ13_3
IO_L34P_M3UDQS_3
IO_L34N_M3UDQSN_3
IO_L35P_M3DQ10_3
IO_L35N_M3DQ11_3
IO_L36P_M3DQ8_3
IO_L36N_M3DQ9_3
IO_L37P_M3DQ0_3
IO_L37N_M3DQ1_3
IO_L38P_M3DQ2_3
IO_L38N_M3DQ3_3
IO_L39P_M3LDQS_3
IO_L39N_M3LDQSN_3
IO_L40P_M3DQ6_3
IO_L40N_M3DQ7_3
IO_L41P_GCLK27_M3DQ4_3
IO_L41N_GCLK26_M3DQ5_3
IO_L42P_GCLK25_TRDY2_M3UDM_3
IO_L42N_GCLK24_M3LDM_3
IO_L43P_GCLK23_M3RASN_3
IO_L43N_GCLK22_IRDY2_M3CASN_3
IO_L44P_GCLK21_M3A5_3
IO_L44N_GCLK20_M3A6_3
IO_L45P_M3A3_3
IO_L45N_M3ODT_3
IO_L46P_M3CLK_3
IO_L46N_M3CLKN_3
IO_L47P_M3A0_3
IO_L47N_M3A1_3
IO_L48P_M3BA0_3
IO_L48N_M3BA1_3
IO_L49P_M3A7_3
IO_L49N_M3A2_3
IO_L50P_M3WE_3
IO_L50N_M3BA2_3
IO_L51P_M3A10_3
IO_L51N_M3A4_3
IO_L52P_M3A8_3
IO_L52N_M3A9_3
IO_L53P_M3CKE_3
IO_L53N_M3A12_3
IO_L54P_M3RESET_3
IO_L54N_M3A11_3
IO_L55P_M3A13_3
IO_L55N_M3A14_3
IO_L83P_3
IO_L83N_VREF_3
VME_A1
VME_A2
VME_A3
VME_A4
VME_A5
VME_A6
VME_A7
VME_A8
VME_A9
VME_A10
VME_A11
VME_A12
VME_A13
VME_A14
VME_A15
VME_A16
VME_A17
VME_A18
VME_A19
VME_A20
VME_A21
VME_A22
VME_A23
VME_A24
VME_A25
VME_A26
LCLK_N
PUSHBUTTON
VME_A27
VME_A28
VME_A29
VME_A30
VME_A31
VME_A_OE_N
VME_D_OE_N
VME_DTACK_OE
VME_DTACK
VME_RETRY_OE
VME_RETRY
VME_BERR
VME_WRITE
VME_SYSRESET
VME_SYSCLK
VME_A_DIR
VME_D_DIR
VME_IACKOUT
VME_IACK
VME_IACKIN
VME_AS
VME_LWORD
VME_GAP
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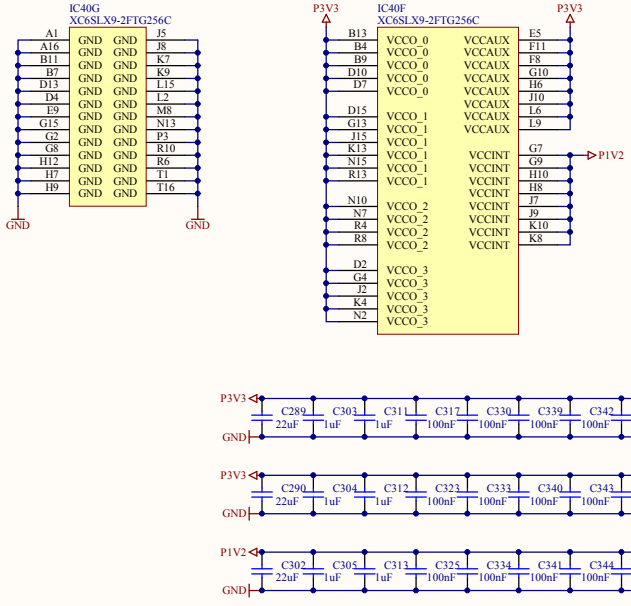
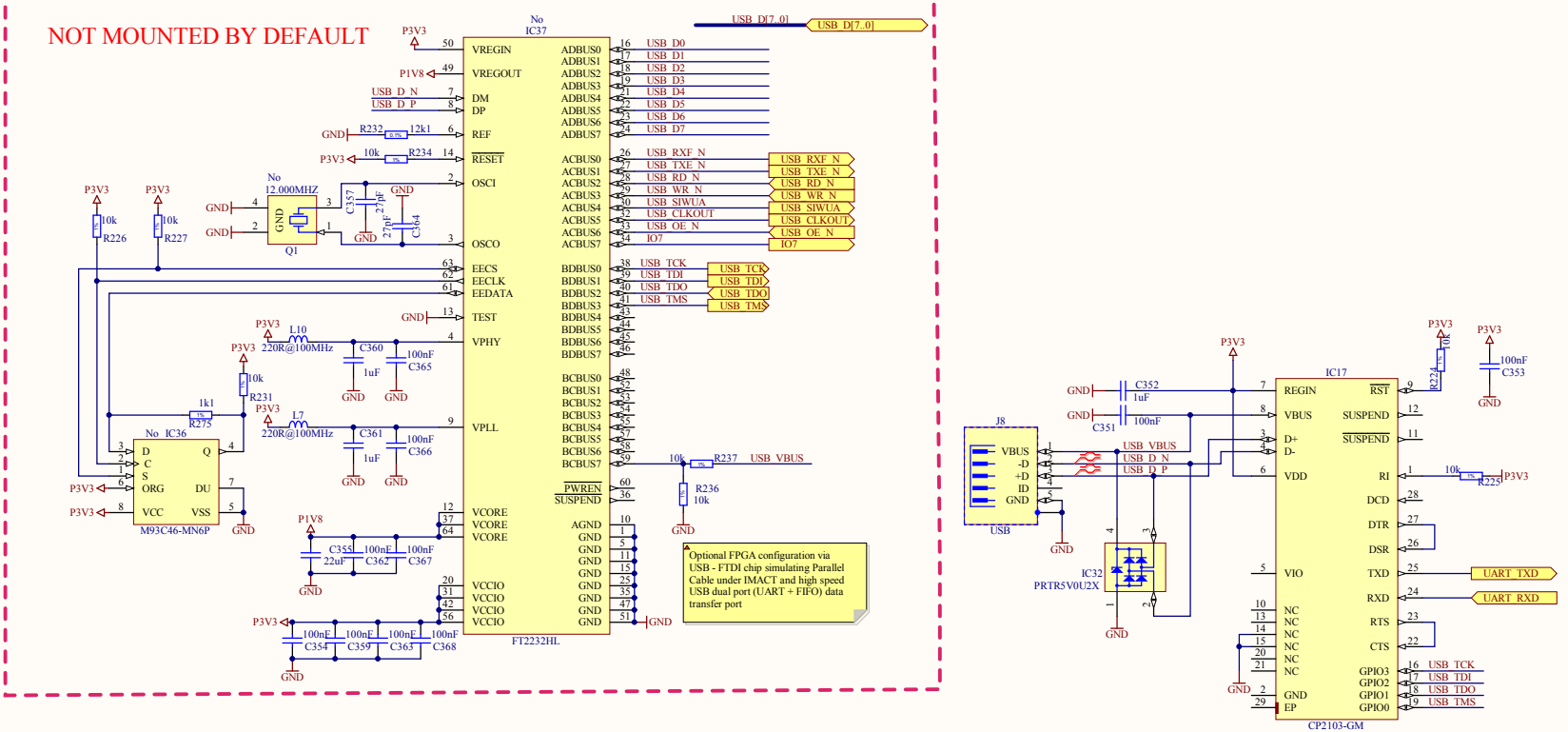
DEBUGLED1
DEBUGLED2
R172 1k1
R173 1k1
LD12
LD18
Red
GND
RSVD[7..0]
P3V3
No
SW1
NOGA0
NOGA1
NOGA2
NOGA3
NOGA4
USEGA
SWITCH0
SWITCH1
4k7
GND
Project/Equipment
Simple VME FMC Carrier
Document
System FPGA
BE-CO
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer G.Kasprowicz
Drawn by Greg Kasprowicz 20/11/2012
Check by T.Janicki 23/01/2012
Last Mod. 2012-02-08
File SFPGA.SchDoc
Print Date 2012-02-08 01:55:50
Sheet 12 of 15
EDA-xxxx
Size A3
Rev -

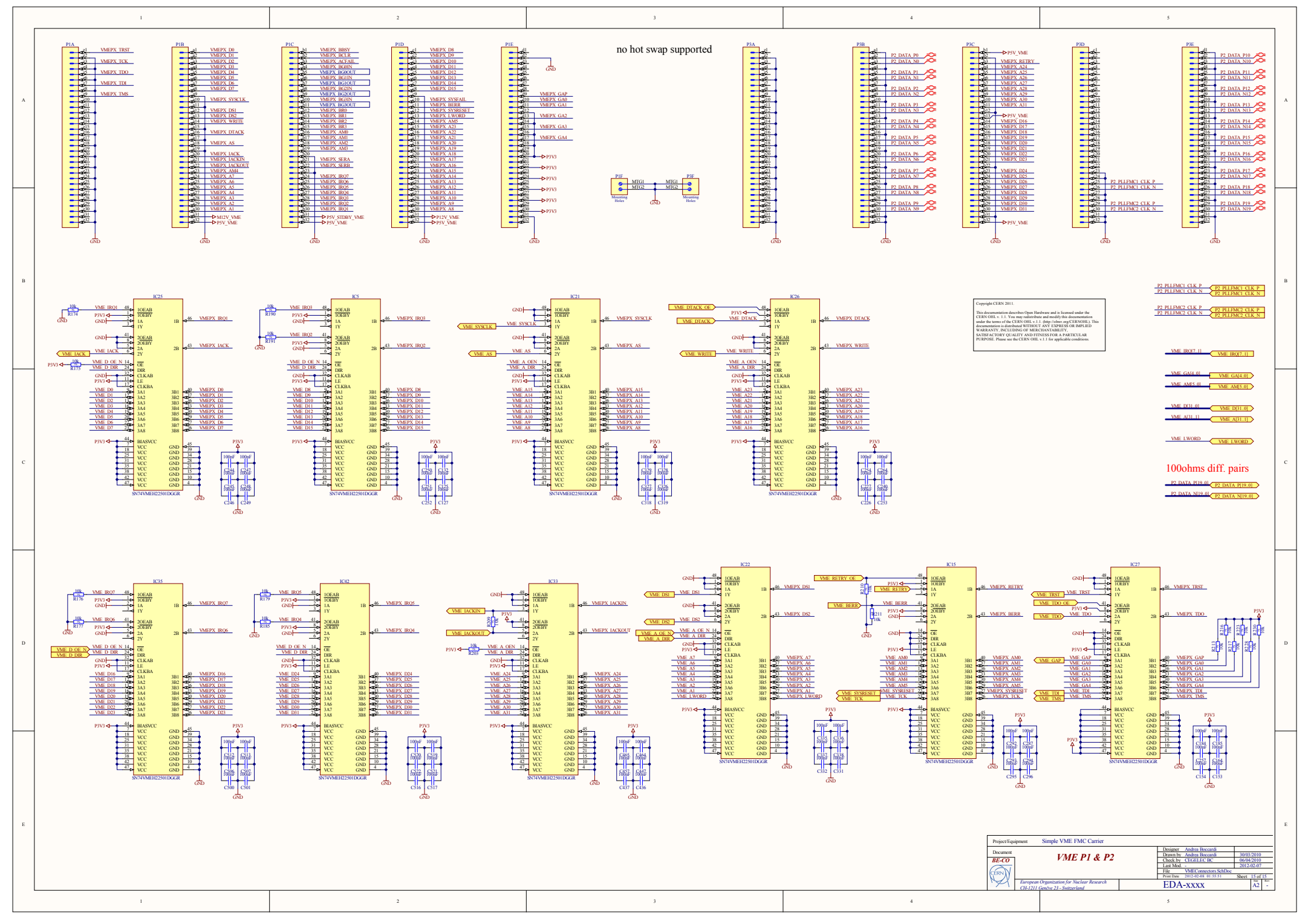


Project/Equipment	Simple VME FMC Carrier		
Document	**USB interface**	Designer G.Kasprowicz	
BE-CO		Drawn by Greg Kasprowicz	20/11/2012
		Check by T.Janicki	23/01/2012
		Last Mod.	2012-02-07
		File SFPGA_power.SchDoc	
		Print Date 2012-02-08 01:55:50	Sheet 13 of 15
European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-xxxx	Size A3	Rev -

NOT MOUNTED BY DEFAULT



Project/Equipment	Simple VME FMC Carrier		
Document	**USB interface**	Designer G.Kasprowicz	
BE-CO		Drawn by Greg Kasprowicz	20/11/2012
		Check by T.Janicki	23/01/2012
		Last Mod.	2012-02-07
		File USB.SchDoc	
		Print Date 2012-02-08 01:55:51	Sheet 14 of 15
European Organization for Nuclear Research CH-1211 Geneve 23 - Switzerland	EDA-xxxx	Size A3	Rev -


no hot swap supported
P1A
P1B
P1C
P1D
P1E
P3A
P3B
P3C
P3D
P3E
P1F
P3F
IC25
IC5
IC21
IC26
IC35
IC42
IC33
IC22
IC15
IC27
SN74VMEH22501DGGR
VMEPX_TRST
VMEPX_TCK
VMEPX_TDO
VMEPX_TDI
VMEPX_TMS
VMEPX_SYSCLK
VMEPX_DS1
VMEPX_DS2
VMEPX_WRITE
VMEPX_DTACK
VMEPX_AS
VMEPX_IACK
VMEPX_IACKIN
VMEPX_IACKOUT
VMEPX_AM4
VMEPX_A7
VMEPX_A6
VMEPX_A5
VMEPX_A4
VMEPX_A3
VMEPX_A2
VMEPX_A1
M12V_VME
P5V_VME
P5V_STDBY_VME
P12V_VME
VMEPX_BBSY
VMEPX_BCLR
VMEPX_ACFAIL
VMEPX_BG0IN
VMEPX_BG0OUT
VMEPX_BG1IN
VMEPX_BG1OUT
VMEPX_BG2IN
VMEPX_BG2OUT
VMEPX_BG3IN
VMEPX_BG3OUT
VMEPX_BR0
VMEPX_BR1
VMEPX_BR2
VMEPX_BR3
VMEPX_AM0
VMEPX_AM1
VMEPX_AM2
VMEPX_AM3
VMEPX_SERA
VMEPX_SERB
VMEPX_IRQ7
VMEPX_IRQ6
VMEPX_IRQ5
VMEPX_IRQ4
VMEPX_IRQ3
VMEPX_IRQ2
VMEPX_IRQ1
VMEPX_D0
VMEPX_D1
VMEPX_D2
VMEPX_D3
VMEPX_D4
VMEPX_D5
VMEPX_D6
VMEPX_D7
VMEPX_D8
VMEPX_D9
VMEPX_D10
VMEPX_D11
VMEPX_D12
VMEPX_D13
VMEPX_D14
VMEPX_D15
VMEPX_SYSFAIL
VMEPX_BERR
VMEPX_SYSRESET
VMEPX_LWORD
VMEPX_AM5
VMEPX_A23
VMEPX_A22
VMEPX_A21
VMEPX_A20
VMEPX_A19
VMEPX_A18
VMEPX_A17
VMEPX_A16
VMEPX_A15
VMEPX_A14
VMEPX_A13
VMEPX_A12
VMEPX_A11
VMEPX_A10
VMEPX_A9
VMEPX_A8
VMEPX_GAP
VMEPX_GA0
VMEPX_GA1
VMEPX_GA2
VMEPX_GA3
VMEPX_GA4
P2_DATA_P0
P2_DATA_N0
P2_DATA_P1
P2_DATA_N1
P2_DATA_P2
P2_DATA_N2
P2_DATA_P3
P2_DATA_N3
P2_DATA_P4
P2_DATA_N4
P2_DATA_P5
P2_DATA_N5
P2_DATA_P6
P2_DATA_N6
P2_DATA_P7
P2_DATA_N7
P2_DATA_P8
P2_DATA_N8
P2_DATA_P9
P2_DATA_N9
P2_DATA_P10
P2_DATA_N10
P2_DATA_P11
P2_DATA_N11
P2_DATA_P12
P2_DATA_N12
P2_DATA_P13
P2_DATA_N13
P2_DATA_P14
P2_DATA_N14
P2_DATA_P15
P2_DATA_N15
P2_DATA_P16
P2_DATA_N16
P2_DATA_P17
P2_DATA_N17
P2_DATA_P18
P2_DATA_N18
P2_DATA_P19
P2_DATA_N19
P2_PLLFMC1_CLK_P
P2_PLLFMC1_CLK_N
P2_PLLFMC2_CLK_P
P2_PLLFMC2_CLK_N
P5V_VME
VMEPX_RETRY
VMEPX_A24
VMEPX_A25
VMEPX_A26
VMEPX_A27
VMEPX_A28
VMEPX_A29
VMEPX_A30
VMEPX_A31
VMEPX_D16
VMEPX_D17
VMEPX_D18
VMEPX_D19
VMEPX_D20
VMEPX_D21
VMEPX_D22
VMEPX_D23
VMEPX_D24
VMEPX_D25
VMEPX_D26
VMEPX_D27
VMEPX_D28
VMEPX_D29
VMEPX_D30
VMEPX_D31
MTG1
MTG2
Mounting Holes
GND
P3V3
VME_IRQ1
VME_IRQ2
VME_IRQ3
VME_IRQ4
VME_IRQ5
VME_IRQ6
VME_IRQ7
VME_IACK
VME_D_OE_N
VME_D_DIR
VME_SYSCLK
VME_AS
VME_DTACK_OE
VME_DTACK
VME_WRITE
VME_A_OEN
VME_A_DIR
VME_A_OE_N
VME_RETRY_OE
VME_RETRY
VME_BERR
VME_SYSRESET
VME_TCK
VME_TDI
VME_TDO_OE
VME_TDO
VME_TRST
VME_TMS
VME_GAP
VME_GA0
VME_GA1
VME_GA2
VME_GA3
VME_GA4
VME_AM0
VME_AM1
VME_AM2
VME_AM3
VME_AM4
VME_AM5
VME_LWORD
VME_A1
VME_A2
VME_A3
VME_A4
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VME_D10
VME_D11
VME_D12
VME_D13
VME_D14
VME_D15
VME_IRQ7_1]
VME_GA[4..0]
VME_AM[5..0]
VME_D[31..0]
VME_A[31..1]
100ohms diff. pairs
P2_DATA_P[19..0]
P2_DATA_N[19..0]
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Project/Equipment
Simple VME FMC Carrier
Document
VME P1 & P2
BE-CO
European Organization for Nuclear Research
CH-1211 Geneve 23 - Switzerland
Designer Andrea Boccardi
Drawn by Andrea Boccardi 30/03/2010
Check by CEGELEC BK 06/04/2010
Last Mod. 2012-02-07
File VMEConnectors.SchDoc
Print Date 2012-02-08 01:55:51
Sheet 15 of 15
EDA-xxxx
A2