

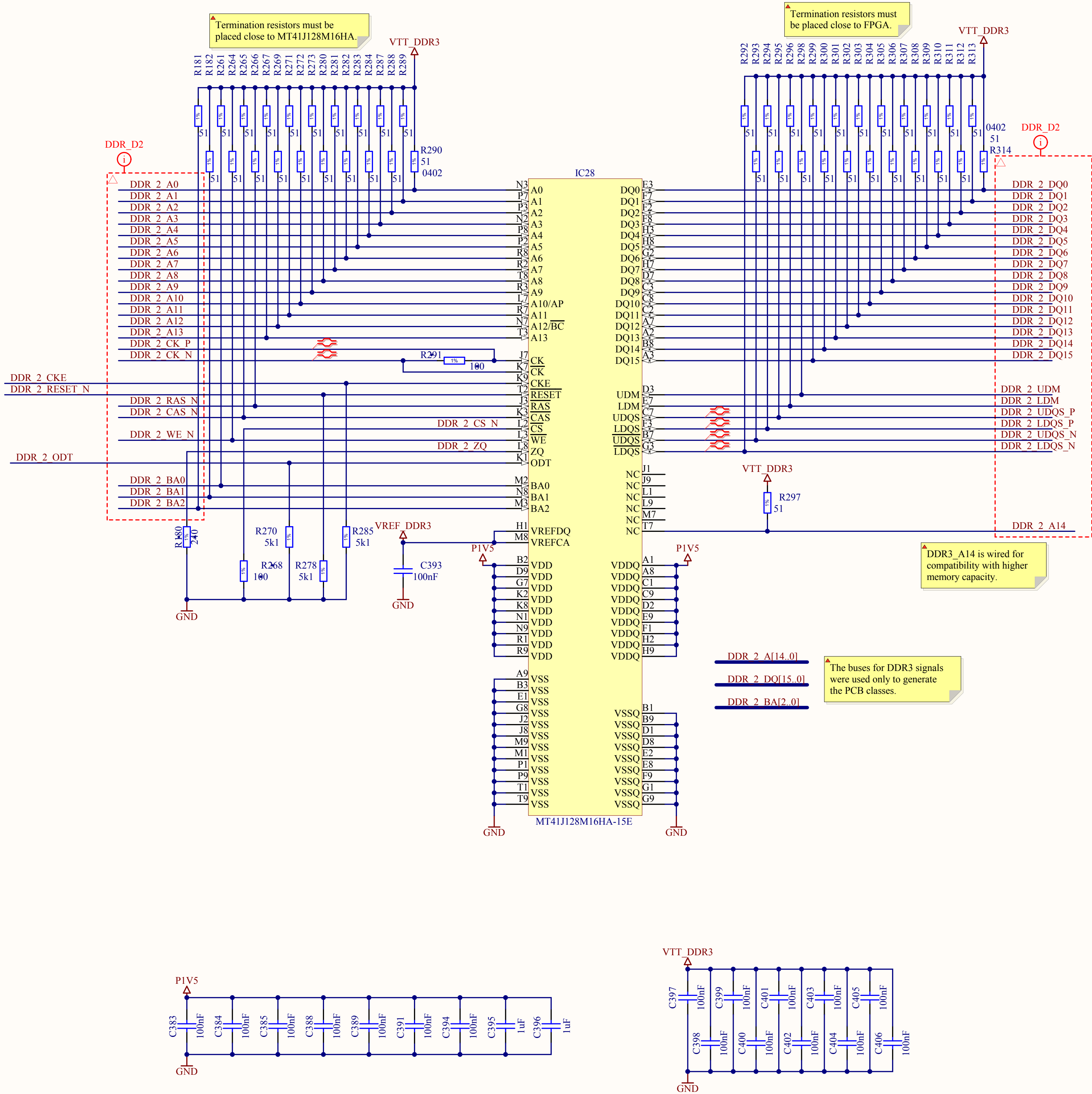




Copyright CERN 2011.

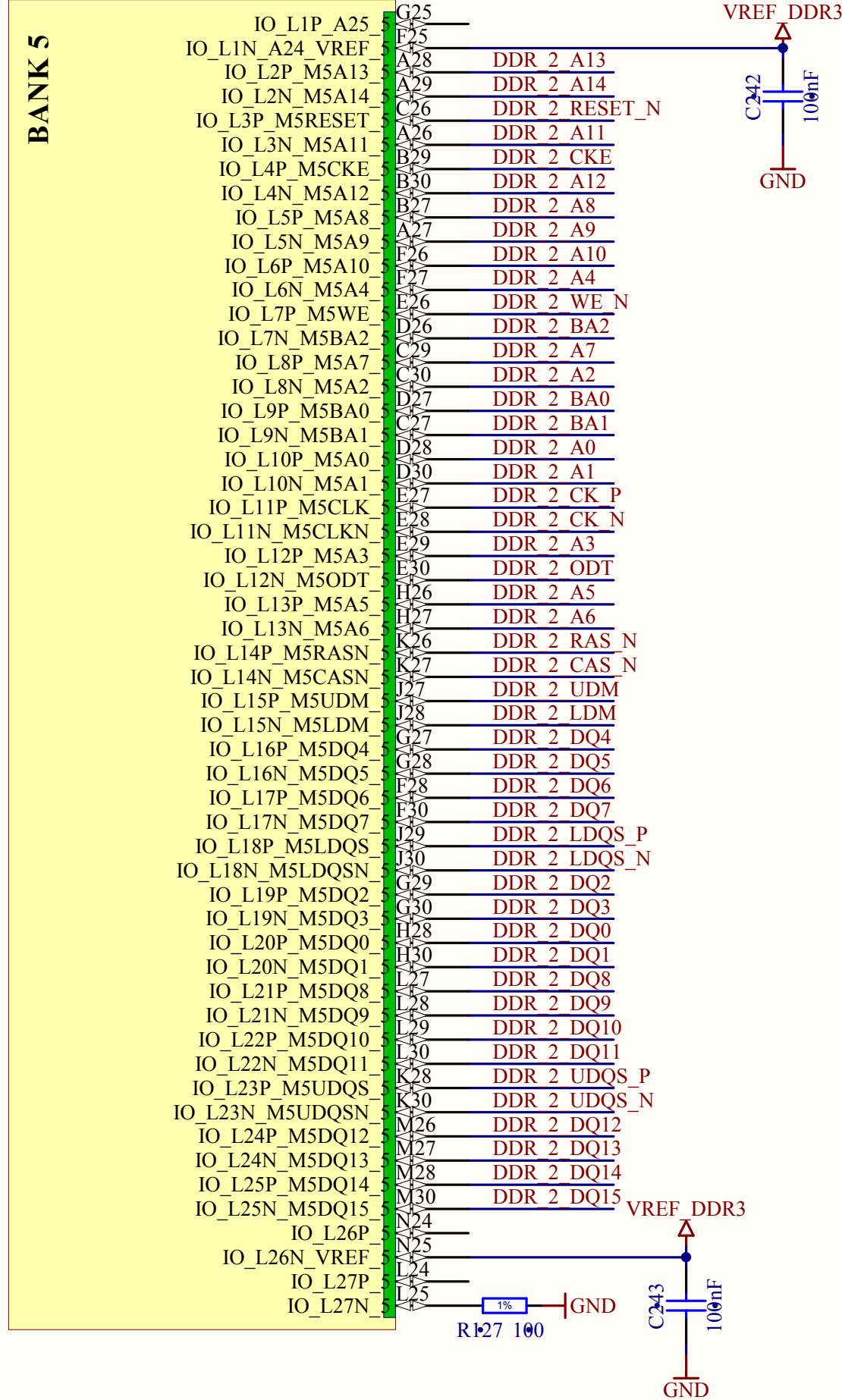
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>).


This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.



VCCO\_5 = 1.5V

4C191  
x6SLX150T-2FGG900C



Project/Equipment		Simple VME FMC Carrier	
Document		Designer	G.Kasprowicz
<b>BE-CO</b> 		Drawn by	G.Kasprowicz
		Check by	T.Janicki
		Last Mod.	-
		File	DDR3_2.SchDoc
		Print Date	2012-05-01 22:22:56
		Sheet	4 of 21
		Size	A3
		Rev	-

**DDR3 memory**  
**- bank 5 -**

European Organization for Nuclear Research  
CH-1211 Geneva 23 - Switzerland

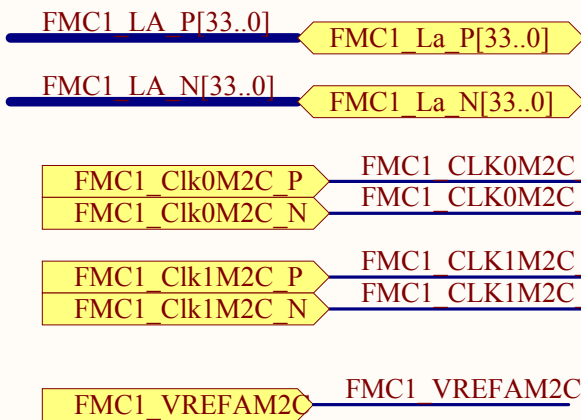
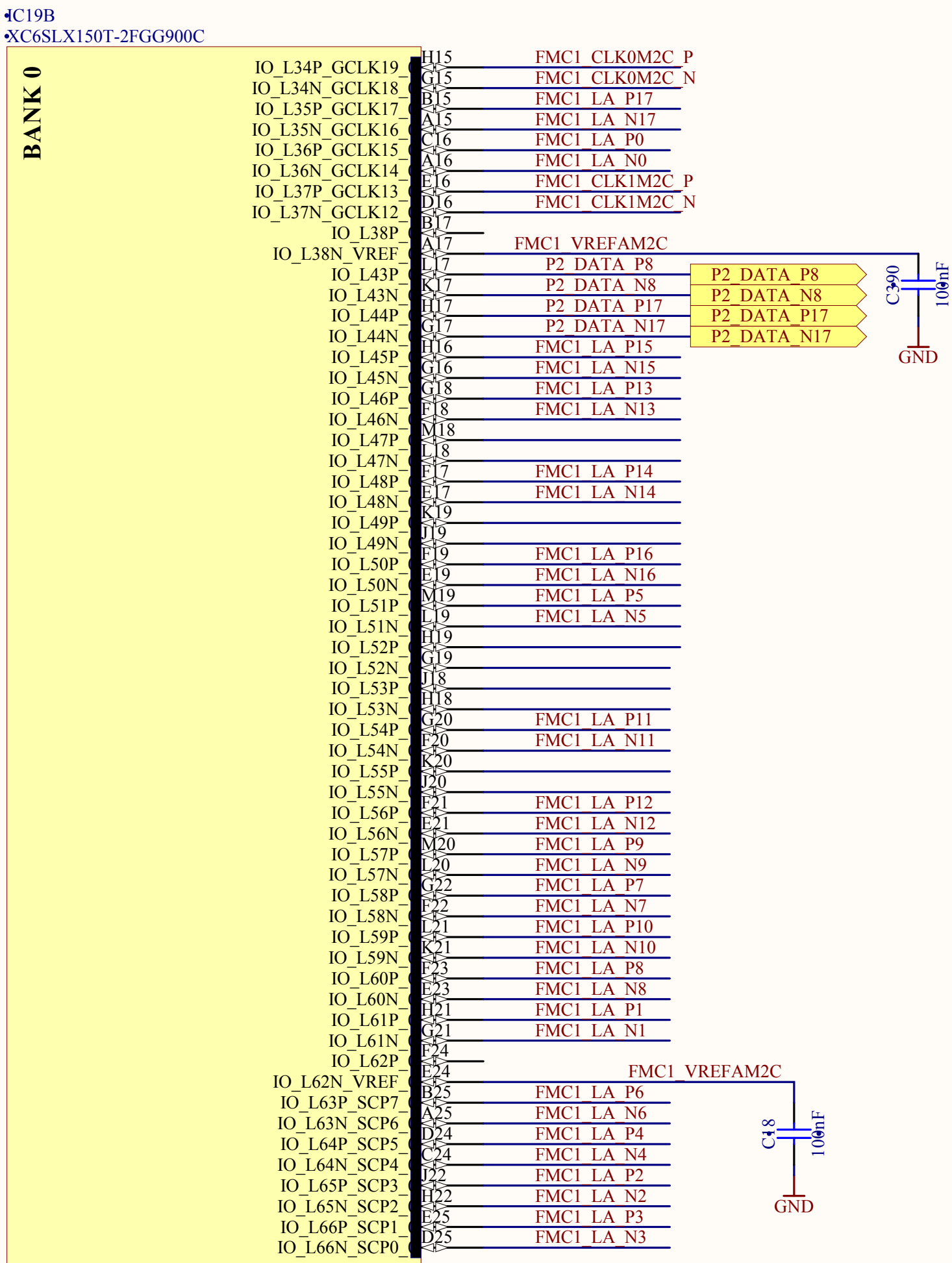
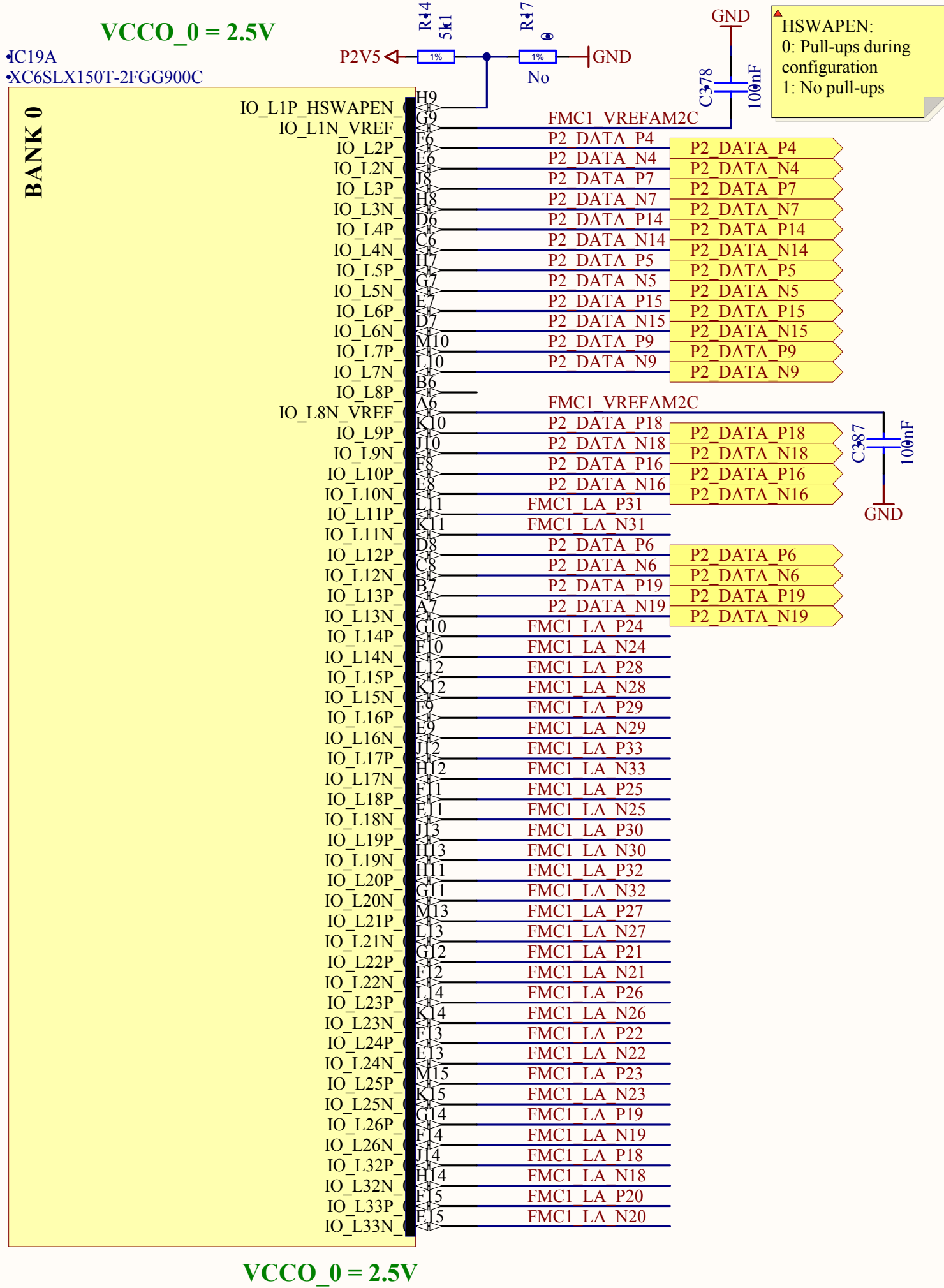
EDA-xxxx




Copyright CERN 2011.

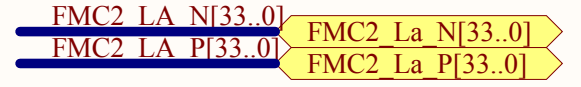
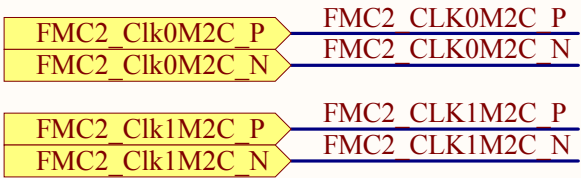
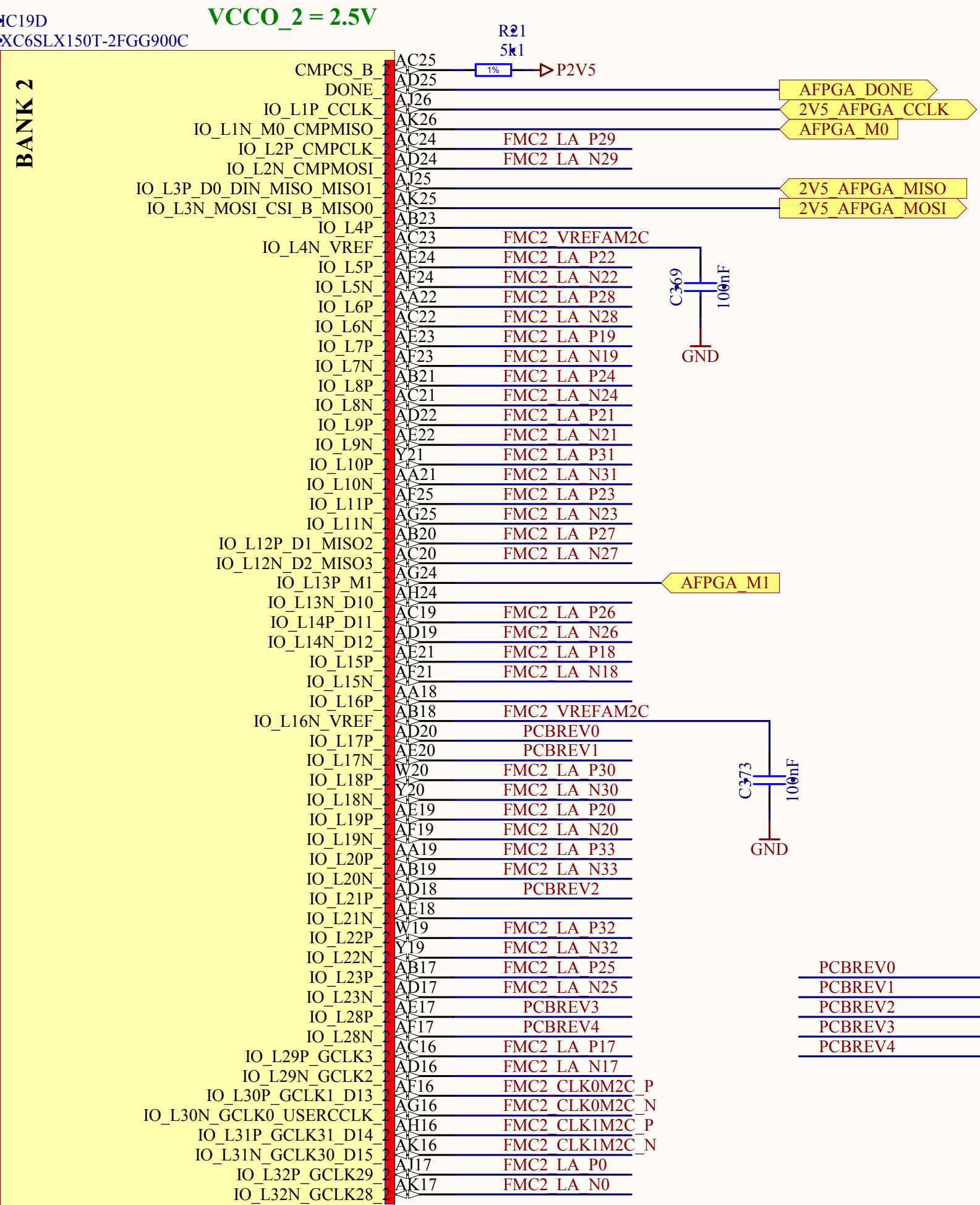
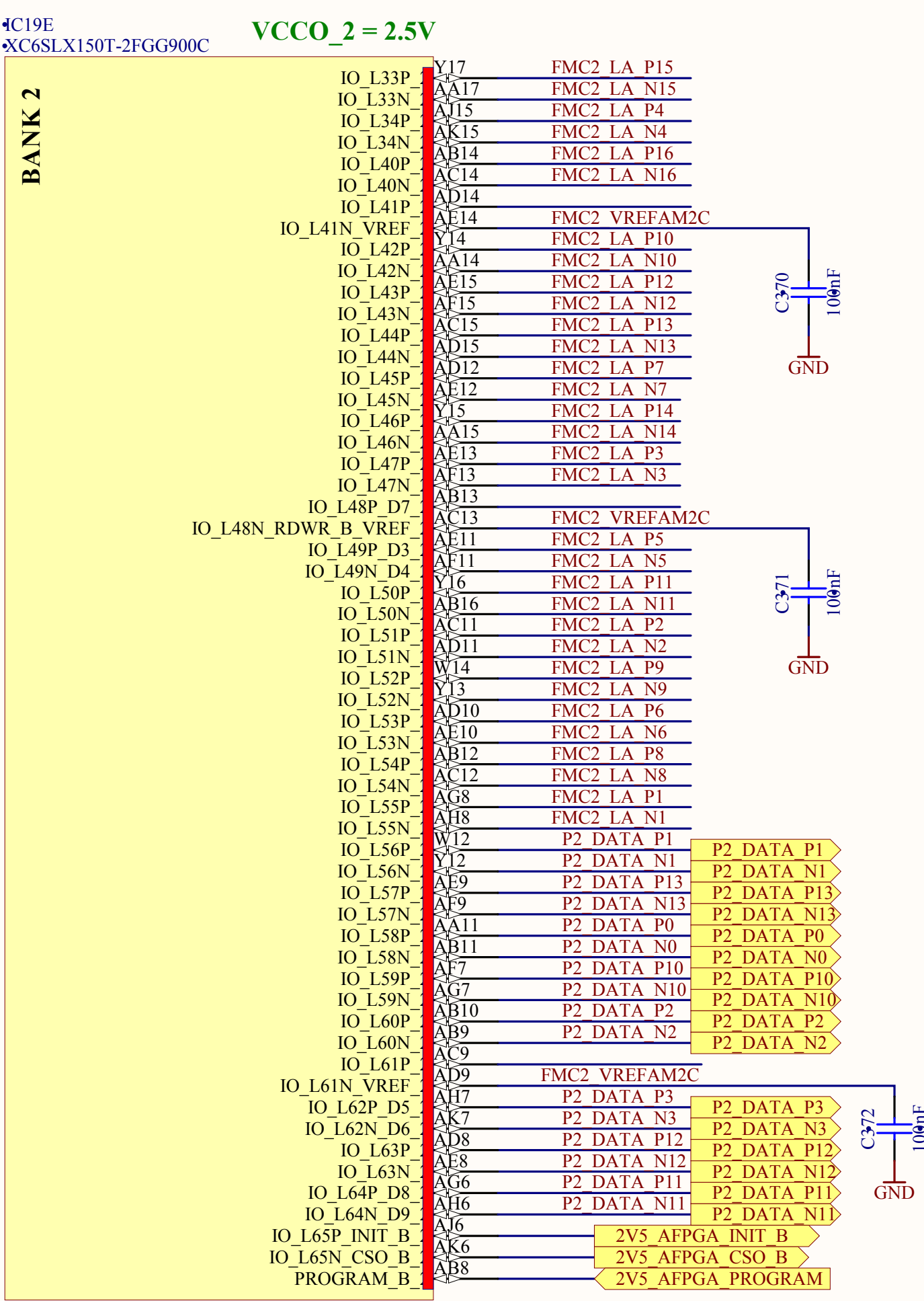
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>).


This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.



Project/Equipment		Simple VME FMC Carrier	
Document		Designer	G.Kasprowicz
<div>BE-CO</div> <div></div>		Drawn by	G.Kasprowicz
		Check by	T.Janicki
		Last Mod.	-
		File	AFPGA_FMC1_bank0.SchDoc
Print Date		2012-05-01 22:22:57	Sheet 5 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		Size	A3
EDA-xxxx		Rev	-

This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>). This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

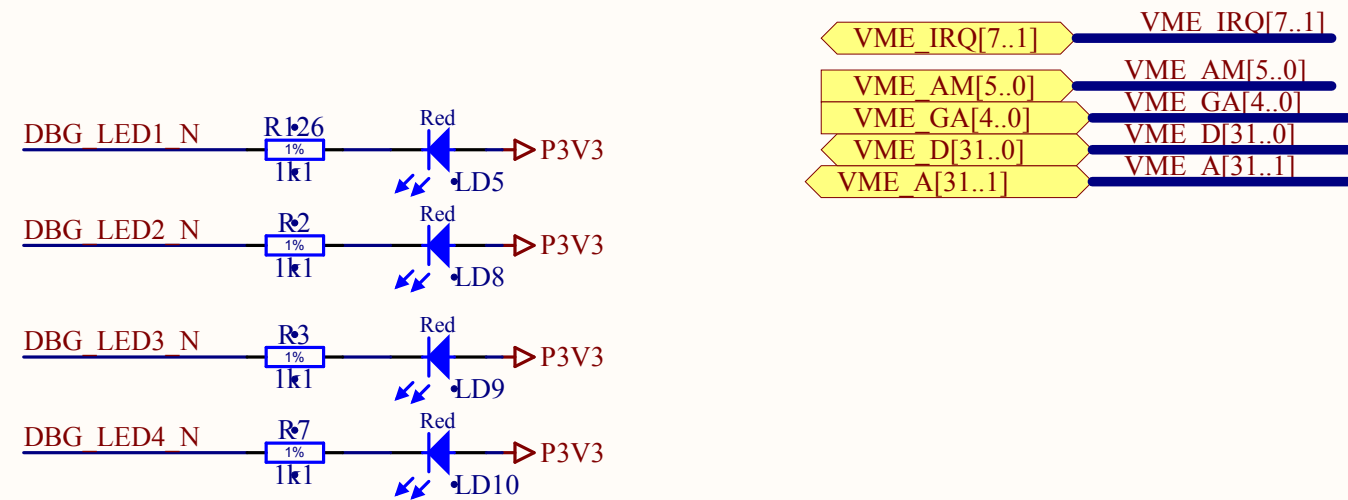
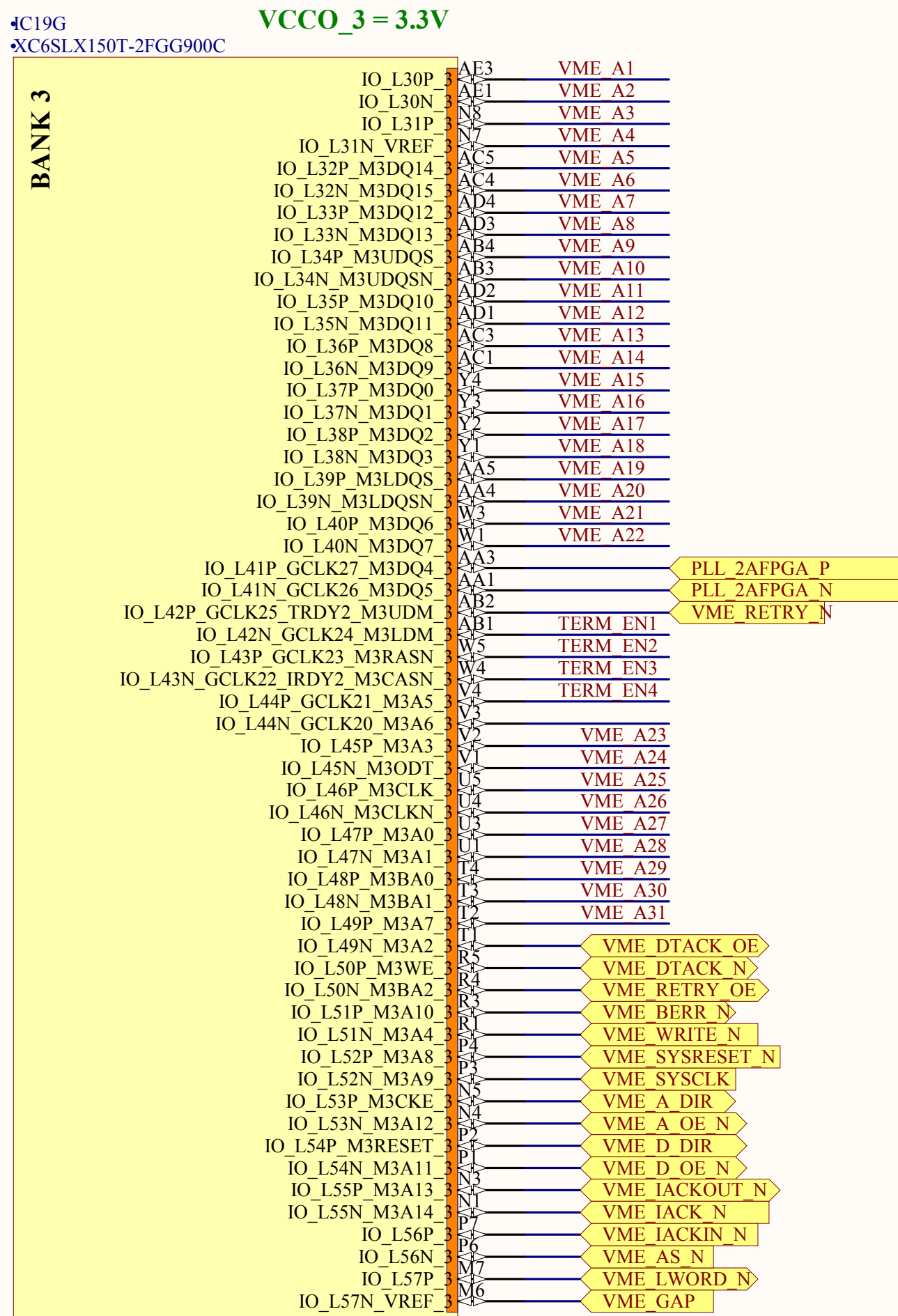
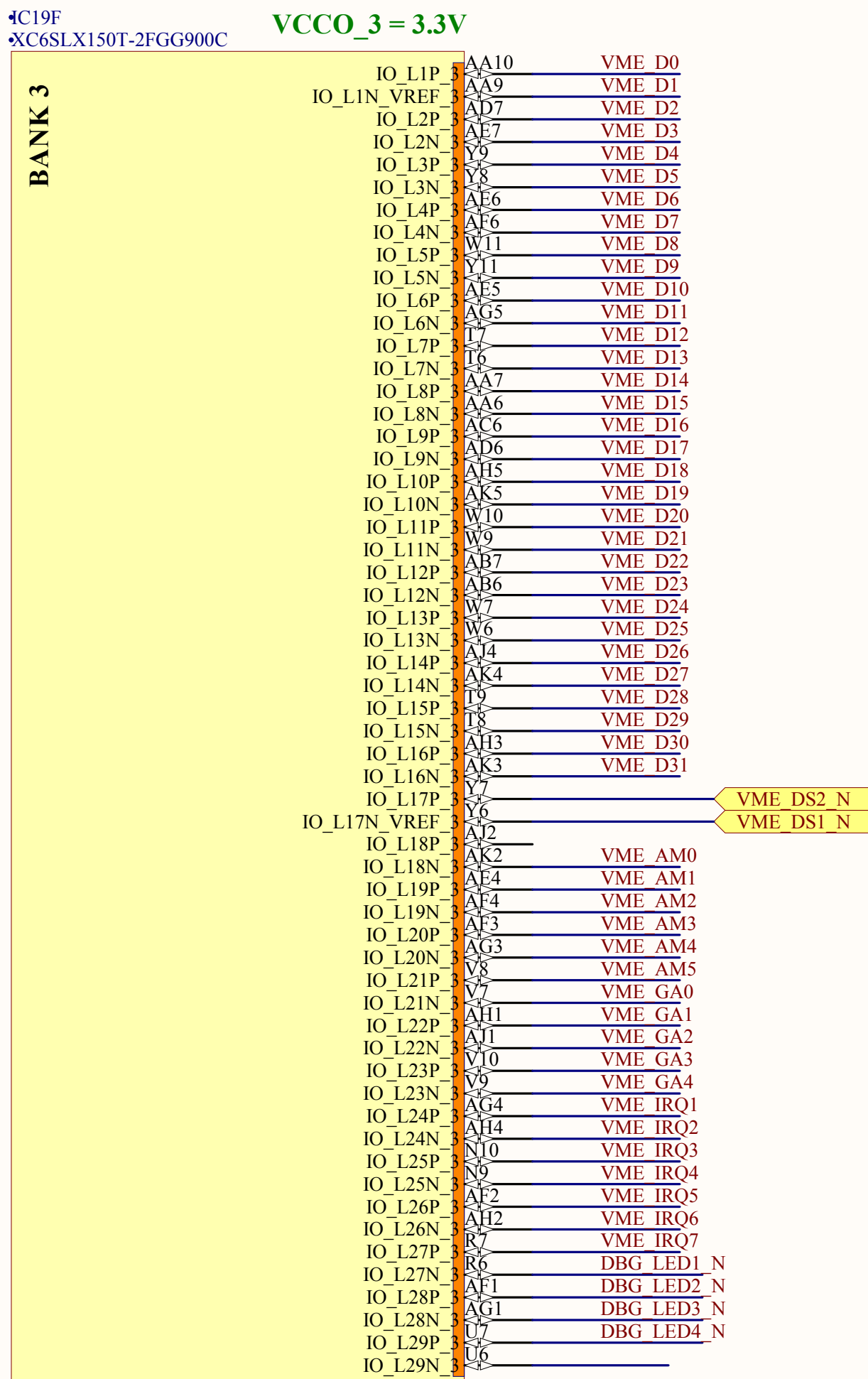
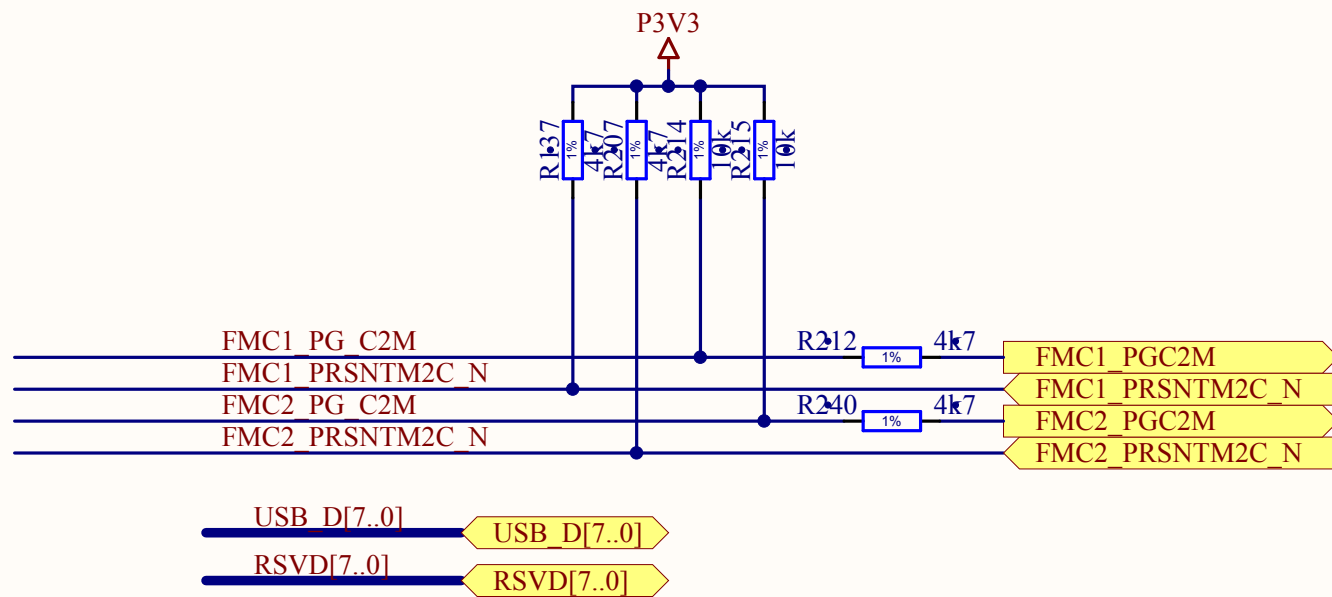
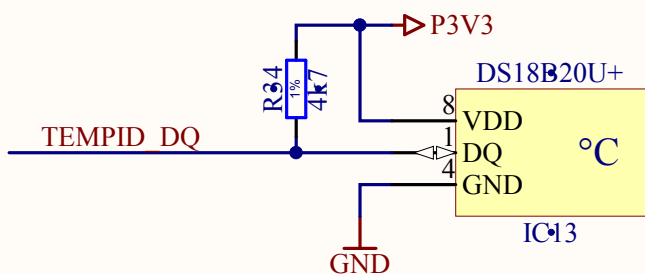
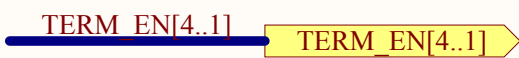
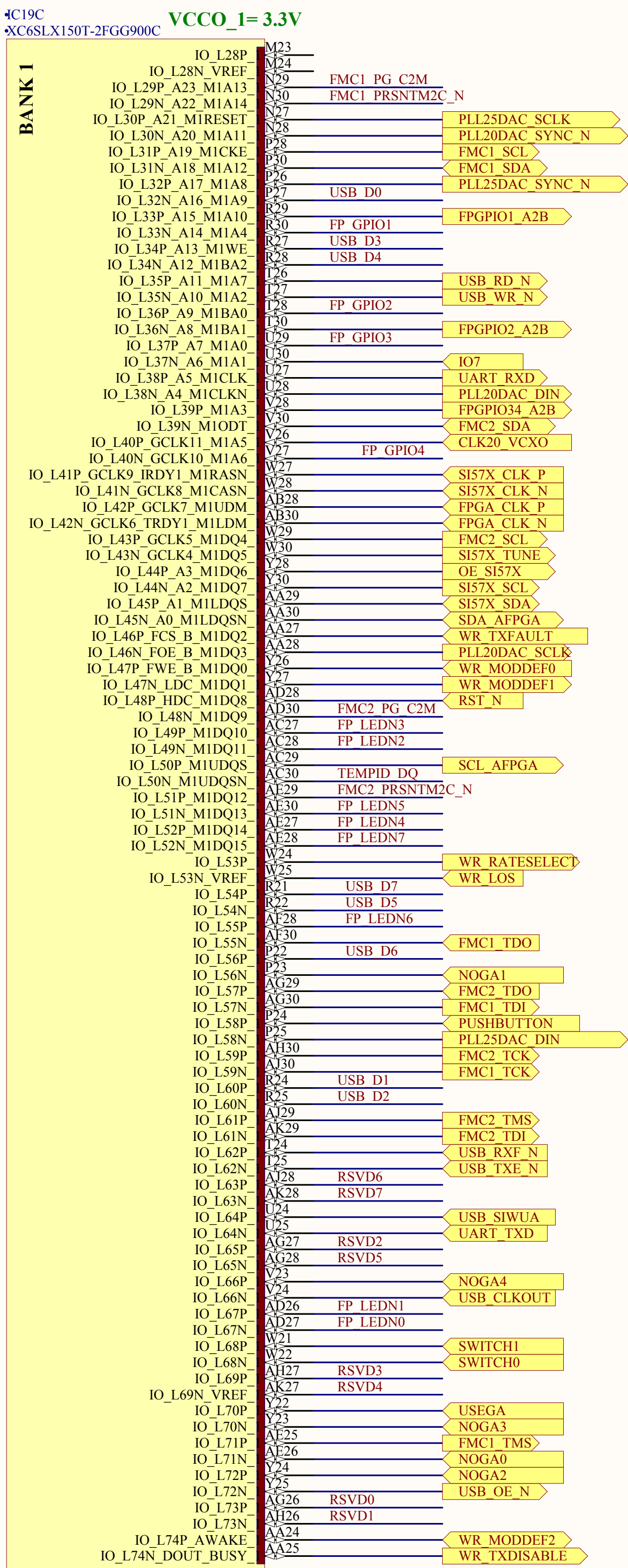


Project/Equipment		Simple VME FMC Carrier	
Document		Designer	G.Kasprowicz
<div>BE-CO</div> <div></div>		Drawn by	G.Kasprowicz
		Check by	T.Janicki
		Last Mod.	-
		File	AFPGA_FMC2_bank2.SchDoc
Print Date		2012-05-01 22:22:57	Sheet 6 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		Size	A3
		Rev	-

AFPGA FMC2  
- bank 2 -

EDA-xxxx





Project/Equipment	Simple VME FMC Carrier		
Document			
Designer	G.Kasprowicz		
Drawn by	G.Kasprowicz		20/11/2012
Check by	T.Janicki		30/04/2012
Last Mod.	-		2012-05-01
File	AFPGA_VME_IO_banks1+3.SchDoc		
Print Date	2012-05-01 22:22:57	Sheet	7 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-xxxx	

Copyright CERN 2011.

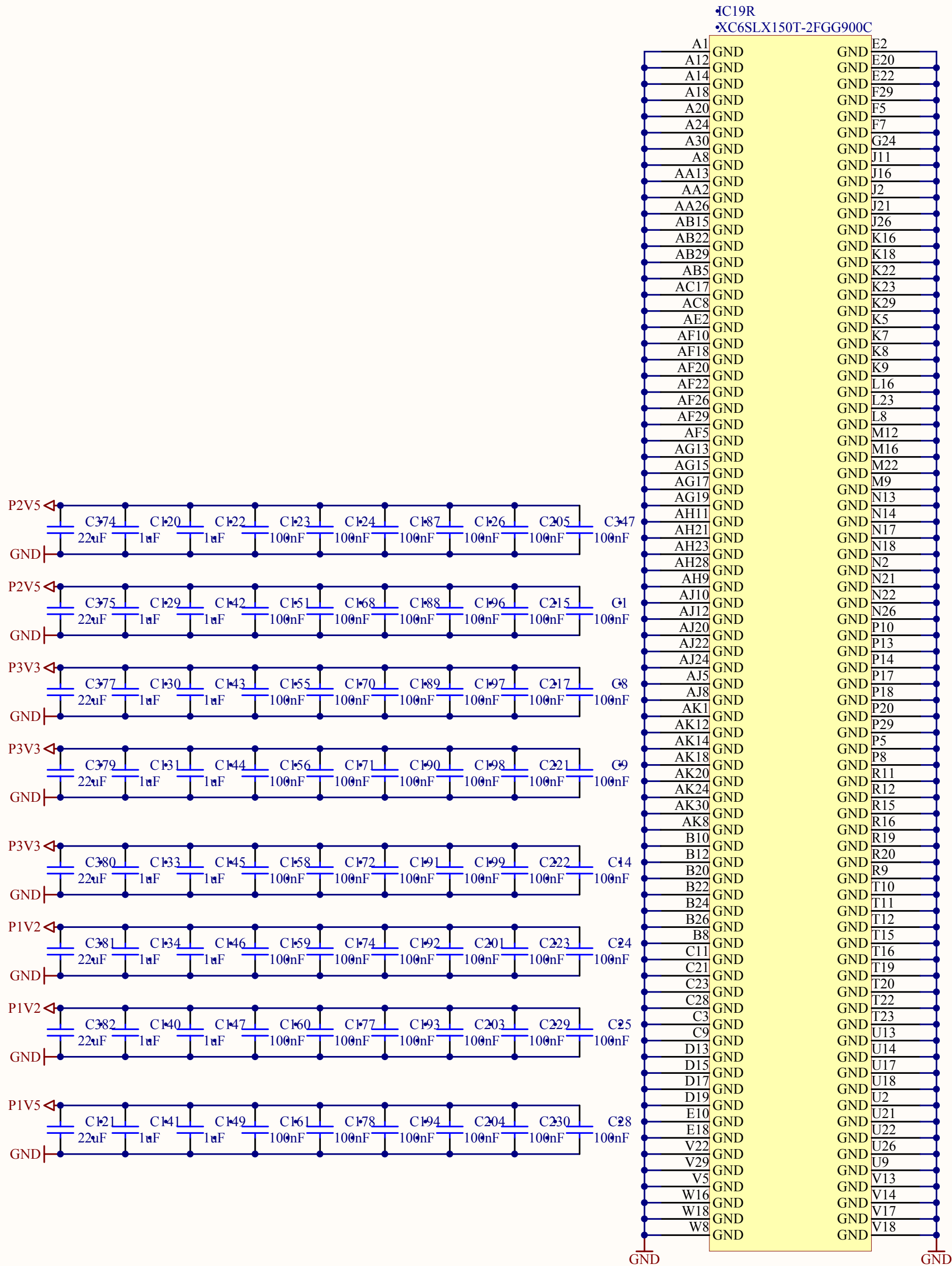
This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>).

This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

**AFPGA VME & IO**  
**- banks 1 & 3 -**



On-chip differential termination is specified with a nominal value of 100R when VCCAUX = 3.3V. The on-chip differential termination can be used when VCCAUX = 2.5V, however a wider resistance range is specified. ([http://www.xilinx.com/support/documentation/user\\_guides/ug381.pdf](http://www.xilinx.com/support/documentation/user_guides/ug381.pdf), page 14). Moreover storage of the AES keys requires VCCAUX of at least 3V

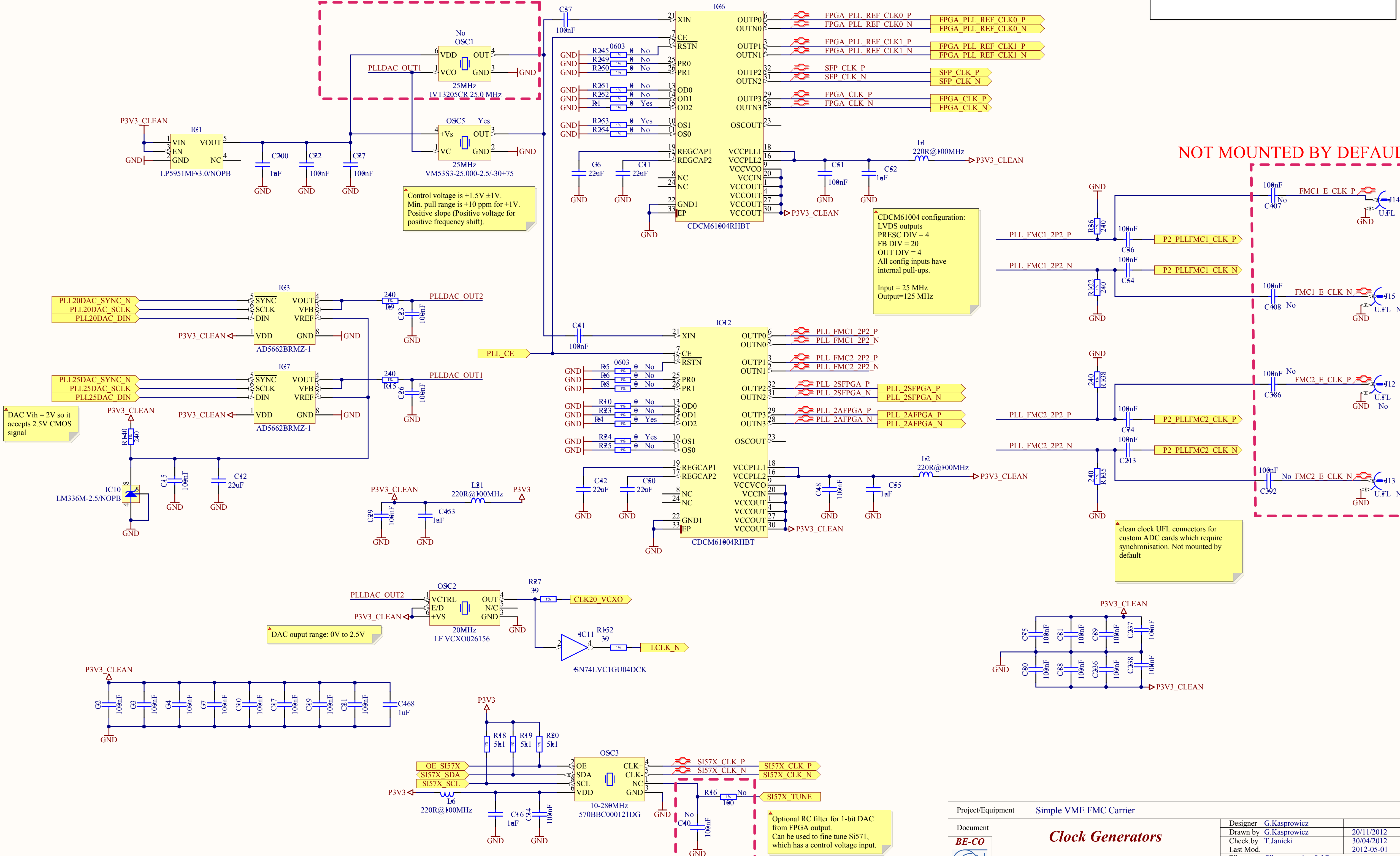




NOT MOUNTED BY DEFAULT

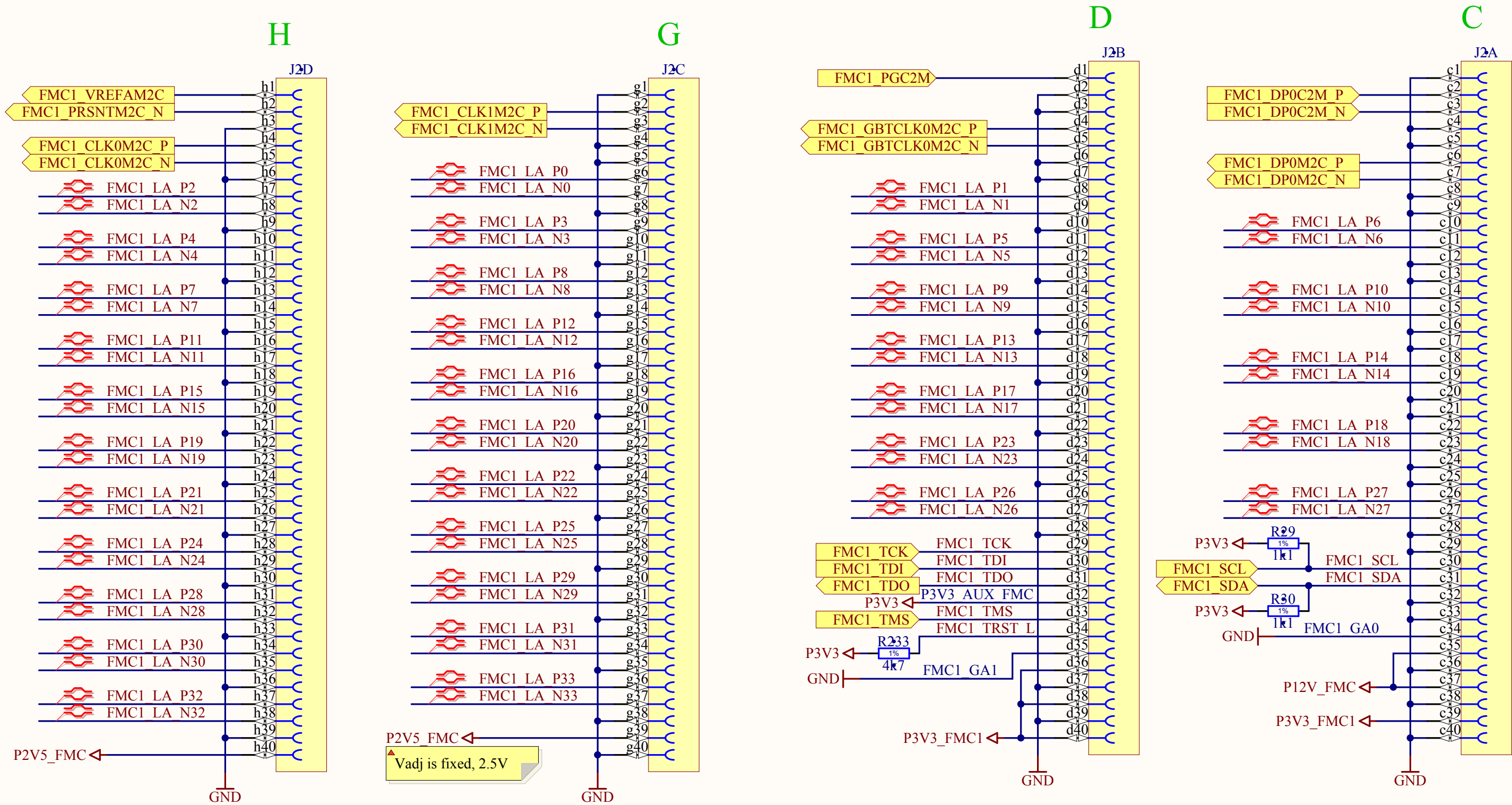
NOT MOUNTED BY DEFAULT

NOT MOUNTED BY DEFAULT

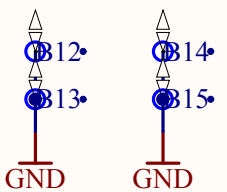
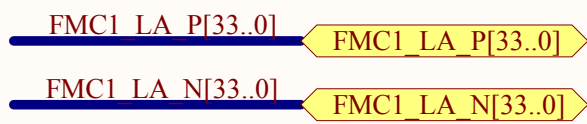




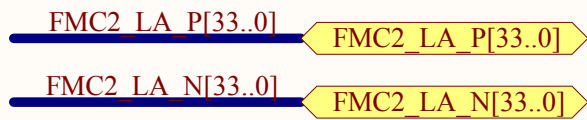
### FMC slot 1



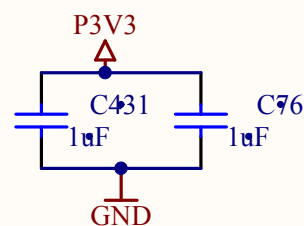
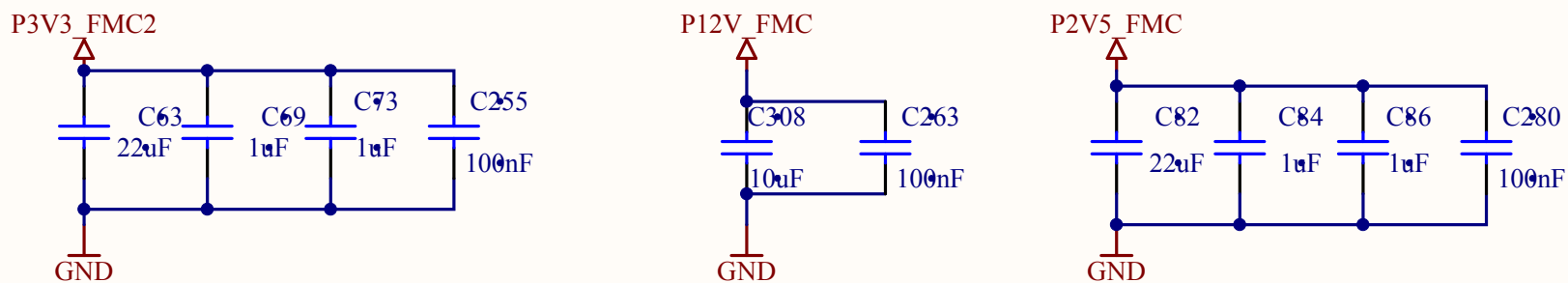
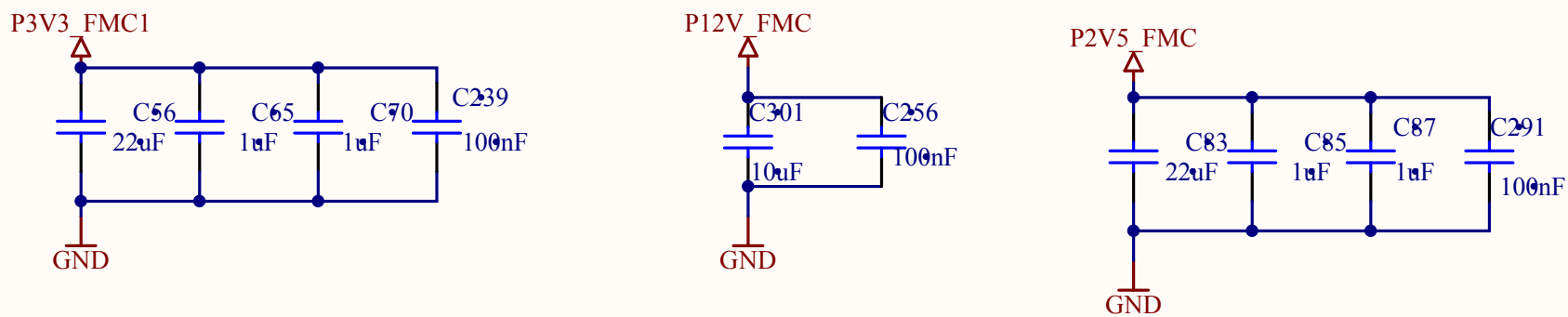
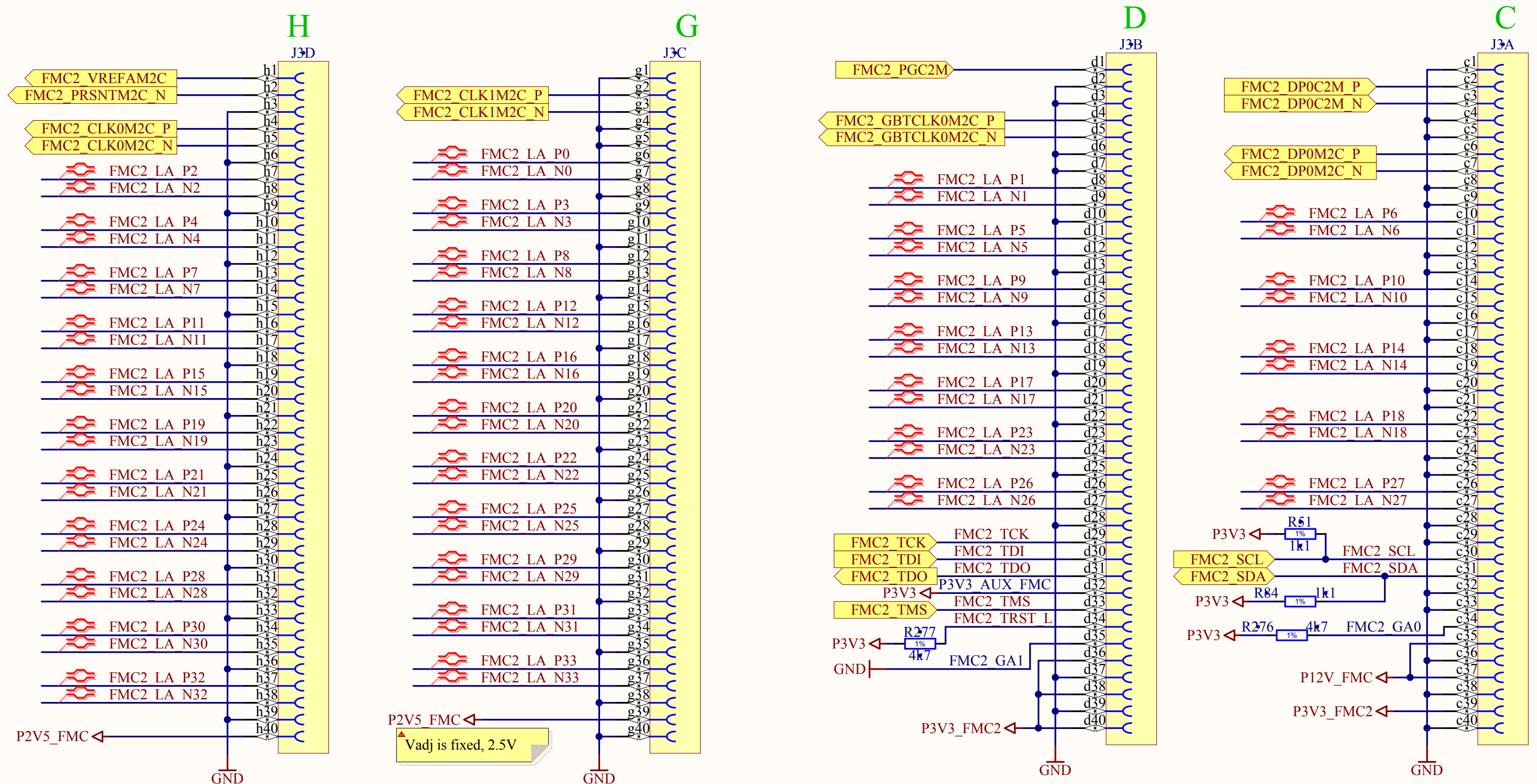
FMC1\_LaP and FMC1\_LaN are 100ohms diff. pairs



FMC2\_LaP and FMC2\_LaN are 100ohms diff. pairs



### FMC slot 2



Project/Equipment		Simple VME FMC Carrier	
Document		Designer	G.Kasprowicz
		Drawn by	G.Kasprowicz
		Check by	T.Janicki
		Last Mod.	2012-05-01
		File	FMC_CONNECTORS.SchDoc
		Print Date	2012-05-01 22:22:57
		Sheet	10 of 21
		Size	A3
		Rev	-

European Organization for Nuclear Research  
CH-1211 Geneva 23 - Switzerland

EDA-xxxx



A

B

C

D

E

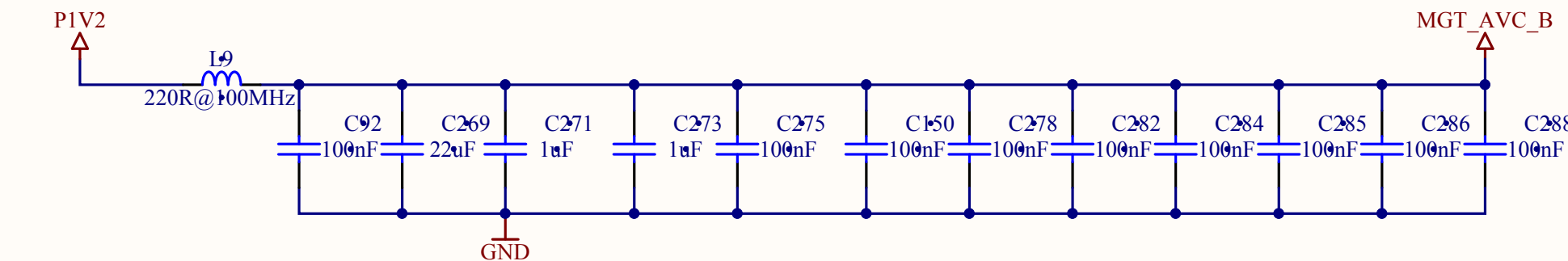
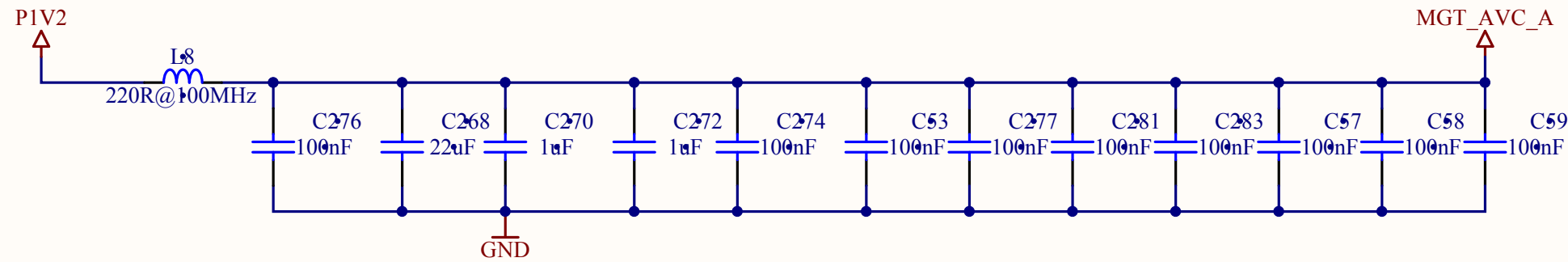
A

B

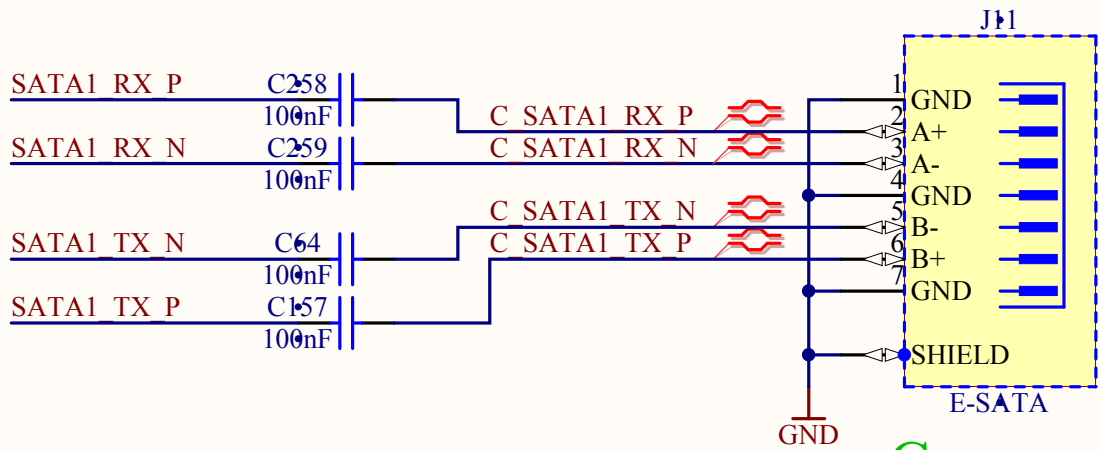
C

D

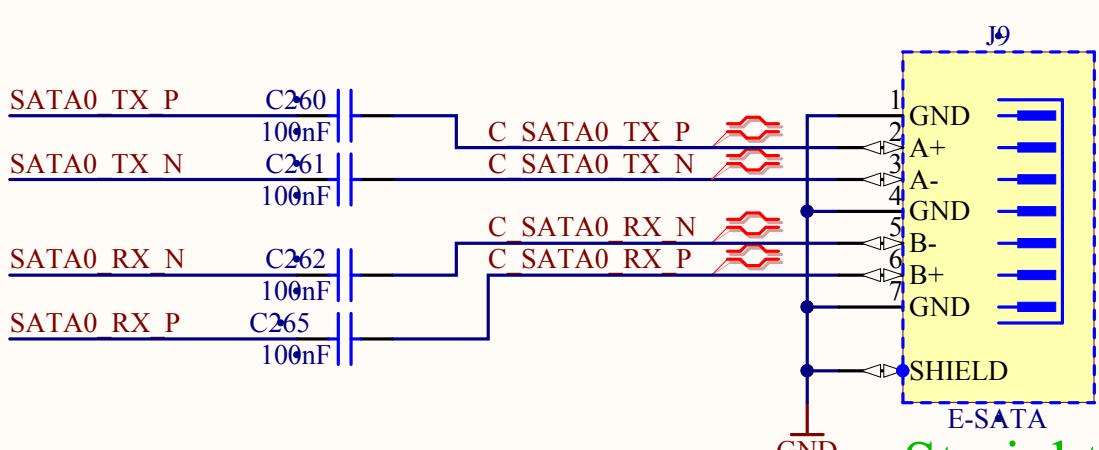
E



## E-SATA connectors

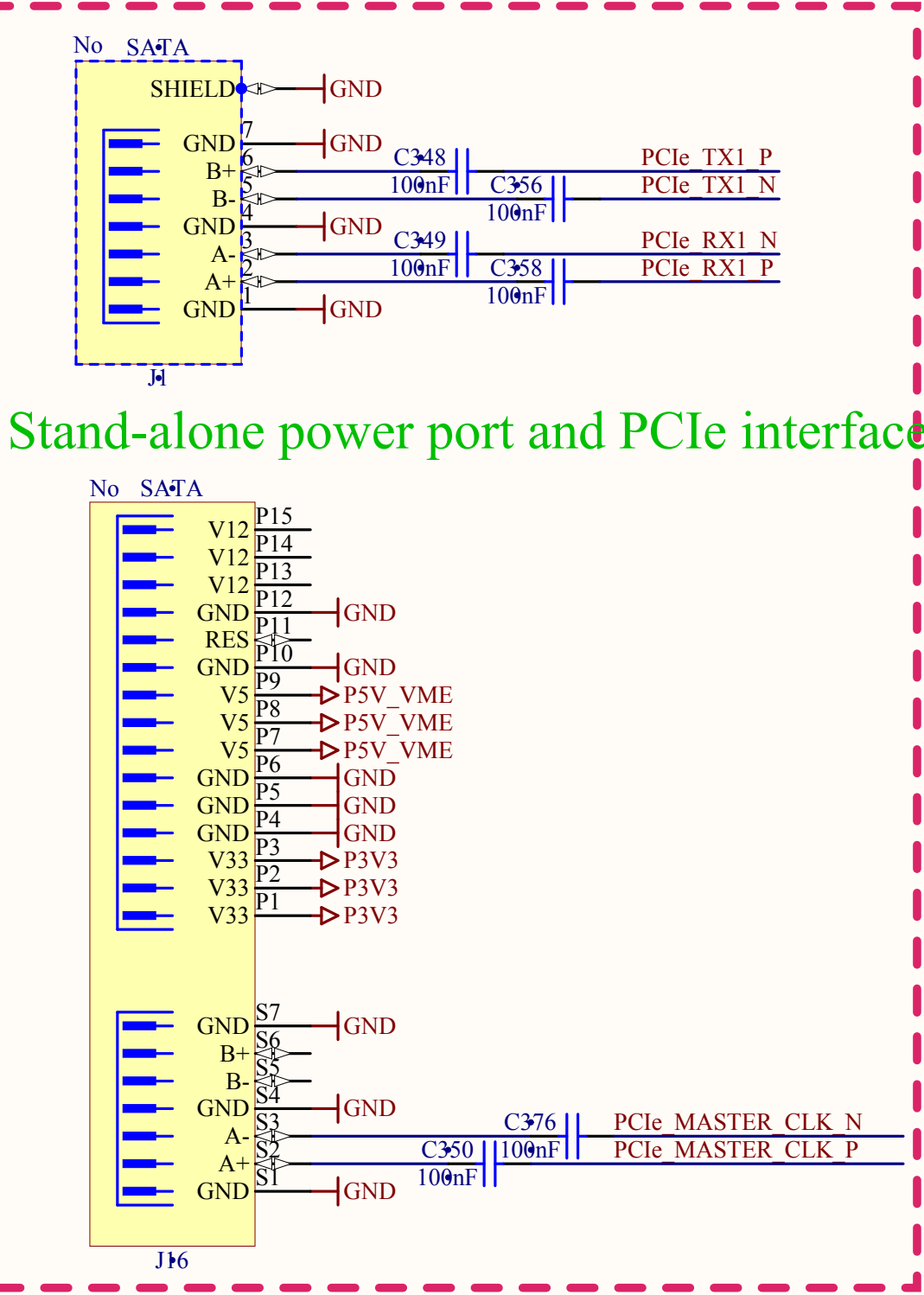


Crossover

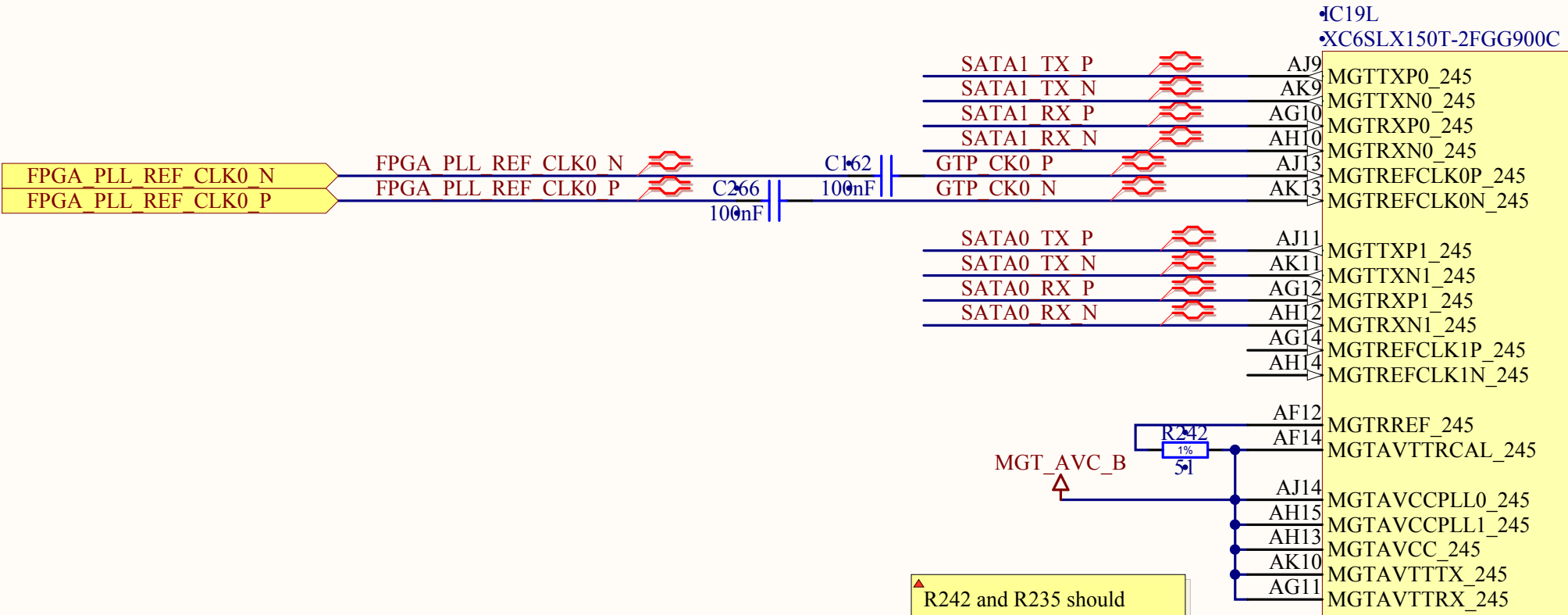
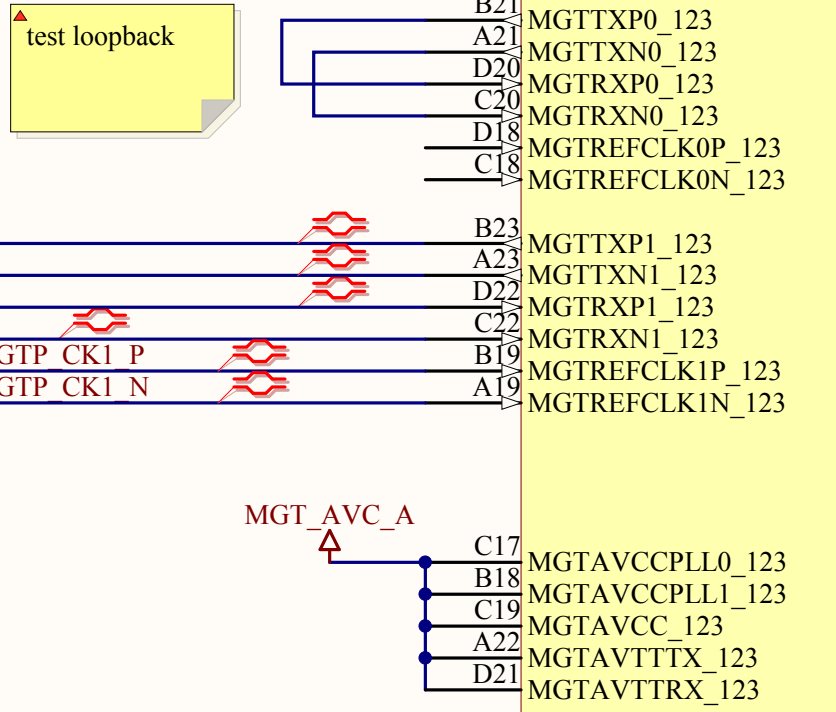
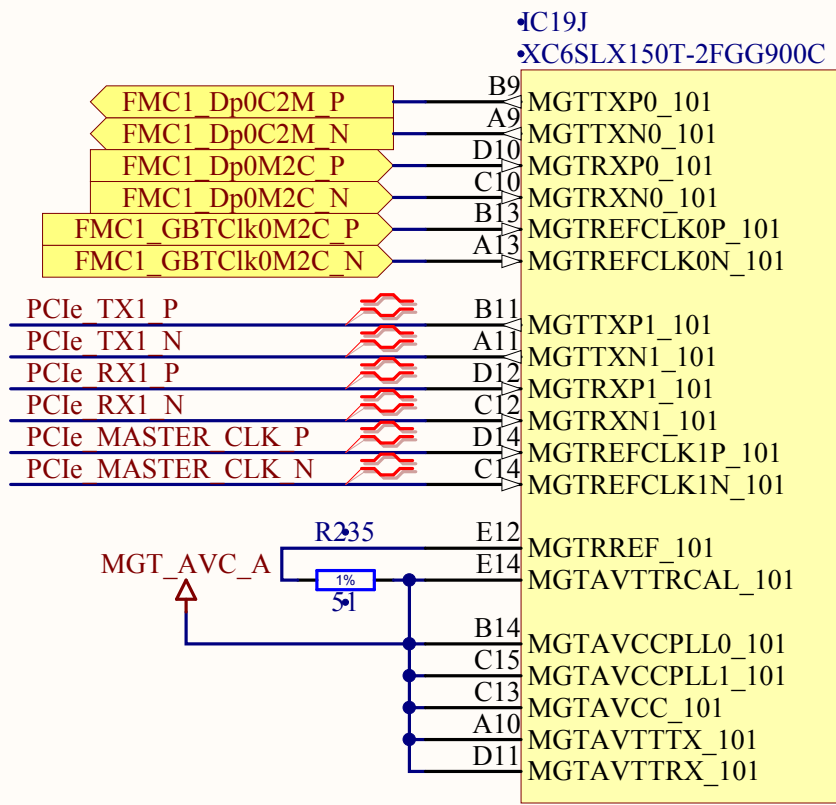


Straight

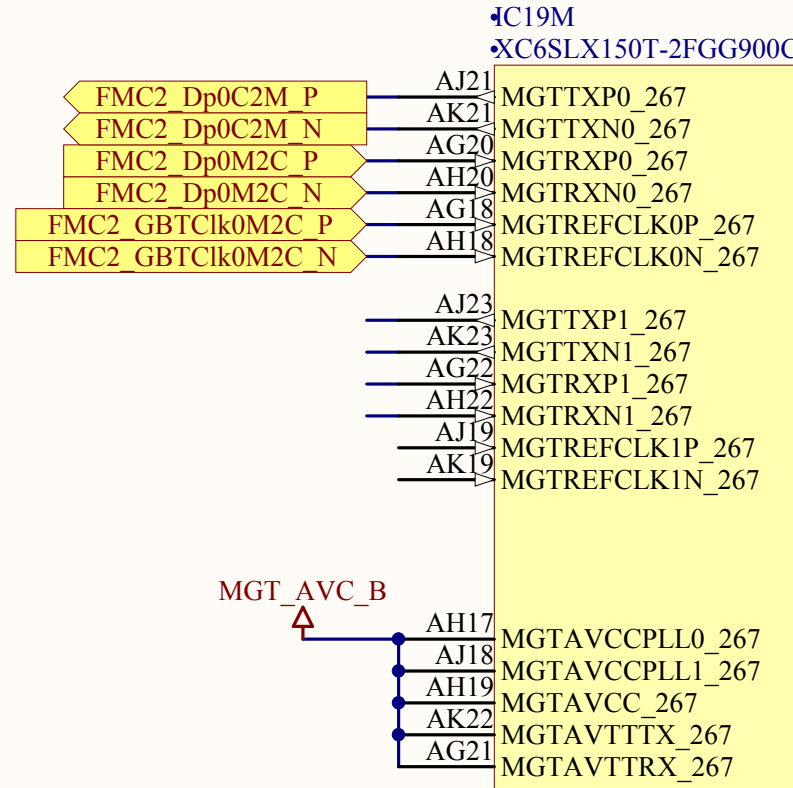
## NOT MOUNTED BY DEFAULT



## Stand-alone power port and PCIe interface



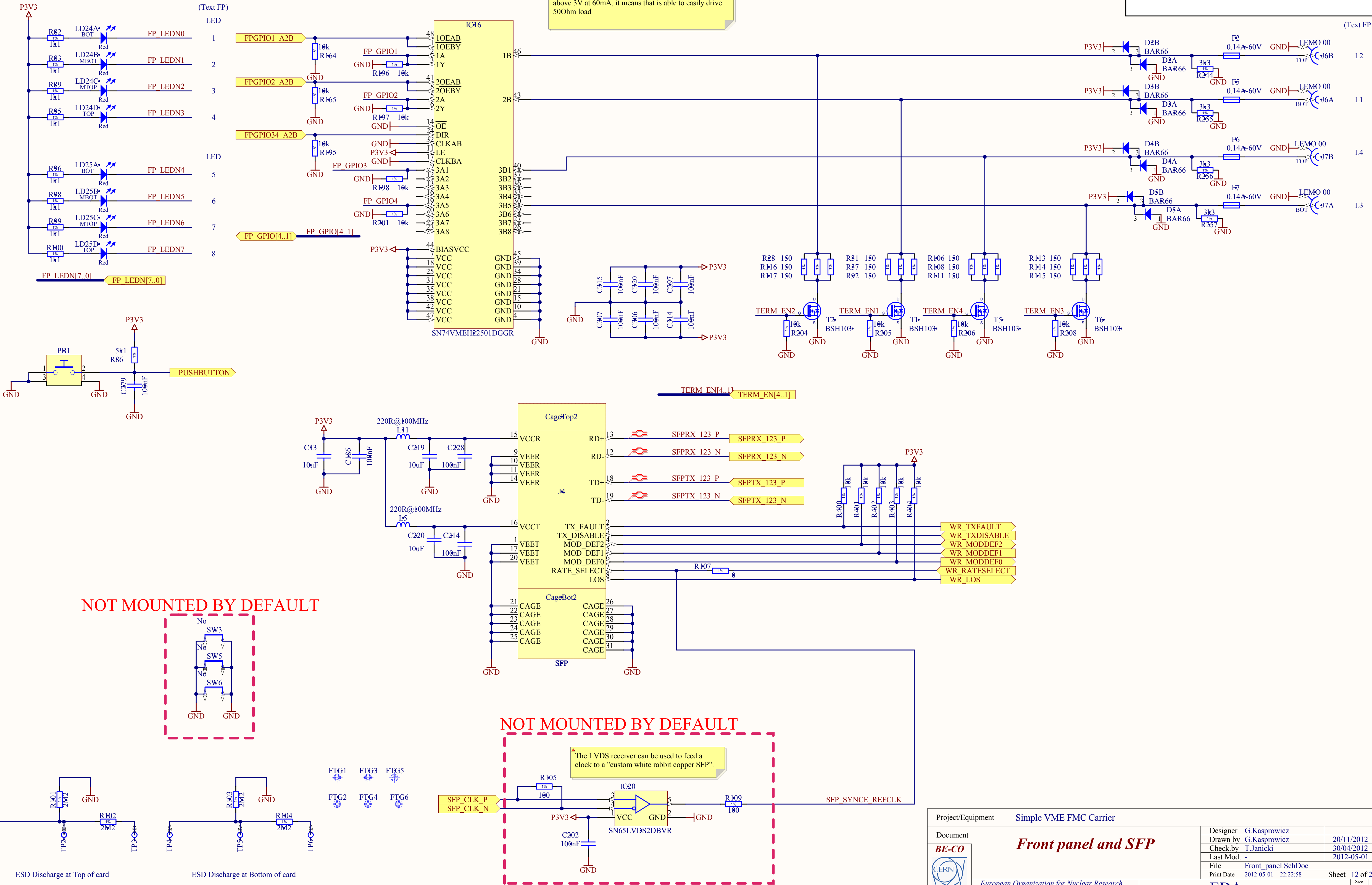
R242 and R235 should have the same lengths for their terminals



Copyright CERN 2011.

This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>).

This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.

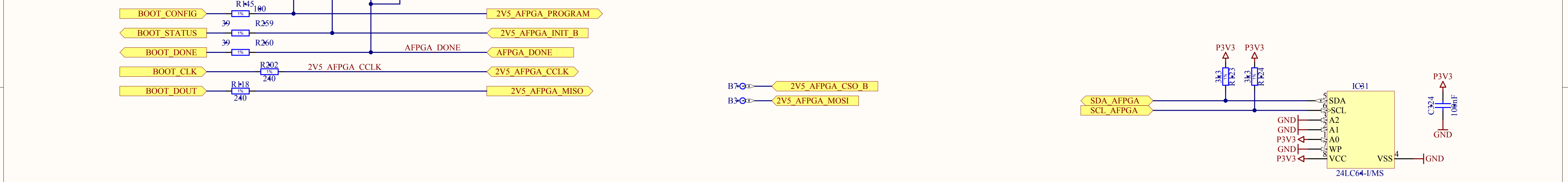
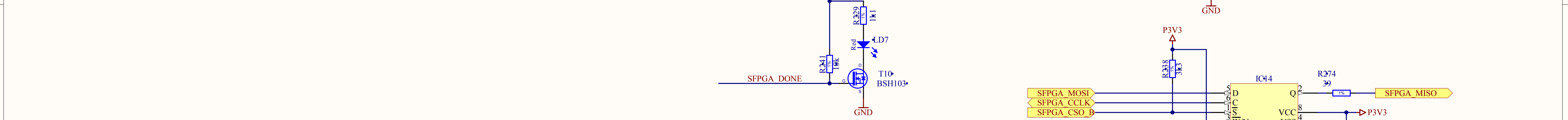
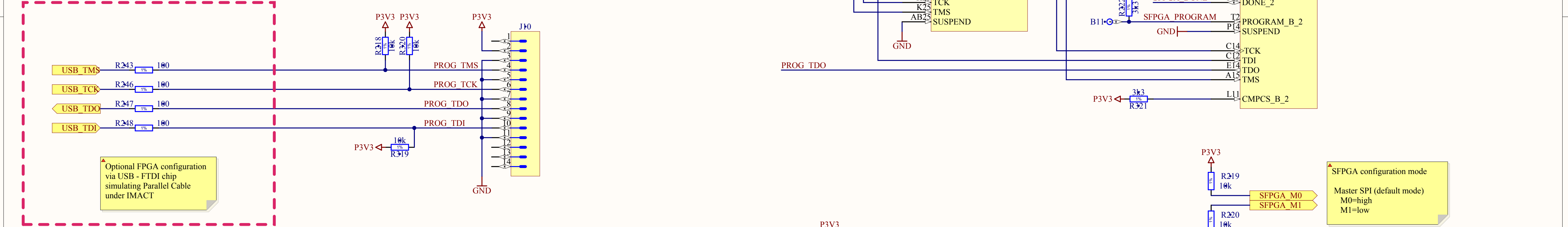


Project/Equipment	Simple VME FMC Carrier		
Document	<b>BE-CO</b> <i>Front panel and SFP</i>		
Designer	G.Kasprowicz	20/11/2012	
Drawn by	G.Kasprowicz	30/04/2012	
Check by	T.Janicke	2012-05-01	
Last Mod.	-		
File	Front_panel.SchDoc	Sheet	12 of 21
Print Date	2012-05-01 22:22:58	Size	A3
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		Rev	-
EDA-xxxx			



A

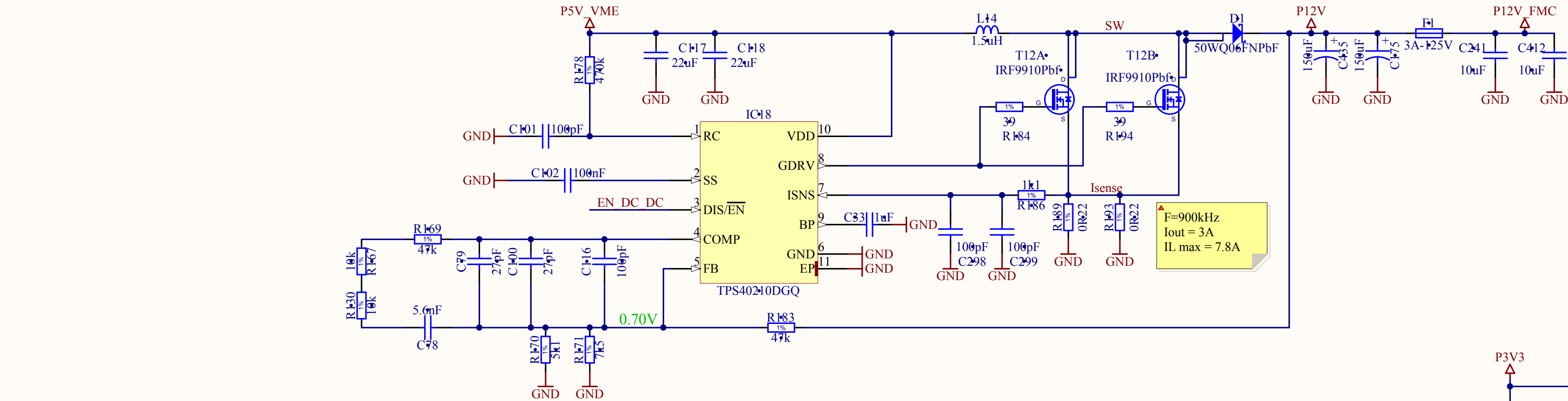
A



Copyright CERN 2011.

This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>).

This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.



Power estimation:

P1V2  
AFPGA 3A  
SFGPA 500mA

P1V5  
AFPGA 1A + 2x DDR3 (max 2x 530mW )  
([http://download.micron.com/pdf/technotes/ddr3/TN41\\_01DDR3%20Power.pdf](http://download.micron.com/pdf/technotes/ddr3/TN41_01DDR3%20Power.pdf))  
estimated power from P1V5 is about 1.5A

P2V5  
AFPGA 2A

P2V5\_FMC1  
FMC slot 2A (HPC = 4A, LPC = 2A)

P2V5\_FMC2  
FMC slot 2A (HPC = 4A, LPC = 2A)

P3V3\_FMC1  
FMC slot 3A

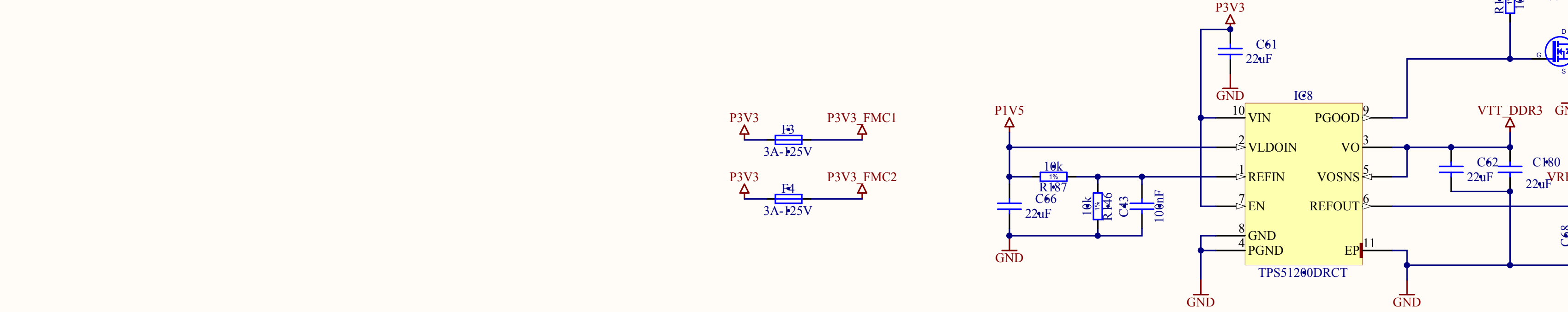
P3V3\_FMC2  
FMC slot 3A

P12V\_FMC1 1A  
P12V\_FMC2 1A

P3V3  
AFPGA+SFGPA (Vccaux, IO) 3A  
VME interface 1A

LAYOUT NOTES:

- Place the input capacitor close to the top switching FET. The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions Kelvin connections should be brought from the output to the feedback pin (FBx) of the device.
- Make a single point connection from the signal ground to power ground
- Do not allow switching current to flow under the device



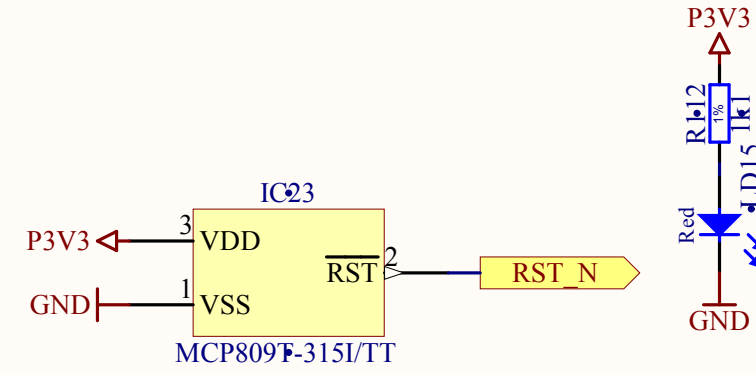
DC/DC calculations, Voripple=30mV

2.5V, I<sub>max</sub>=5.4A, L=1uH, R<sub>trip</sub> = 5670, C=50uF, IL<sub>peak</sub>=3.75A

1.2V, I<sub>max</sub>=4A, L=1uH, R<sub>trip</sub>=4200, C=80uF, IL<sub>peak</sub>=6A

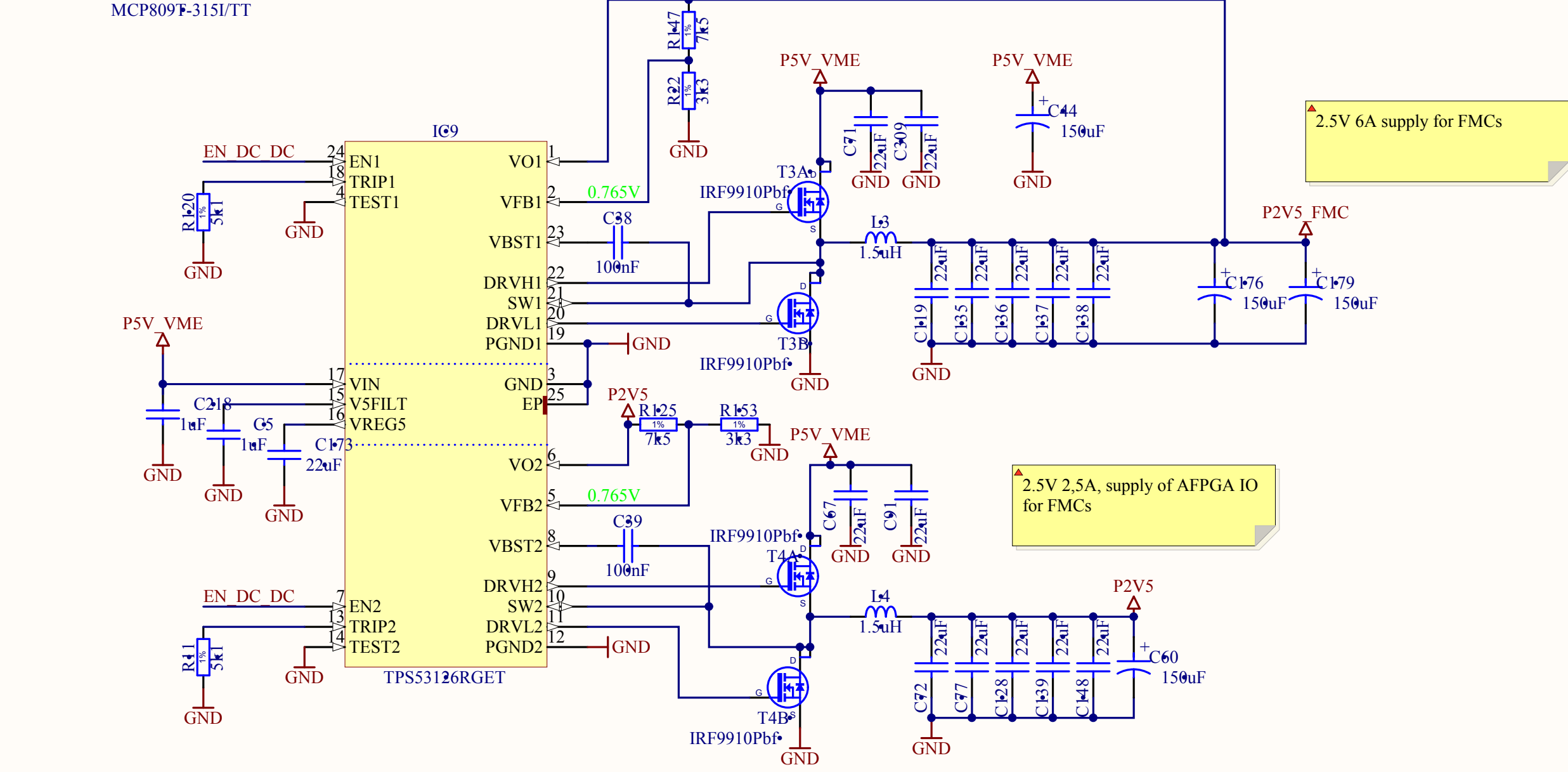
2.5V, I<sub>max</sub>=4A, L=1uH, R<sub>trip</sub> = 4200, C=80uF, IL<sub>peak</sub>=6A

1.5V, I<sub>max</sub>=4A, L=1uH, R<sub>trip</sub>=4200, C=33uF, IL<sub>peak</sub>=6A

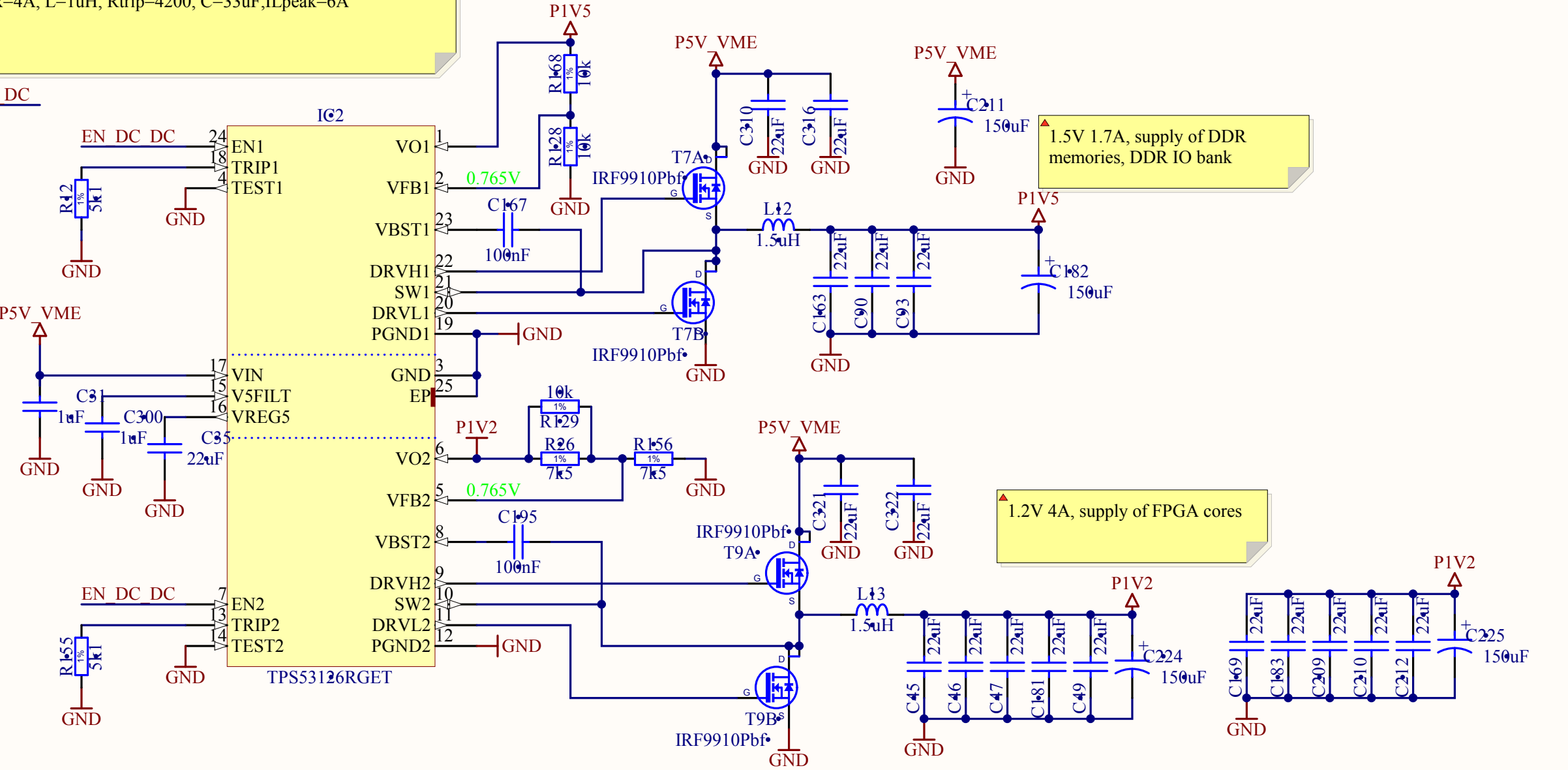


- B1 → P5V\_VME
- B6 → P1V2
- B2 → P1V8
- B5 → P12V
- B8 → P3V3
- B9 → P2V5
- B10 → GND

2.5V 6A supply for FMCs



2.5V 2.5A, supply of AFPGA IO for FMCs



1.5V 1.7A, supply of DDR memories, DDR IO bank

1.2V 4A, supply of FPGA cores

Project/Equipment		Simple VME Carrier Board	
Document		Designer	G.Kasprowicz
BE-CO		Drawn by	G.Kasprowicz
		Check by	T.Janicki
		Last Mod.	2012-05-01
		File	Power_supplies.SchDoc
		Print Date	2012-05-01 22:22:58
		Sheet	14 of 21
		Size	A3
		Rev	-

European Organization for Nuclear Research  
CH-1211 Geneva 23 - Switzerland

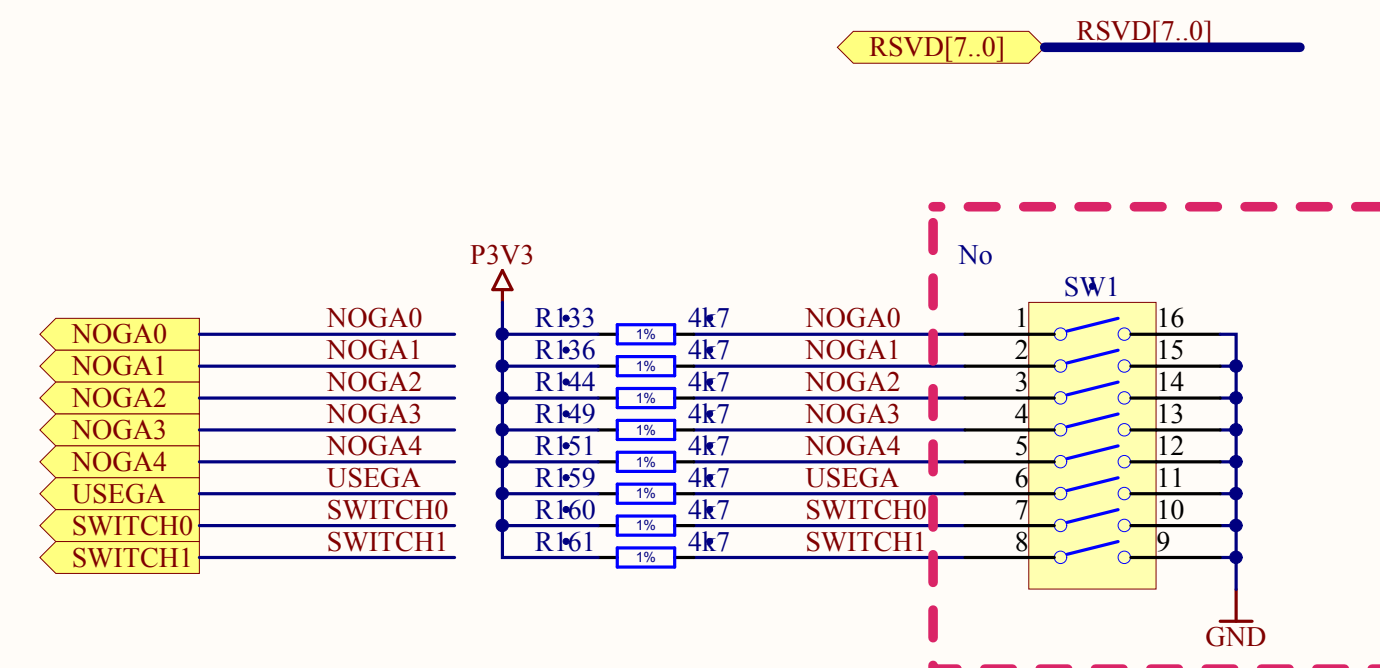
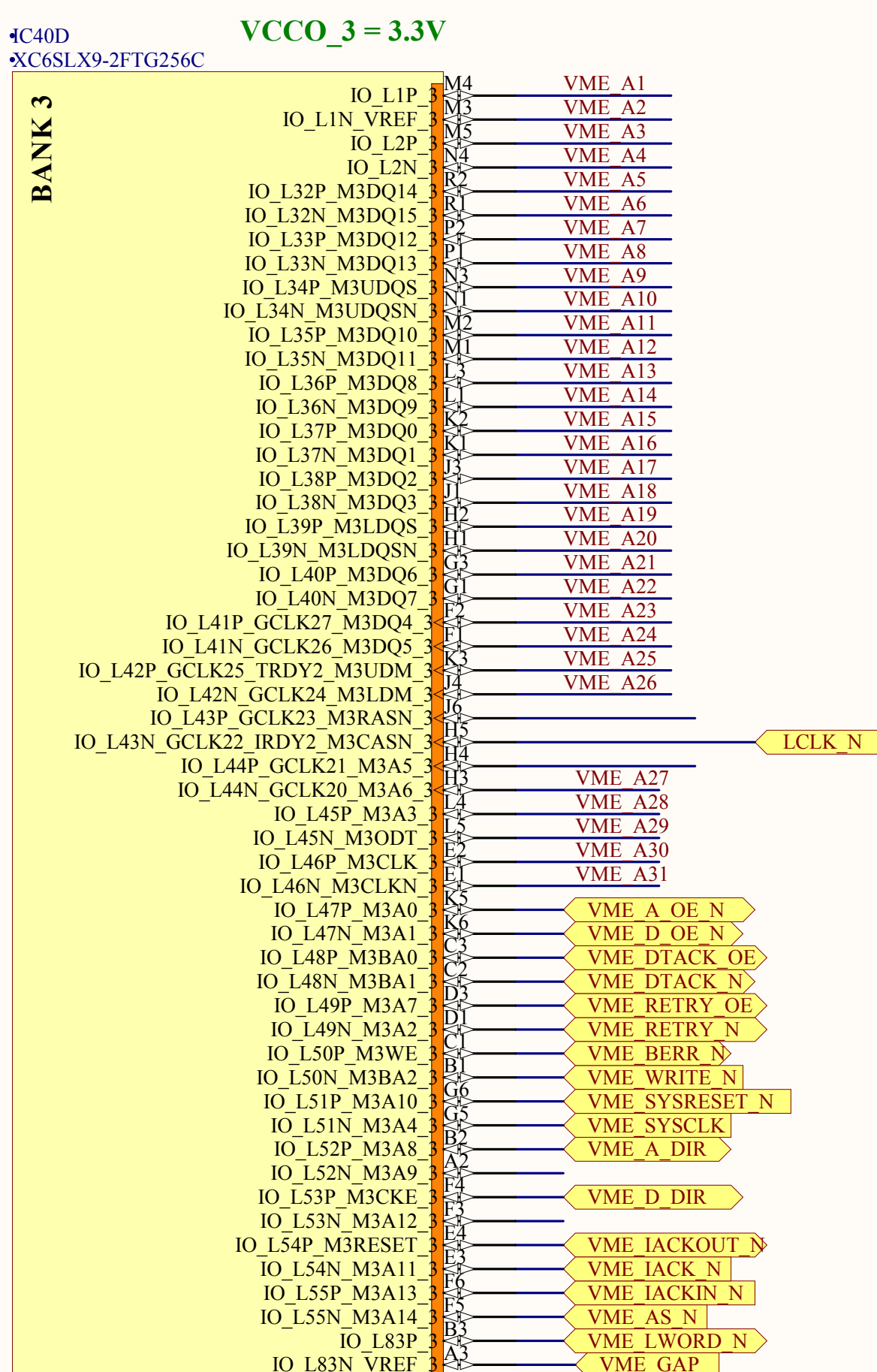
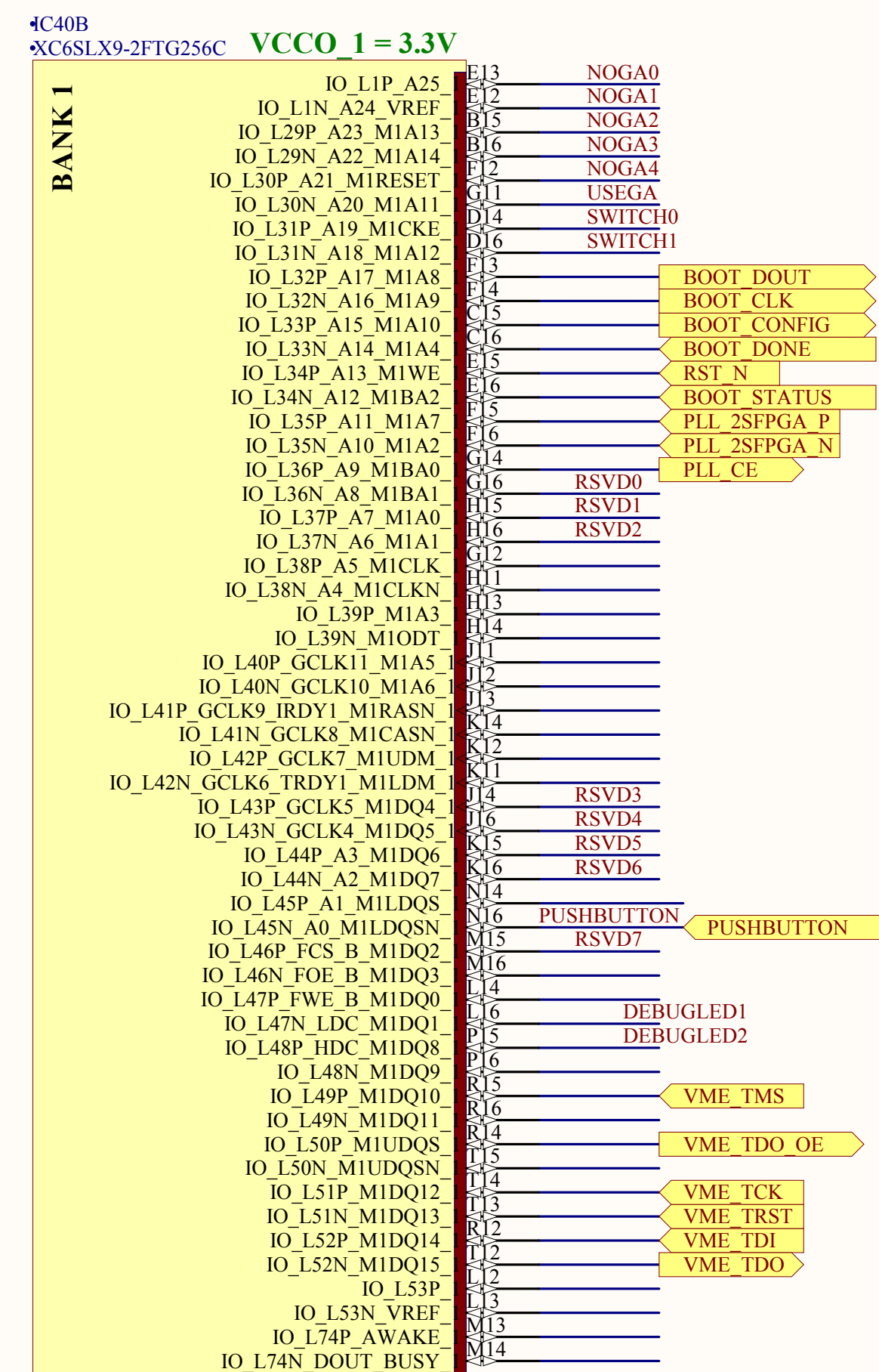
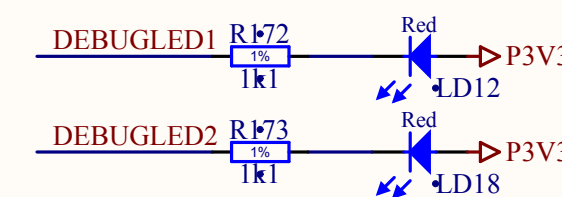
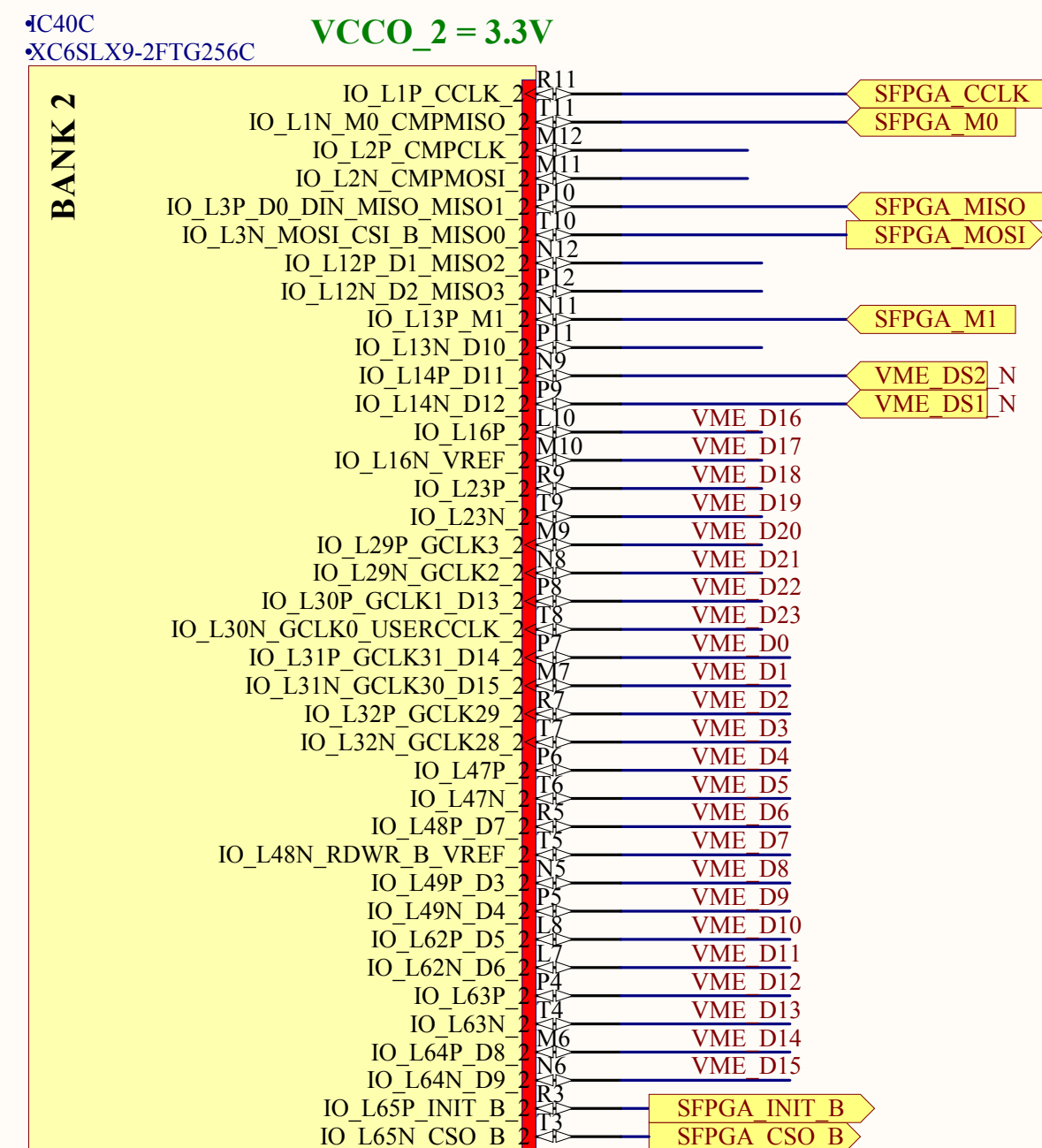
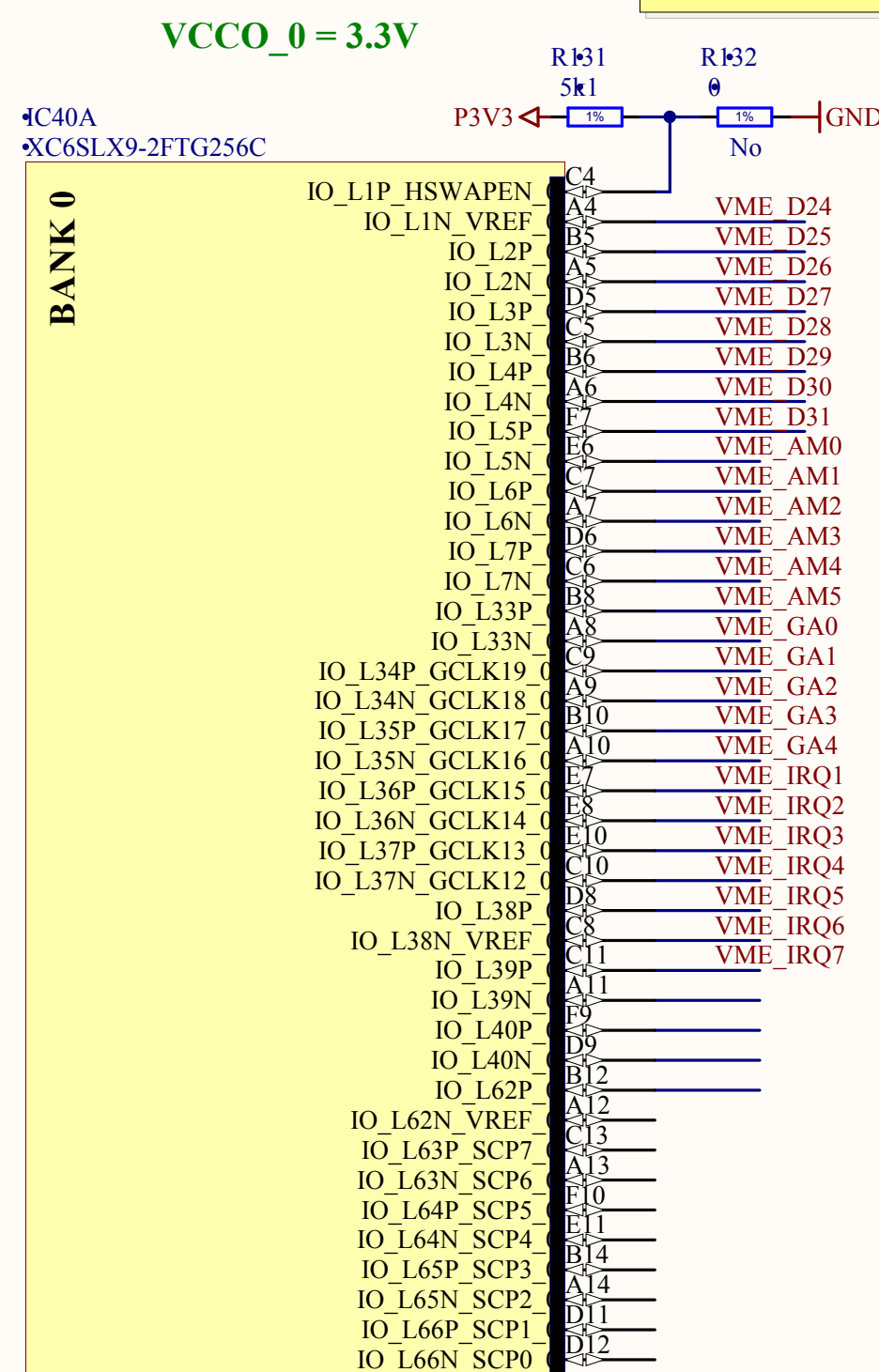
EDA-xxxx



Copyright CERN 2011.

This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>).

This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.



NOT MOUNTED BY DEFAULT

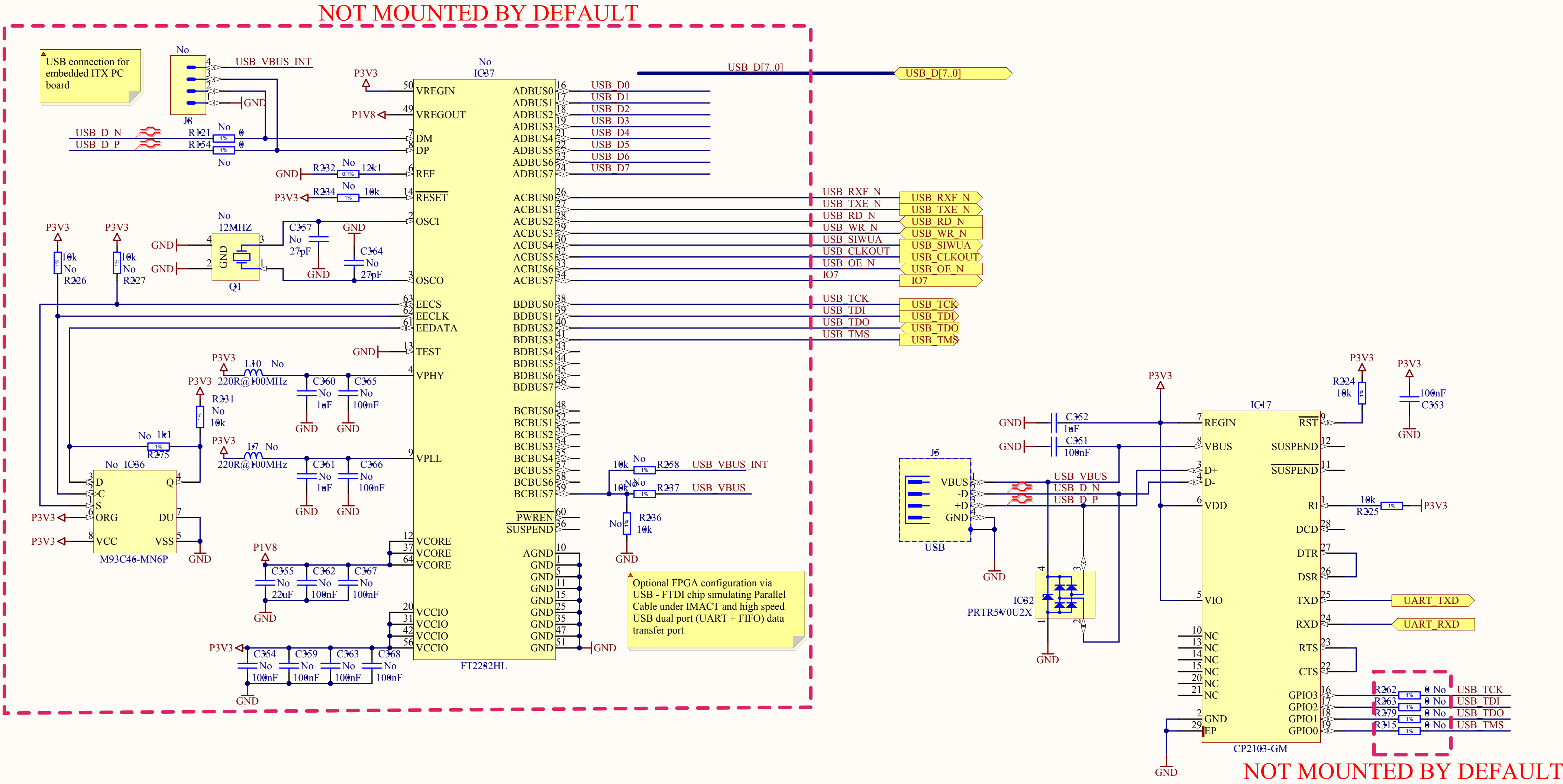




Copyright CERN 2011.

This documentation describes Open Hardware and is licensed under the CERN OHL v. 1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>).

This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.



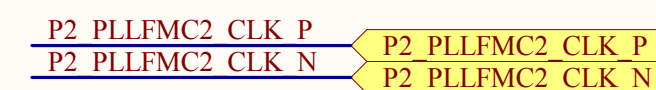
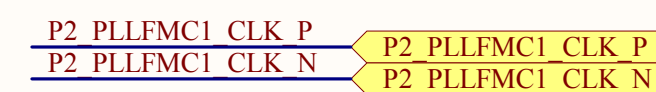
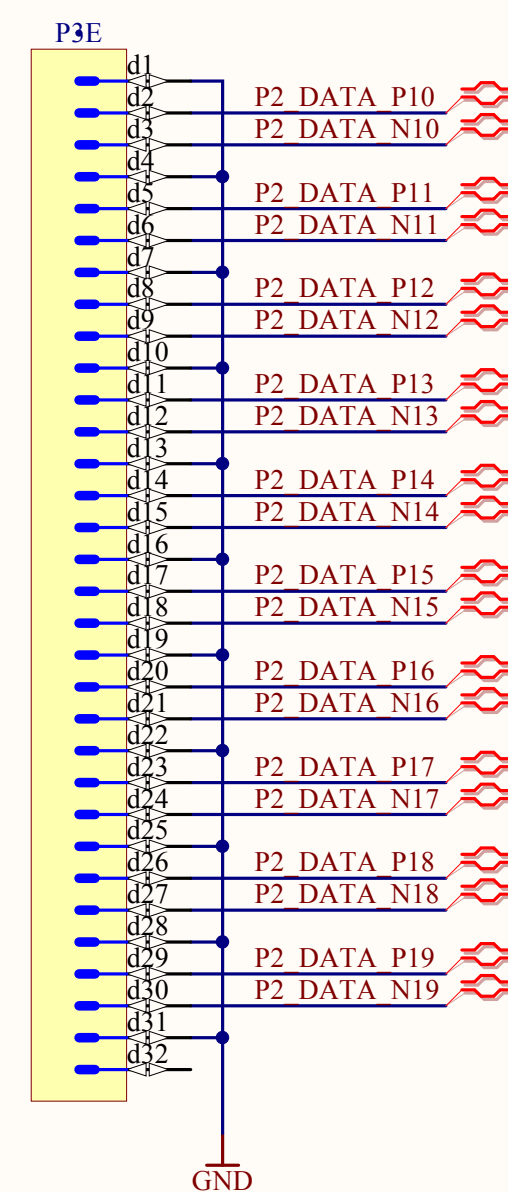
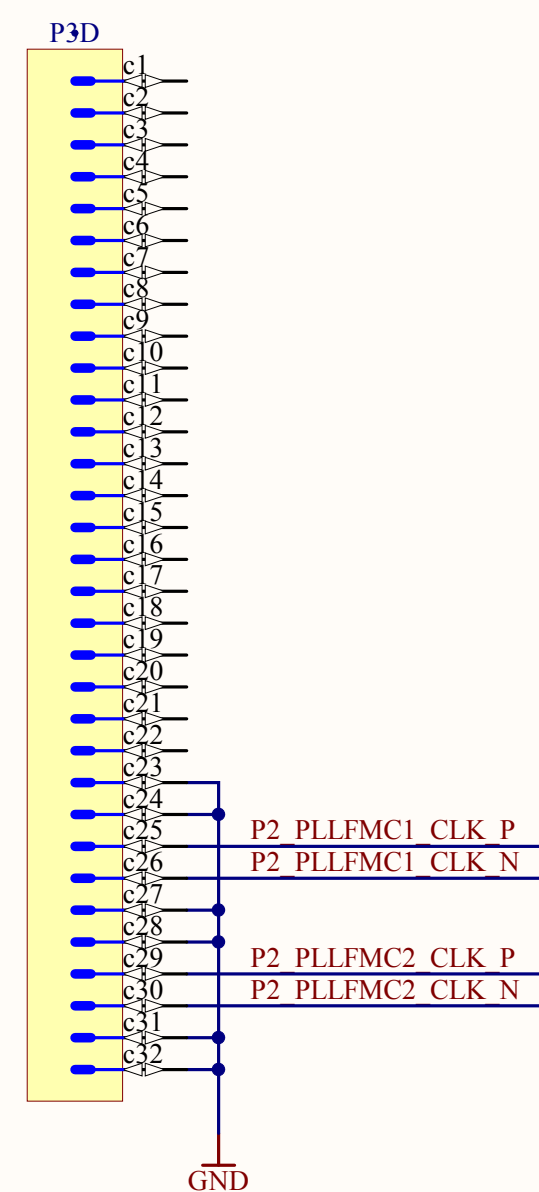
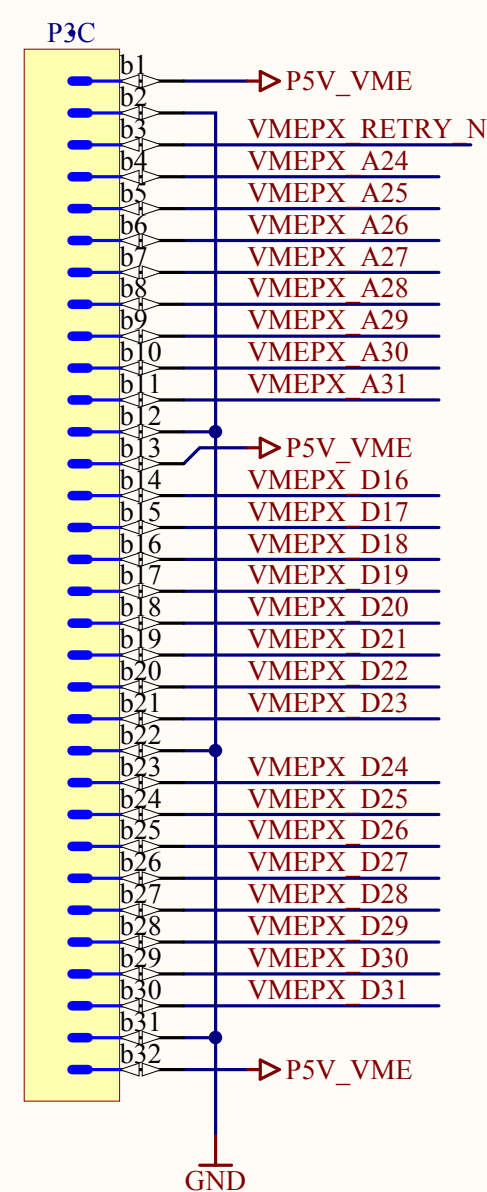
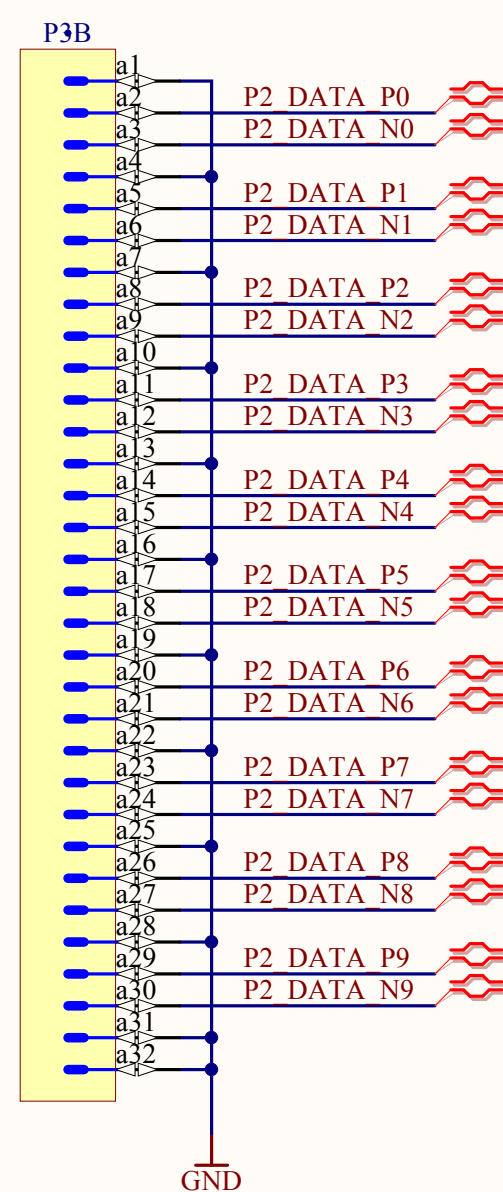
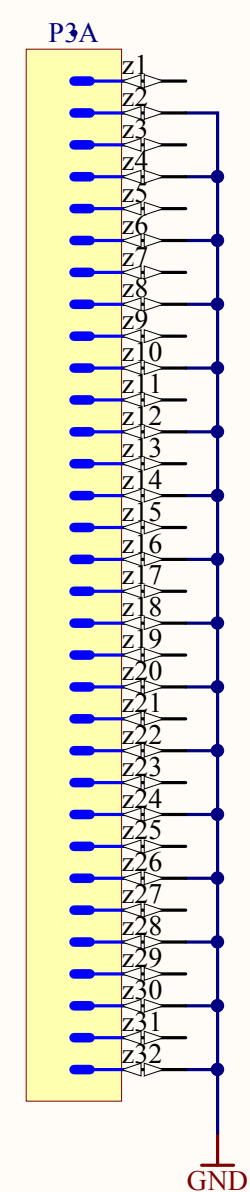
Project/Equipment		Simple VME FMC Carrier	
Document		Designer	G.Kasprowicz
<div>BE-CO</div> <div></div>		Drawn by	G. Kasprowicz
		Check by	T. Janicki
		Last Mod.	2012-05-01
		File	USB_interface.SchDoc
Print Date		2012-05-01 22:22:59	Sheet 17 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-xxxx	Size A3 Rev -



Copyright CERN 2011.

This documentation describes Open Hardware and is licensed under the CERN OHL v.1.1. You may redistribute and modify this documentation under the terms of the CERN OHL v.1.1. (<http://ohwr.org/CERNOHL>).

This documentation is distributed WITHOUT ANY EXPRESS OR IMPLIED WARRANTY, INCLUDING OF MERCHANTABILITY, SATISFACTORY QUALITY AND FITNESS FOR A PARTICULAR PURPOSE. Please see the CERN OHL v.1.1 for applicable conditions.



100ohms diff. pairs

