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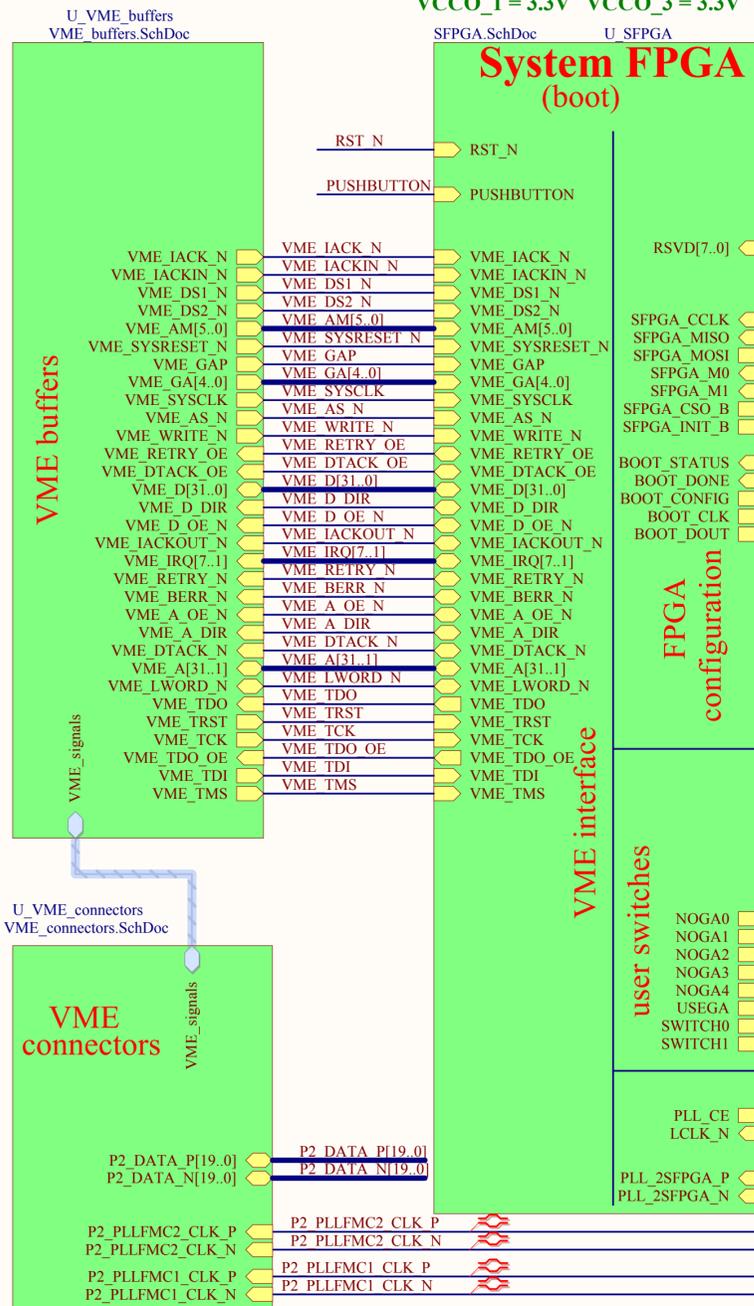
U_AFPGA_power
AFPGA_power.SchDoc
Application FPGA supply

U_SFPGA_power
SFPGA_power.SchDoc
System FPGA supply

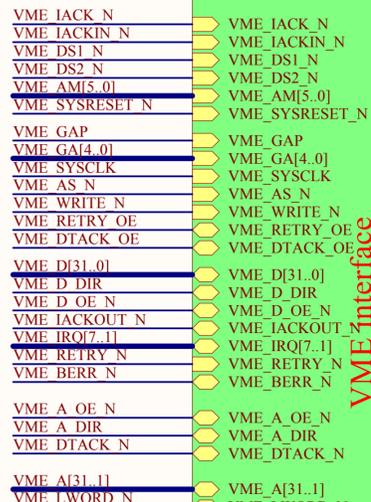
B16
B17
B18
B19
B20
B21
stand-alone version mounting holes

Power_supplies.SchDocU_PowerSupplies
RST_N **switching power supply**

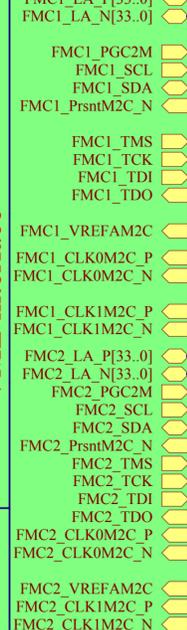
VCCO_0 = 3.3V VCCO_2 = 3.3V
VCCO_1 = 3.3V VCCO_3 = 3.3V



AFPGA.SchDoc U_AFPGA
ApplicationFPGA

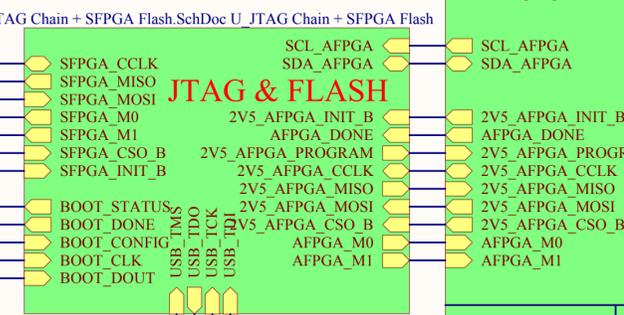
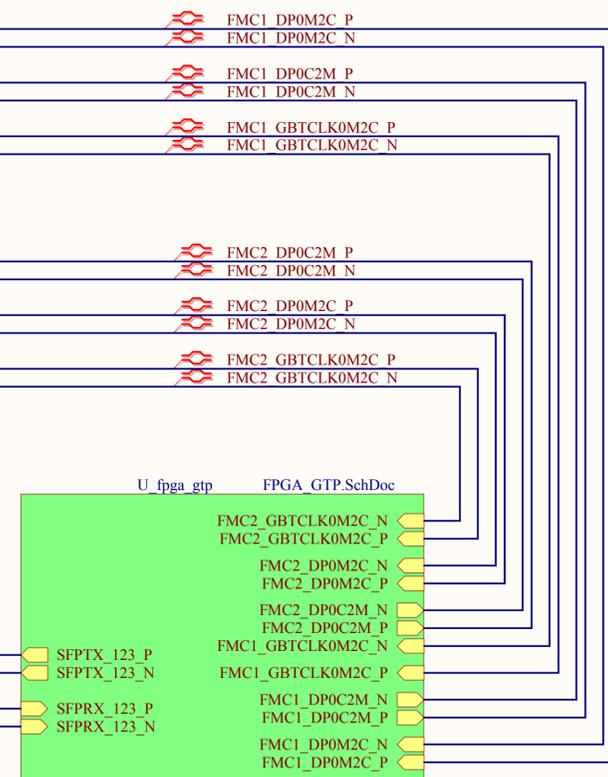
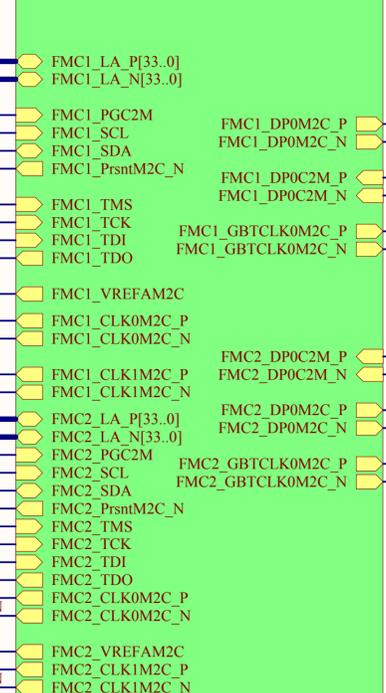


FMC control

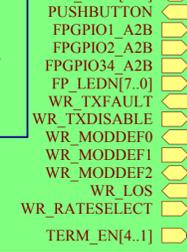


VCCO_0 = 2.5V VCCO_2 = 2.5V
VCCO_1 = 3.3V VCCO_3 = 3.3V
FMC_connectors.SchDoc U_FmcConnectors

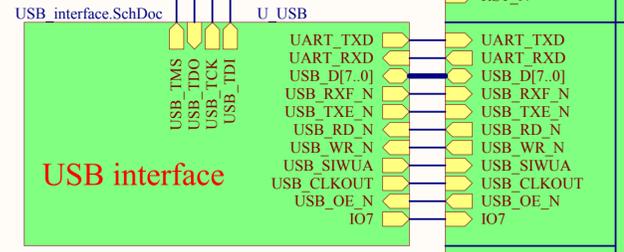
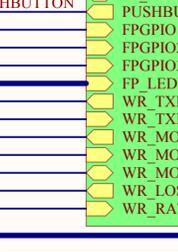
FMC connectors



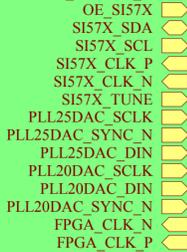
front panel



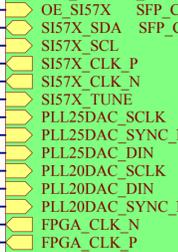
front panel



clock control



clock generators

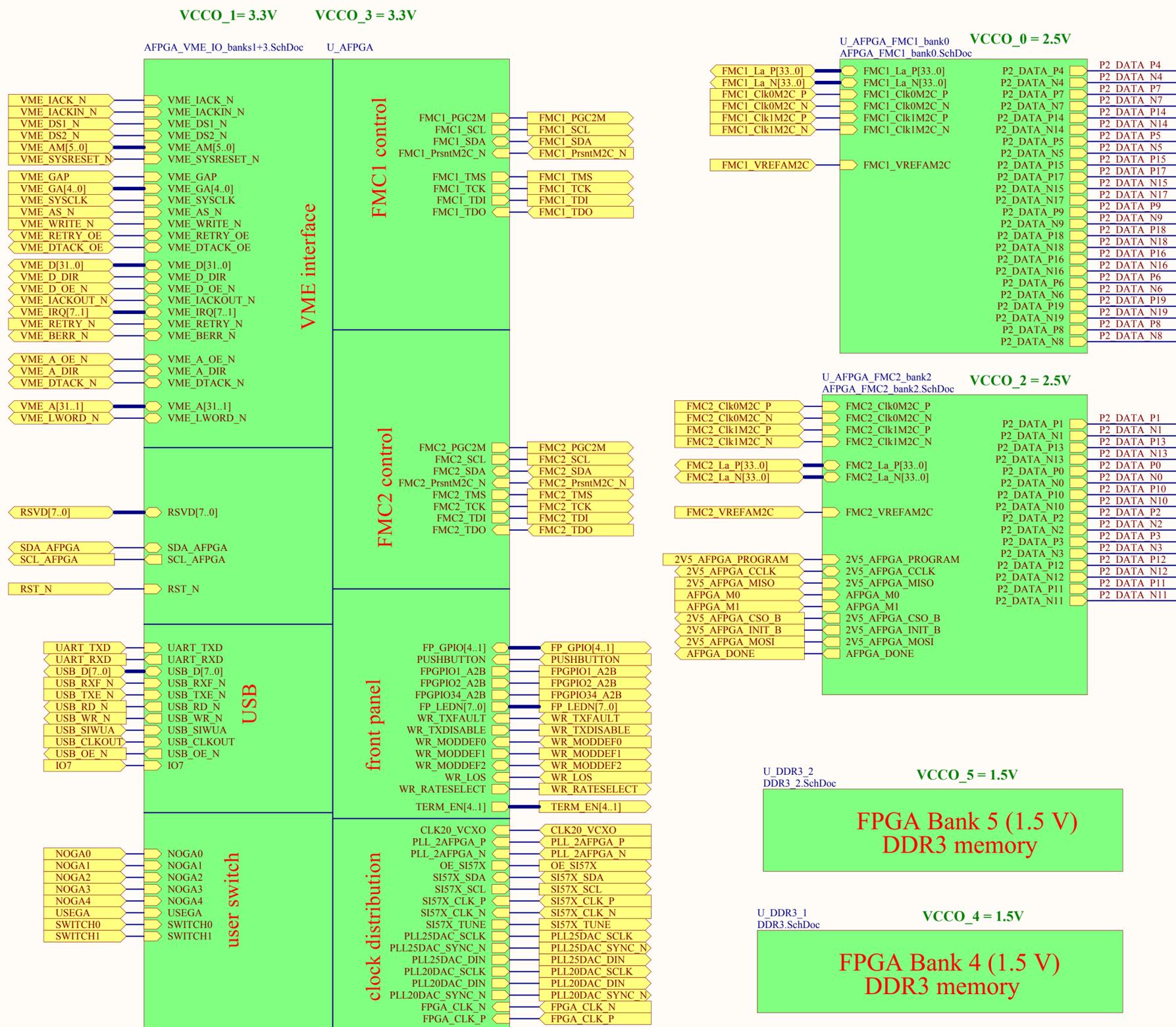


Project/Equipment	Simple VME FMC Carrier	Designer	G.Kasprowicz	20/11/2012
Document	Simple VME FMC Carrier	Drawn by	G.Kasprowicz	30/04/2012
	top	Check by	T.Janicke	2012-05-01
		Last Mod.	-	-
File	SVEC_top.SchDoc	Print Date	2012-05-01 22:22:56	Sheet 1 of 21
		Size	A3	Rev -

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EDA-xxxx

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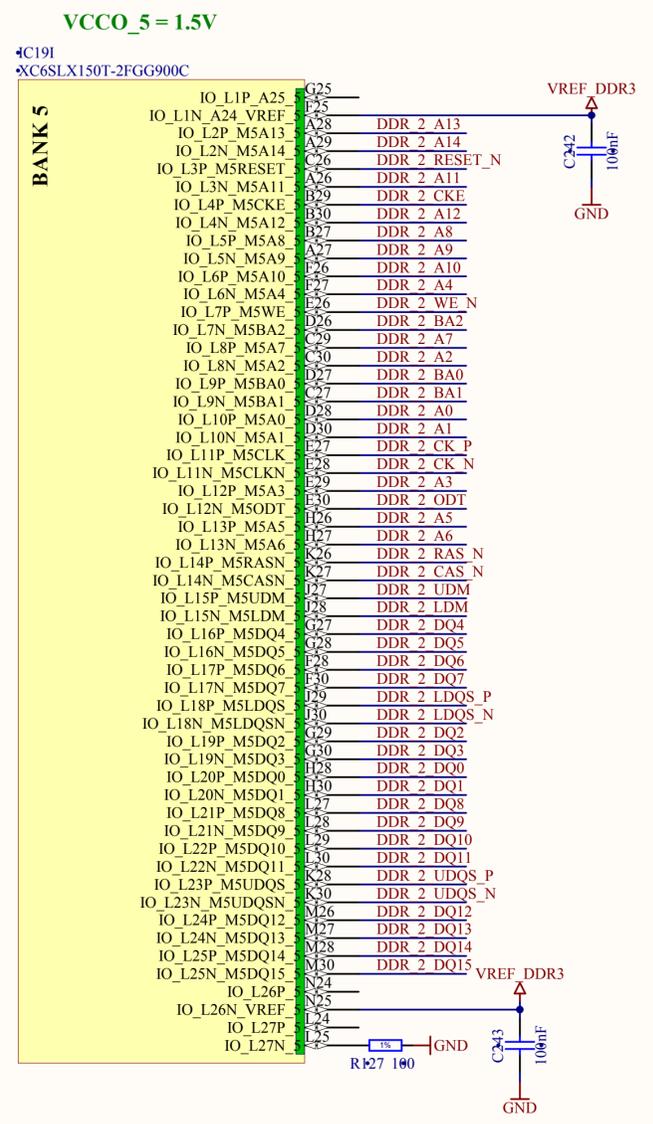
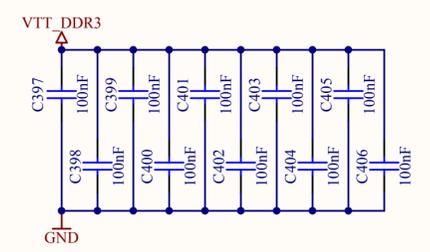
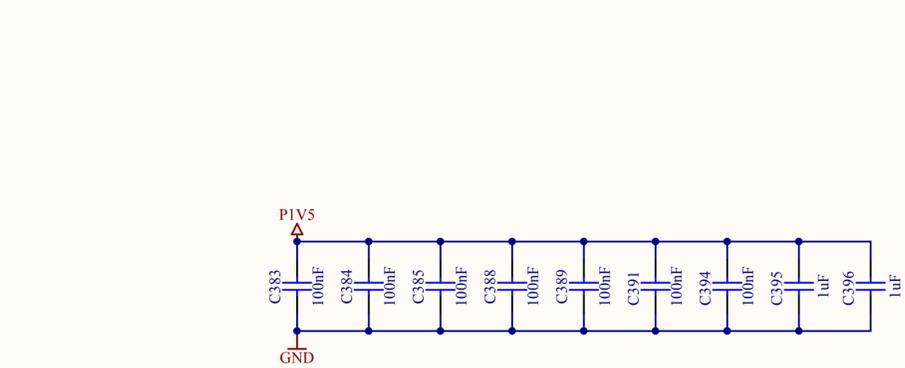
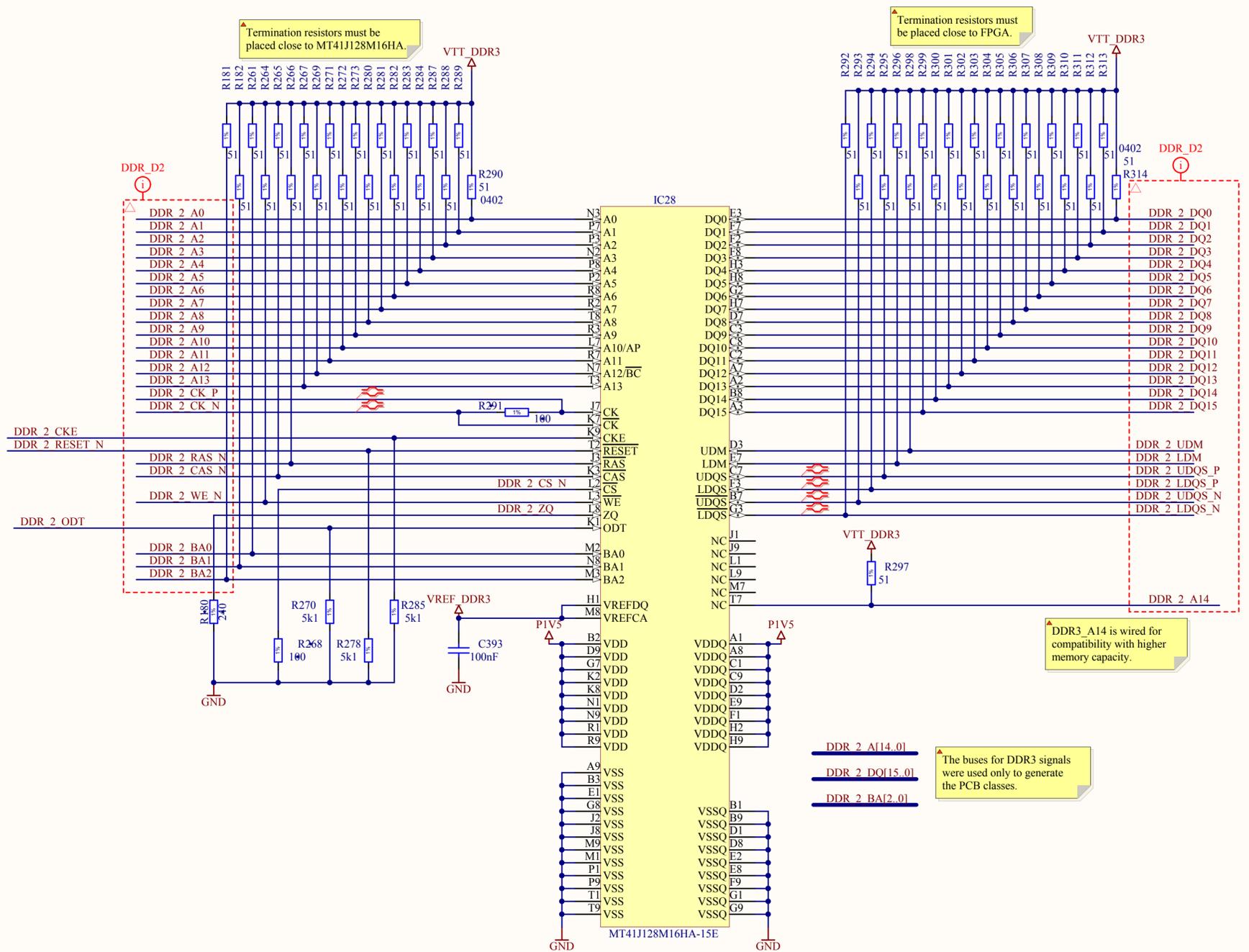


Project/Equipment		Simple VME FMC Carrier	
Document		<i>Application FPGA</i>	
BE-CO	Designer	G.Kasprowicz	20/11/2012
	Drawn by	G.Kasprowicz	30/04/2012
CERN	Check by	T.Janicke	2012-05-01
	Last Mod.	-	-
File		AFPGA.SchDoc	
Print Date		2012-05-01 22:22:56	Sheet 2 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-xxxx	Size A3 Rev -

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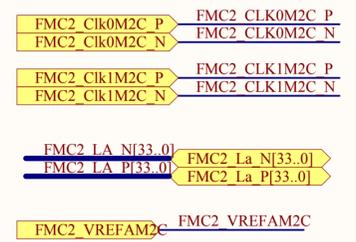
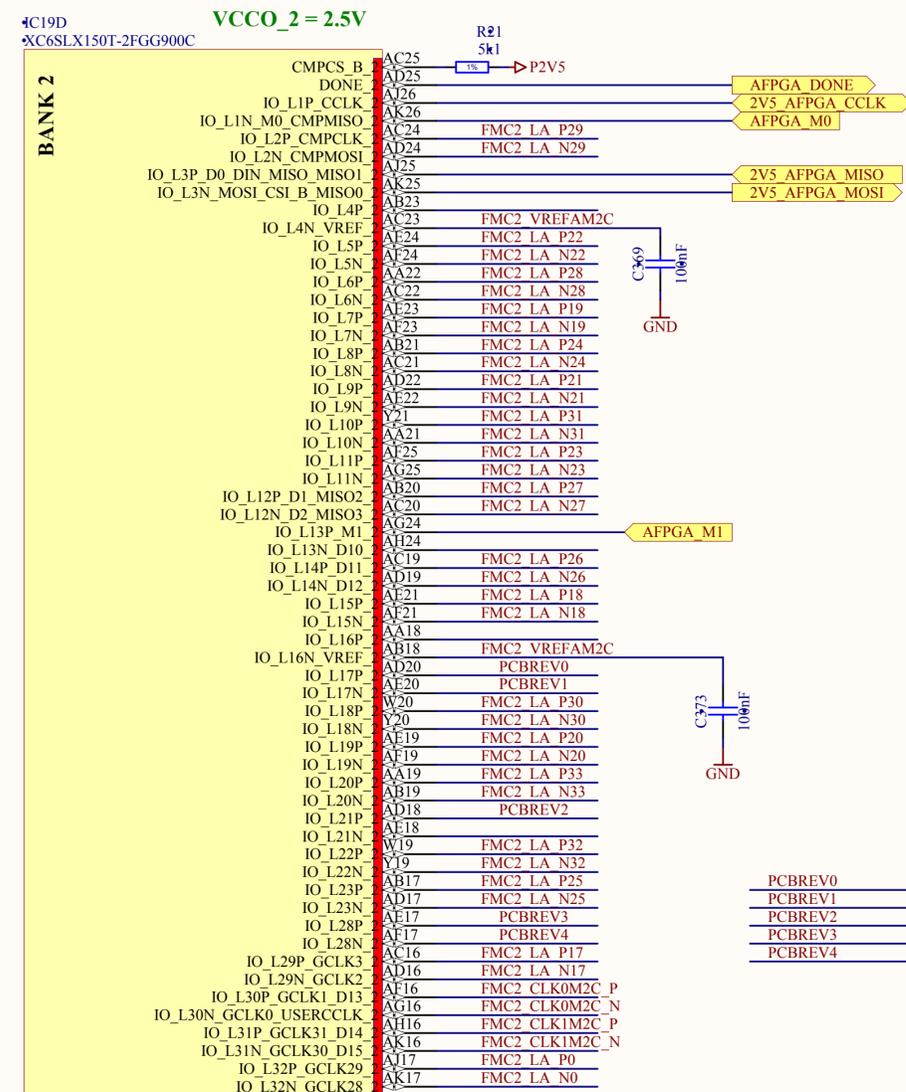
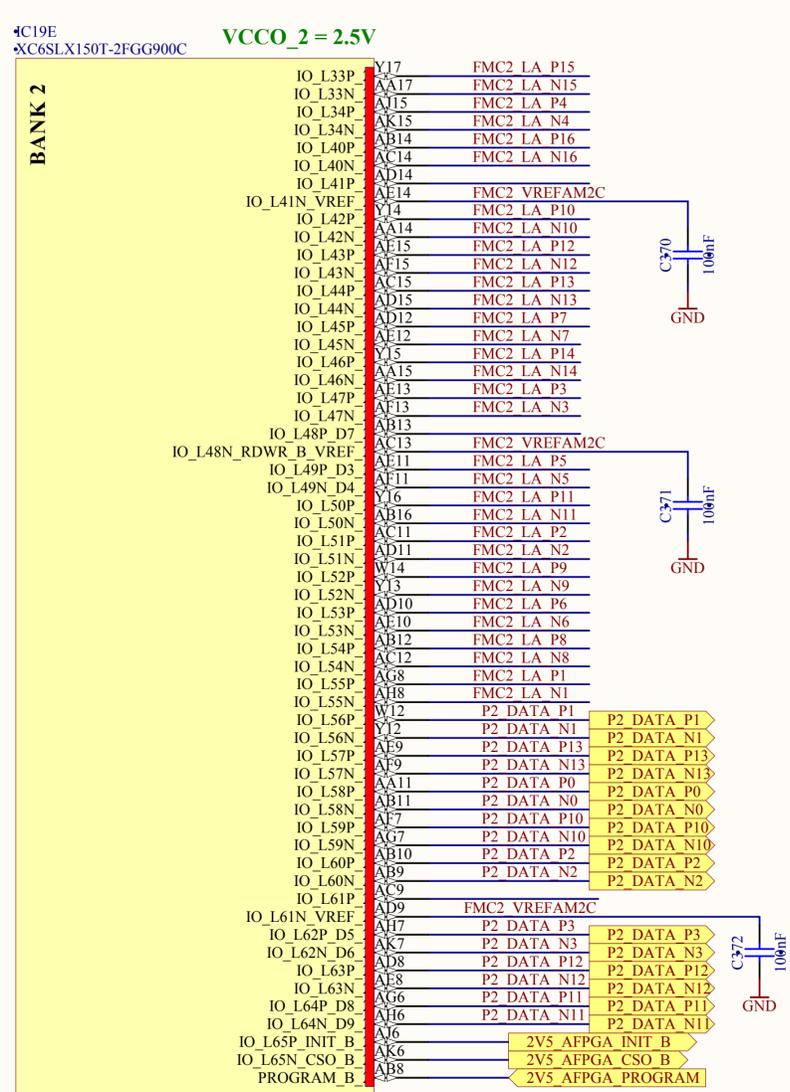
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Project/Equipment	Simple VME FMC Carrier	Designer	G.Kasprowicz
Document	DDR3 memory - bank 5 -	Drawn by	G.Kasprowicz
BE-CO	EDA-xxxx	Check by	T.Janicki
		Last Mod.	-
CERN	European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland	File	DDR3_2.SchDoc
		Print Date	2012-05-01 22:22:56
		Sheet	4 of 21
		Size	A3
		Rev	-

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Project/Equipment		Simple VME FMC Carrier	
Document		Designer G.Kasprowicz	
BE-CO		Drawn by G.Kasprowicz	
CERN		Check by T.Janicke	
		Last Mod. -	
		File AFPGA_FMC2_bank2.SchDoc	
		Print Date 2012-05-01 22:22:57	
		Sheet 6 of 21	
		Size A3	
		Rev -	

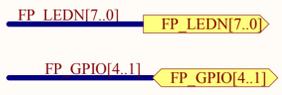
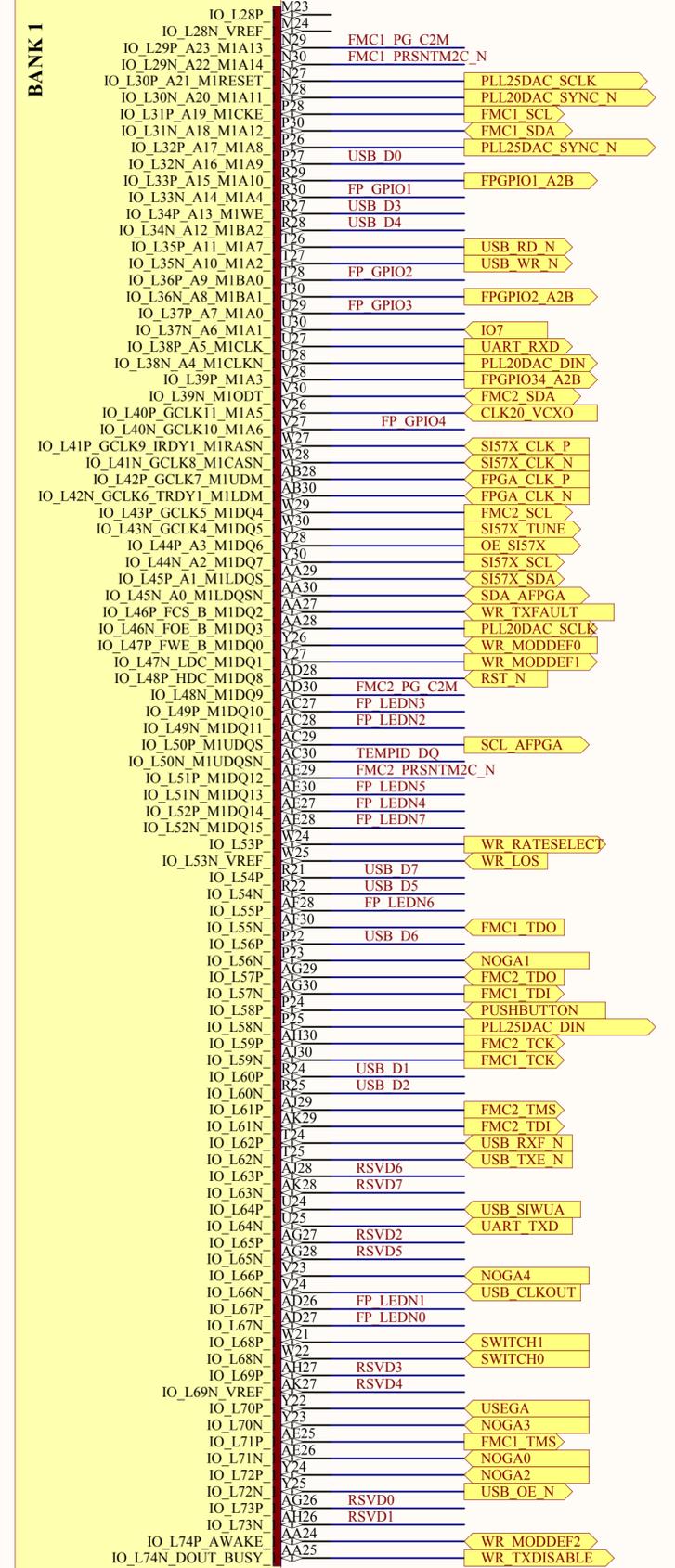
AFPGA FMC2
- bank 2 -

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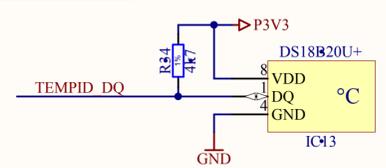
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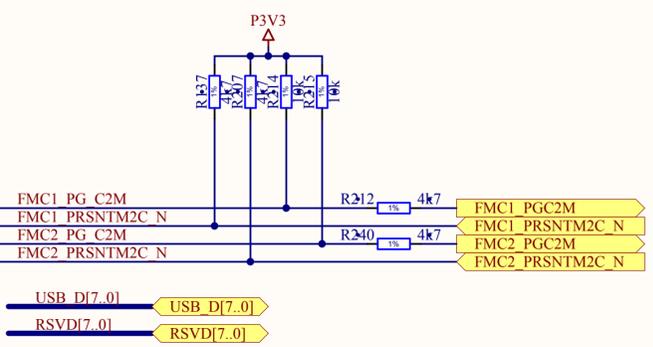
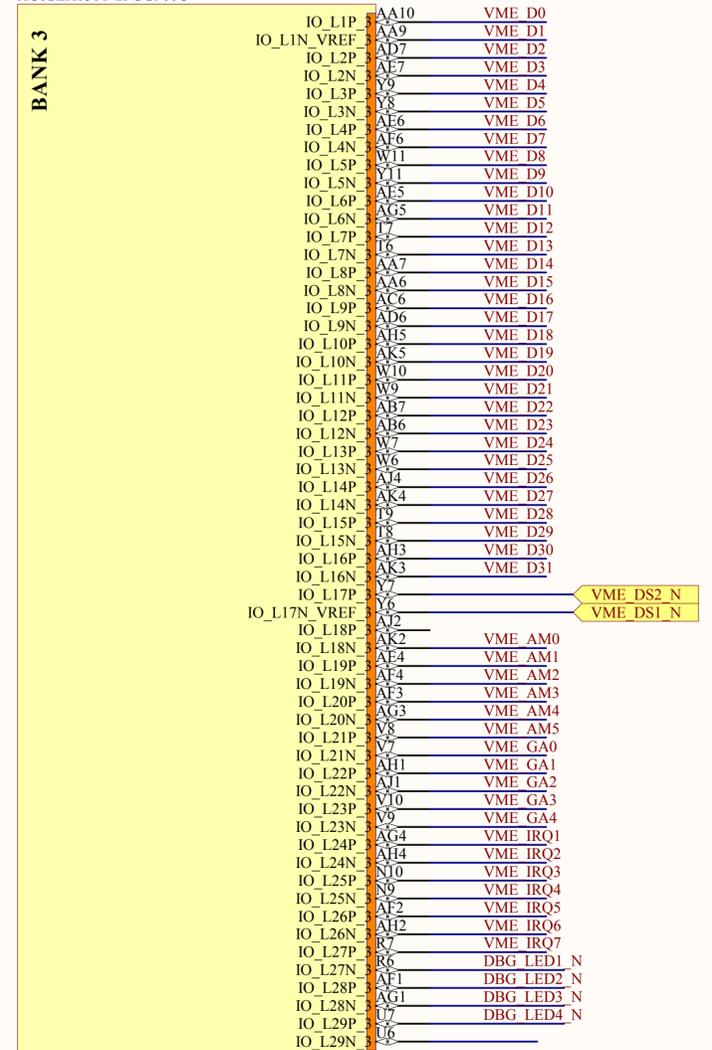
4C19C
XC6SLX150T-2FGG900C VCCO_1= 3.3V



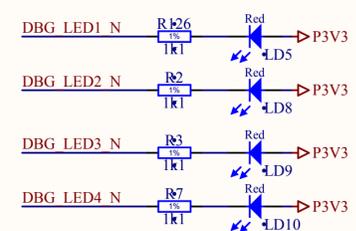
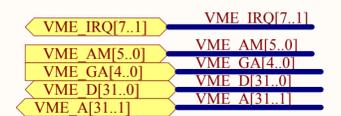
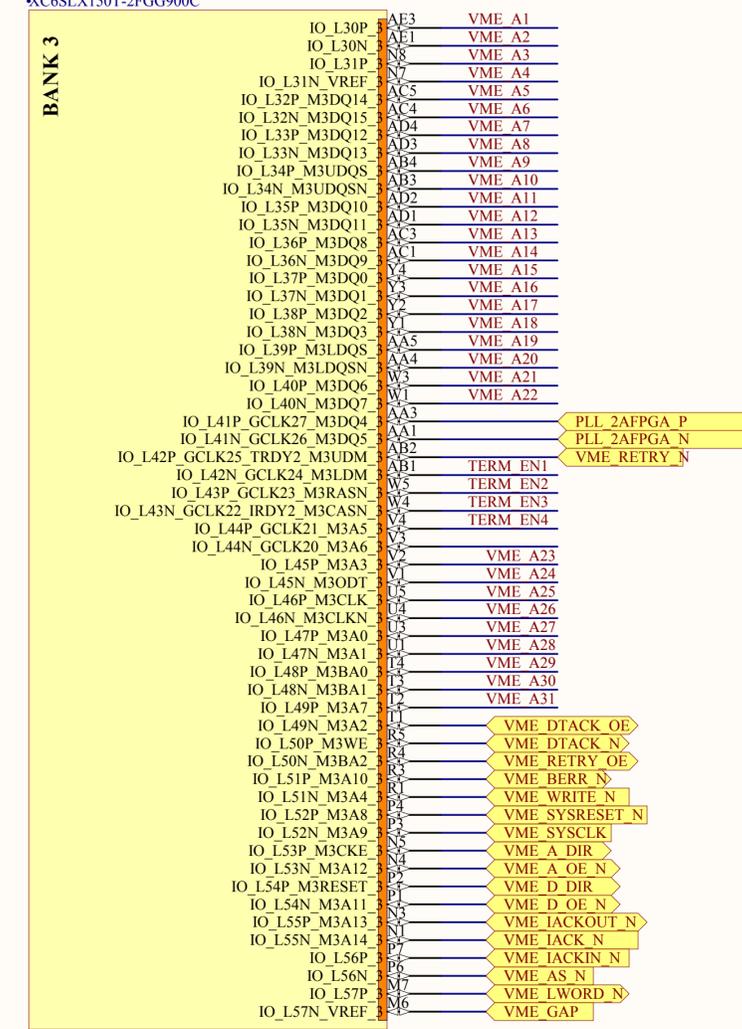
TERM_EN[4..1] TERM_EN[4..1]



4C19F
XC6SLX150T-2FGG900C VCCO_3 = 3.3V



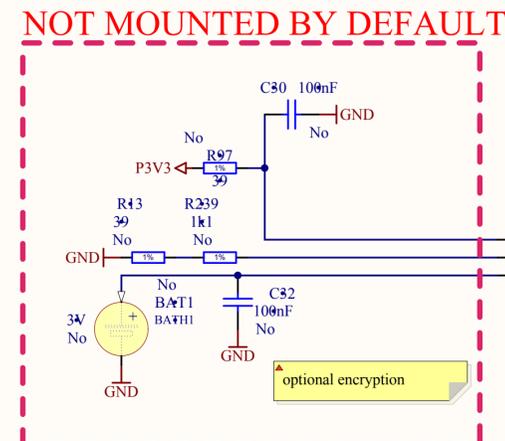
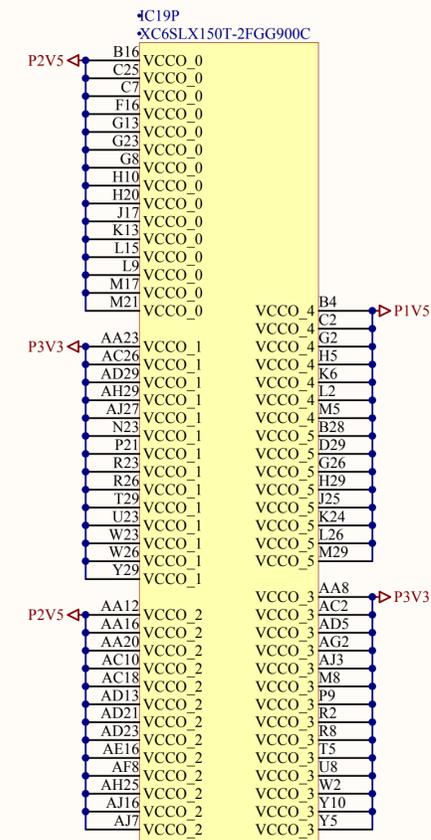
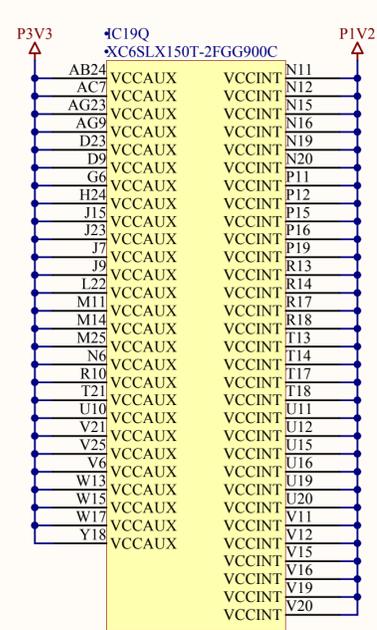
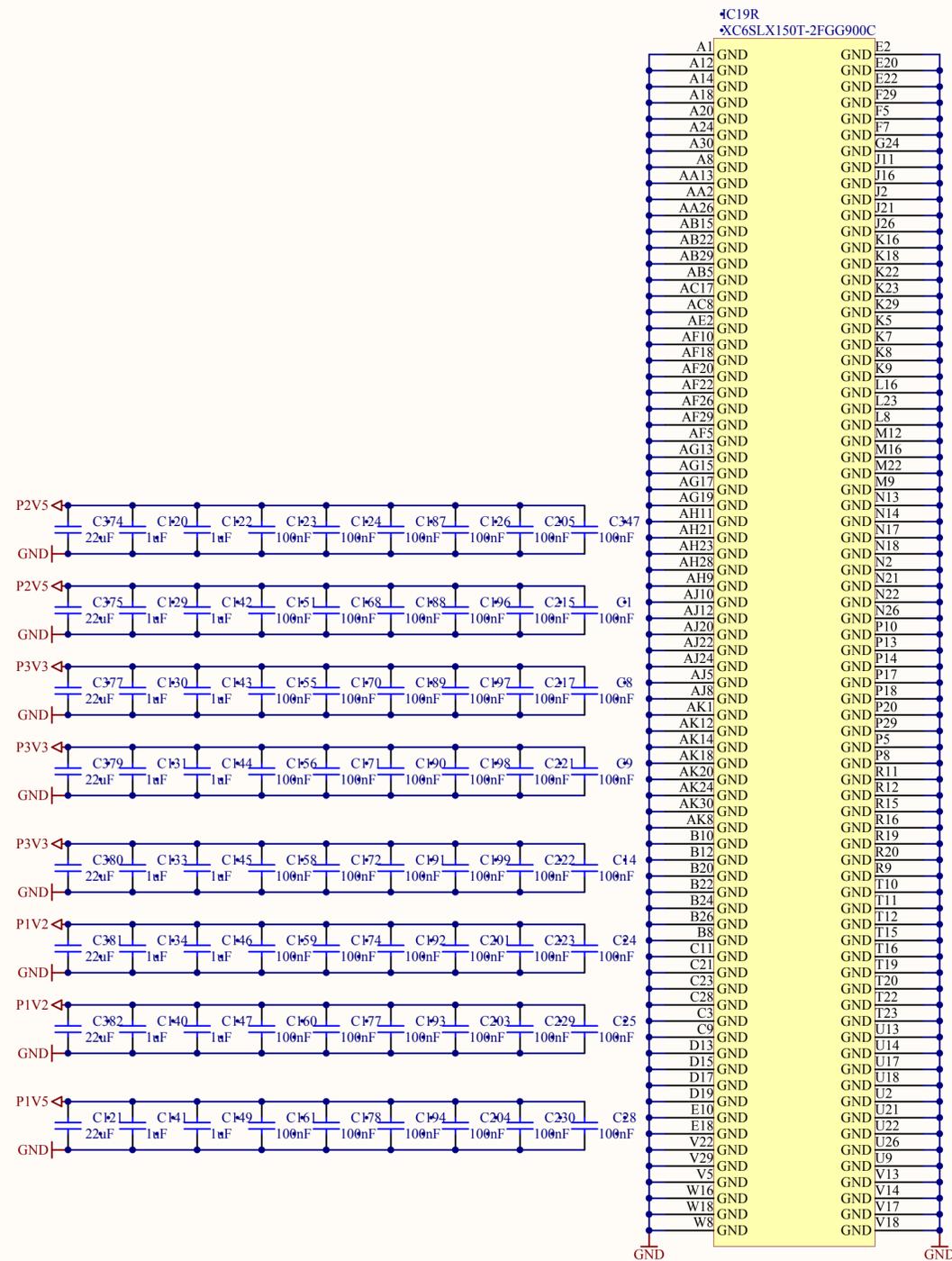
4C19G
XC6SLX150T-2FGG900C VCCO_3 = 3.3V



Project/Equipment	Simple VME FMC Carrier	Designer	G.Kasprowicz	20/11/2012
Document	AFPGA VME & IO - banks 1 & 3 -	Drawn by	G.Kasprowicz	30/04/2012
BE-CO		Check by	T.Janicke	2012-05-01
		Last Mod.	-	2012-05-01
		File	AFPGA_VME_IO_banks1+3.SchDoc	
		Print Date	2012-05-01 22:22:57	Sheet 7 of 21
			European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland	Size A3 Rev -
			EDA-xxxx	

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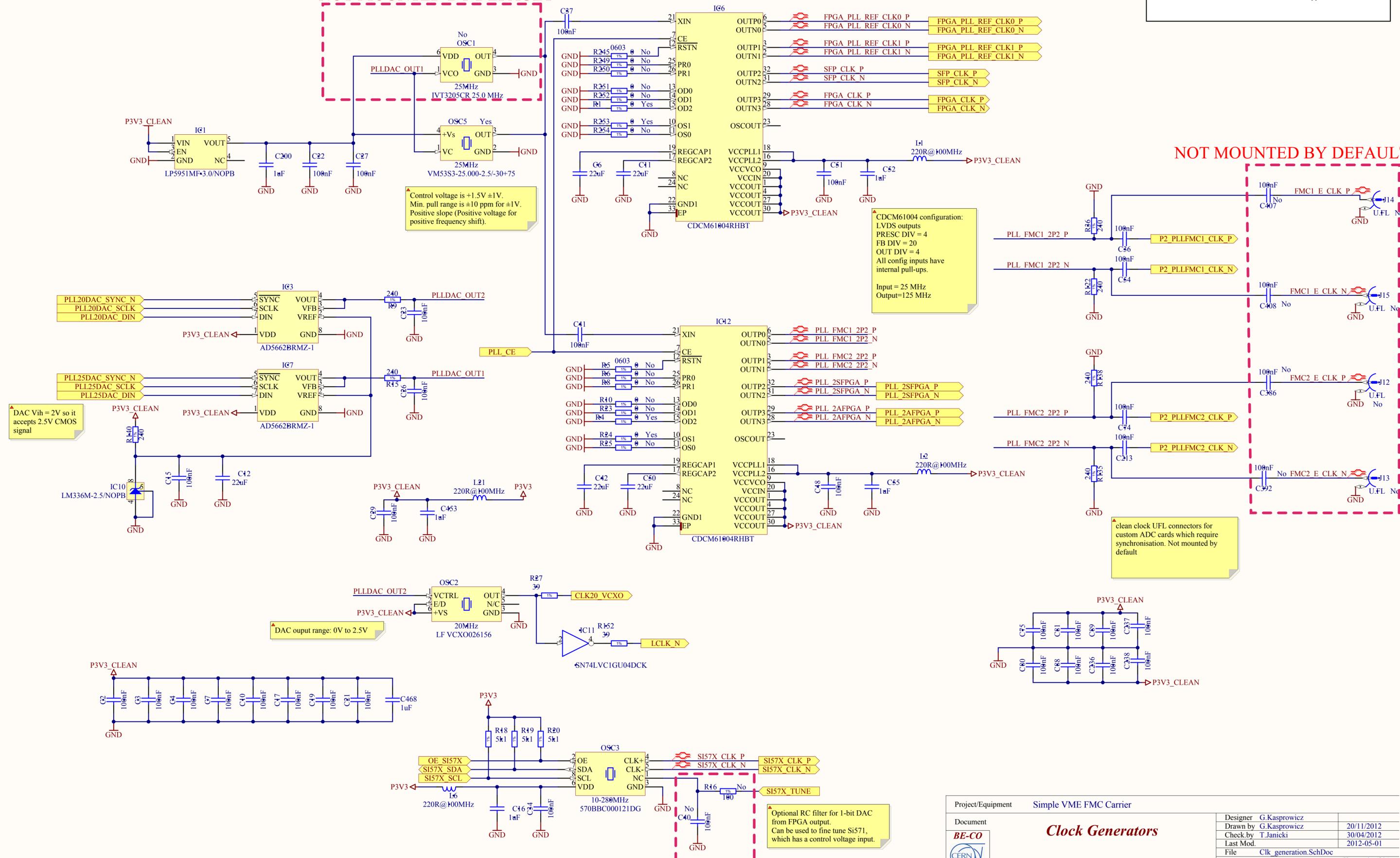
On-chip differential termination is specified with a nominal value of 100R when VCCAUX = 3.3V. The on-chip differential termination can be used when VCCAUX = 2.5V, however a wider resistance range is specified. (http://www.xilinx.com/support/documentation/user_guides/ug381.pdf, page 14). Moreover storage of the AES keys requires VCCAUX of at least 3V



Project/Equipment	Simple VME FMC Carrier	Designer	G.Kasprowicz
Document	Application FPGA power supply	Drawn by	G.Kasprowicz
BE-CO		Check by	T.Janicke
	European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland	Last Mod.	2012-05-01
	File	AFPGA_power.SchDoc	Print Date
		Sheet	8 of 21
		Size	A3
		Rev	-

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NOT MOUNTED BY DEFAULT



NOT MOUNTED BY DEFAULT

clean clock UFL connectors for custom ADC cards which require synchronisation. Not mounted by default

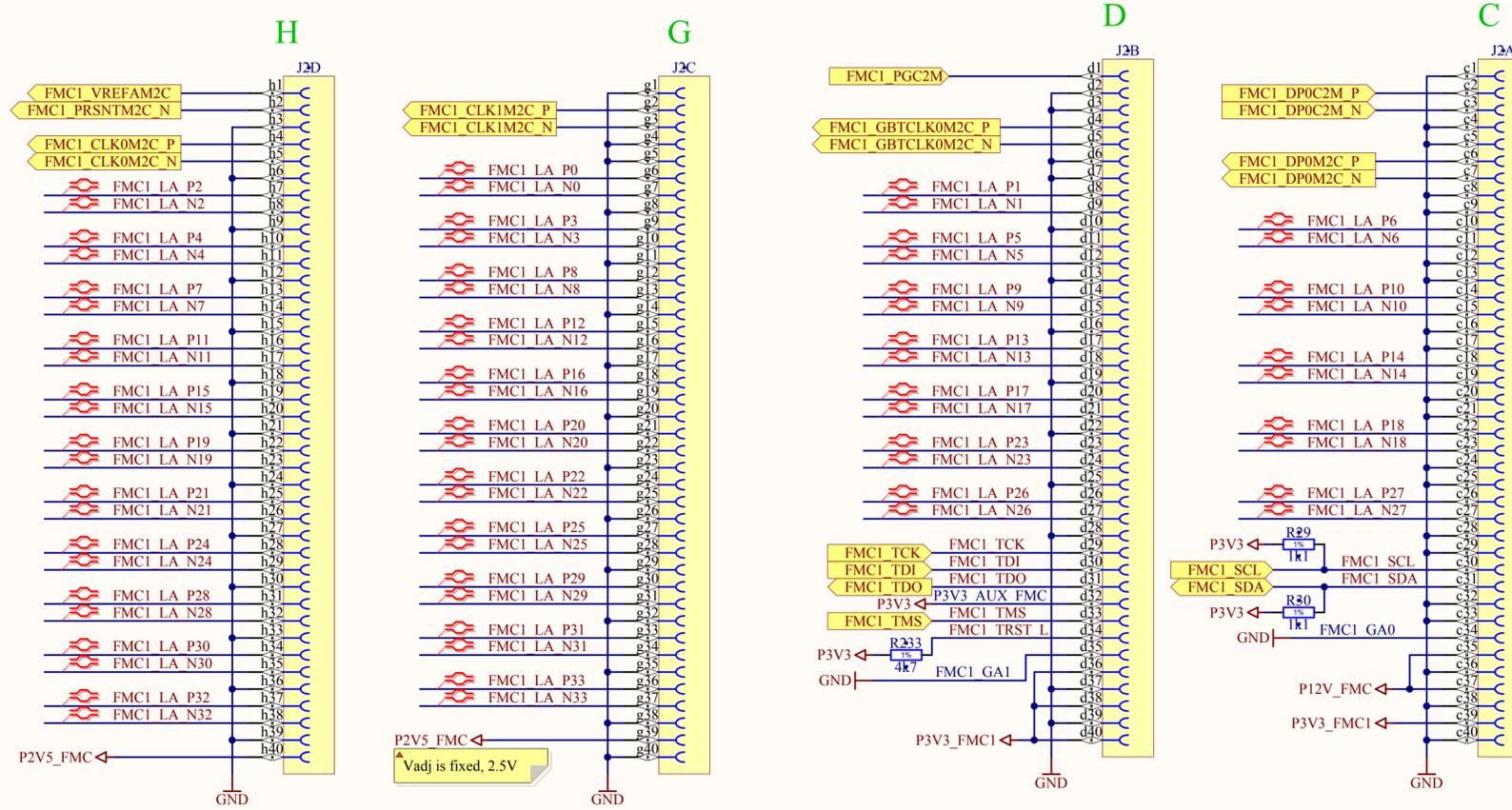
Optional RC filter for 1-bit DAC from FPGA output. Can be used to fine tune Si571, which has a control voltage input.

NOT MOUNTED BY DEFAULT

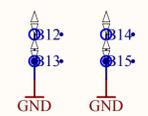
Project/Equipment	Simple VME FMC Carrier	
Document	Clock Generators	
Designer	G.Kasprowicz	20/11/2012
Drawn by	G.Kasprowicz	30/04/2012
Check by	T.Janicke	2012-05-01
Last Mod.		
File	Clk_generation.SchDoc	
Print Date	2012-05-01 22:22:57	Sheet 9 of 21
Size	A3	Rev -
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		
EDA-xxxx		

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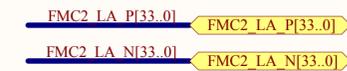
FMC slot 1



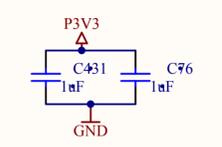
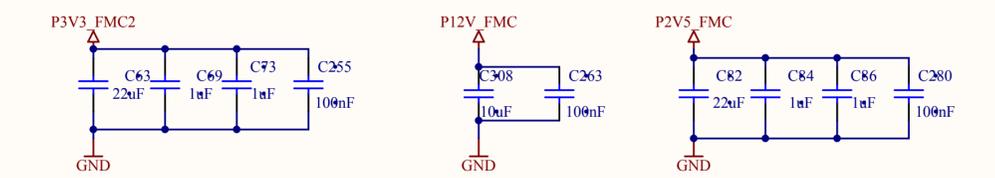
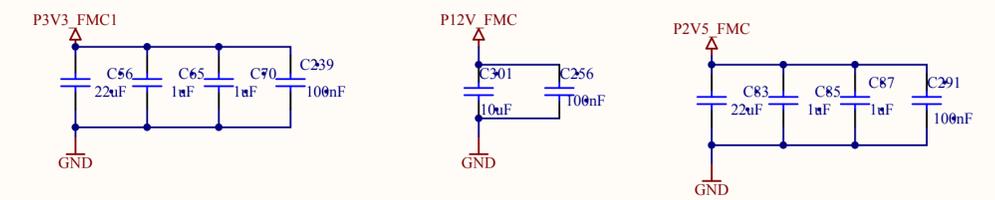
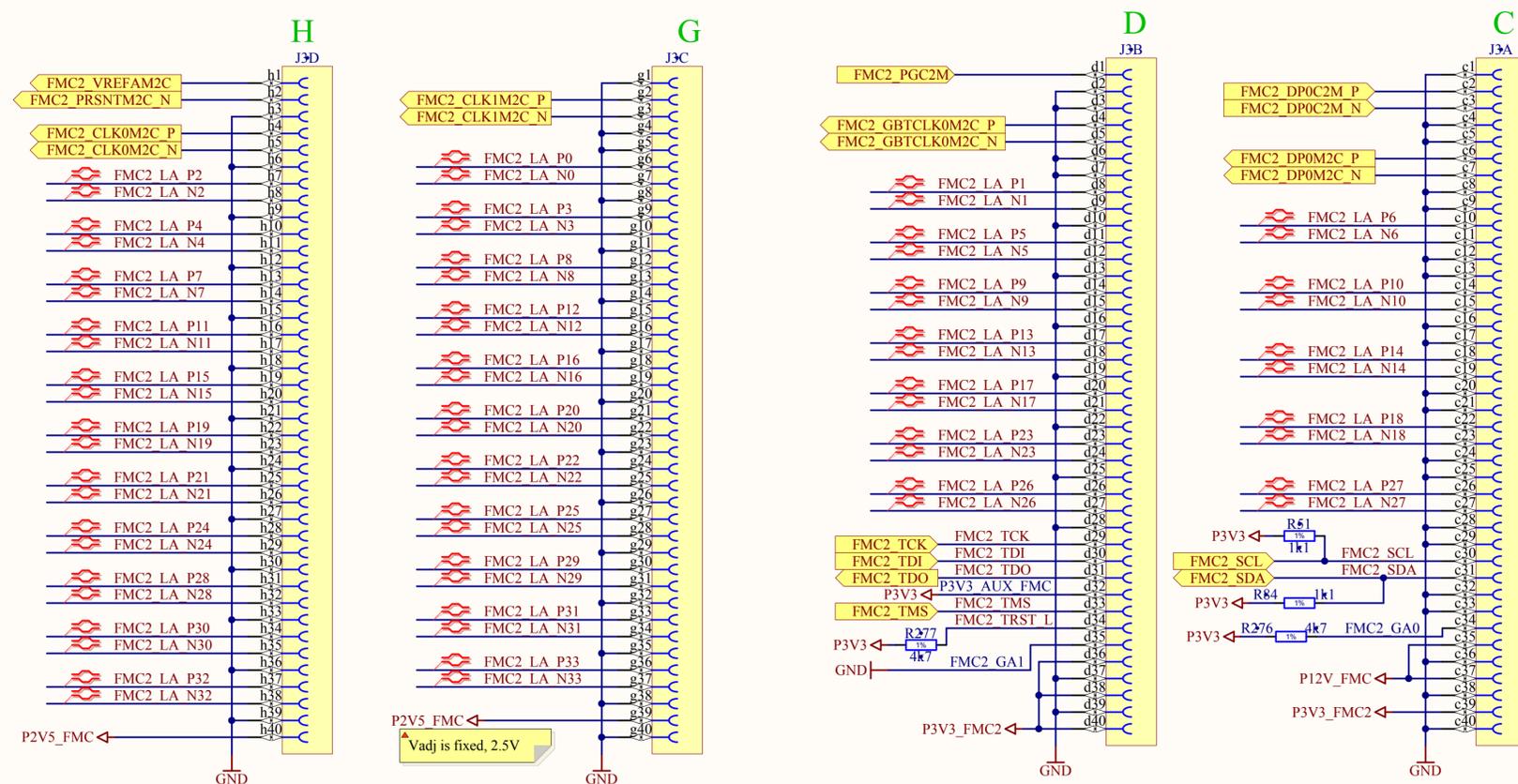
FMC1_LaP and FMC1_LaN are 100ohms diff. pairs



FMC2_LaP and FMC2_LaN are 100ohms diff. pairs

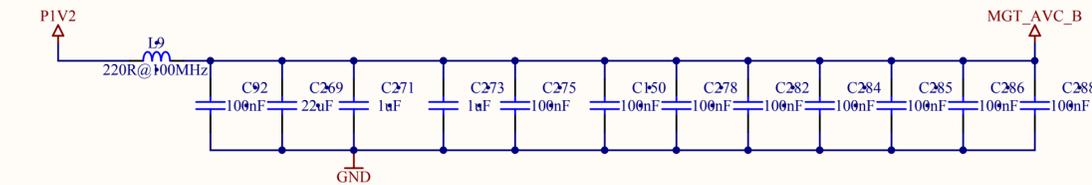
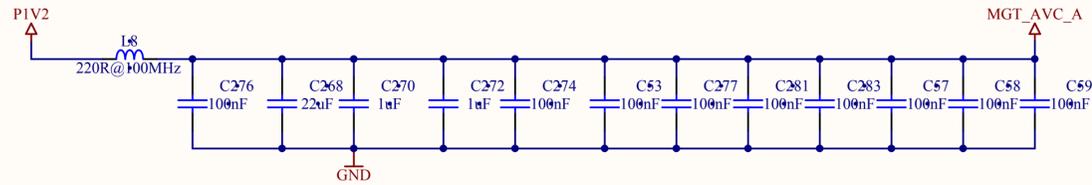


FMC slot 2

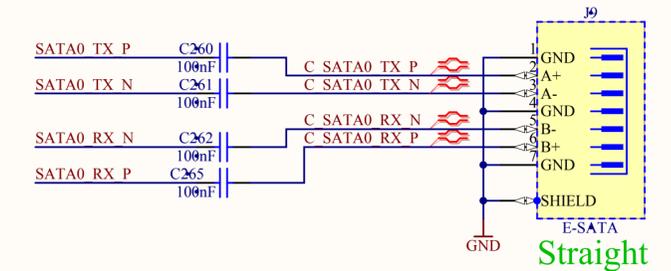
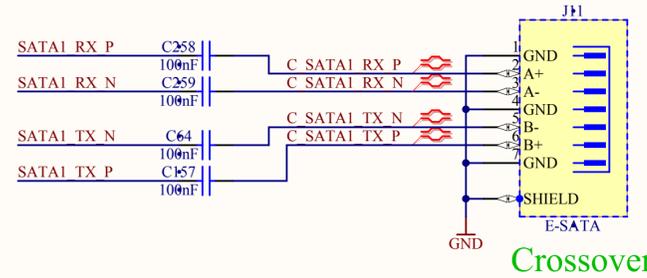


Project/Equipment		Simple VME FMC Carrier	
Document		FMC Connectors	
BE-CO		Designer	G.Kasprowicz
CERN		Drawn by	G.Kasprowicz
		Check by	T.Janicke
		Last Mod.	2012-05-01
		File	FMC_CONNECTORS.SchDoc
		Print Date	2012-05-01 22:22:57
		Sheet	10 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-xxxx	Size A3

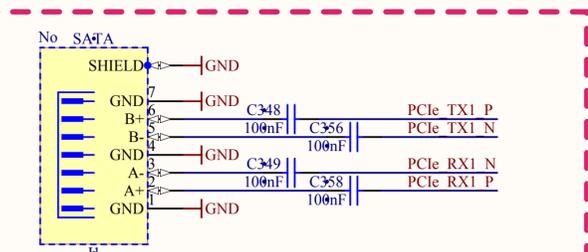
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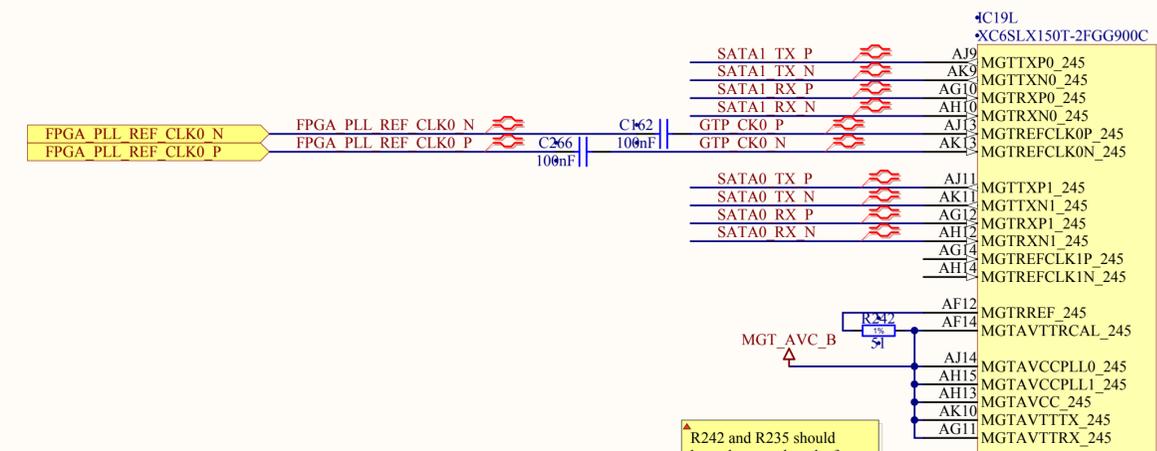
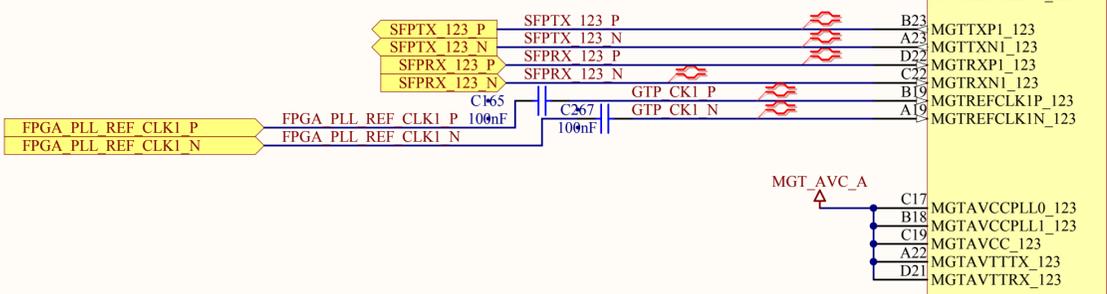
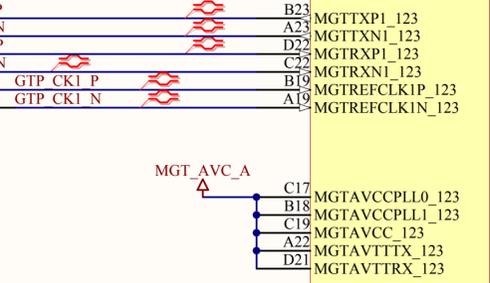
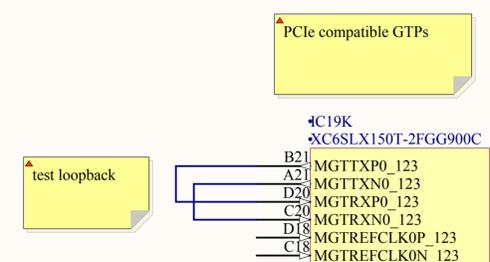
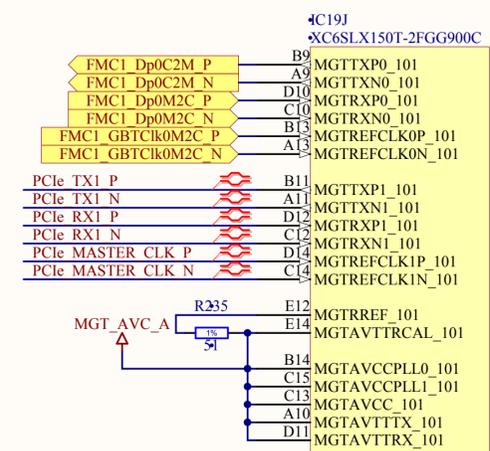
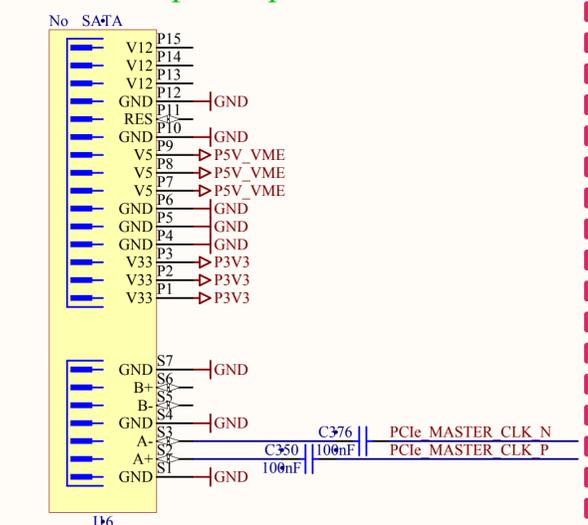
E-SATA connectors



NOT MOUNTED BY DEFAULT



Stand-alone power port and PCIe interface



R242 and R235 should have the same lengths for their terminals

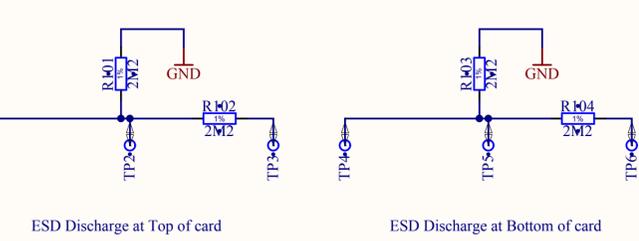
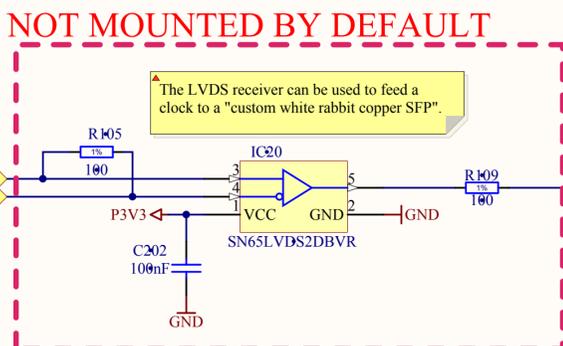
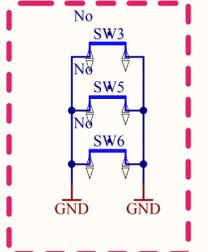
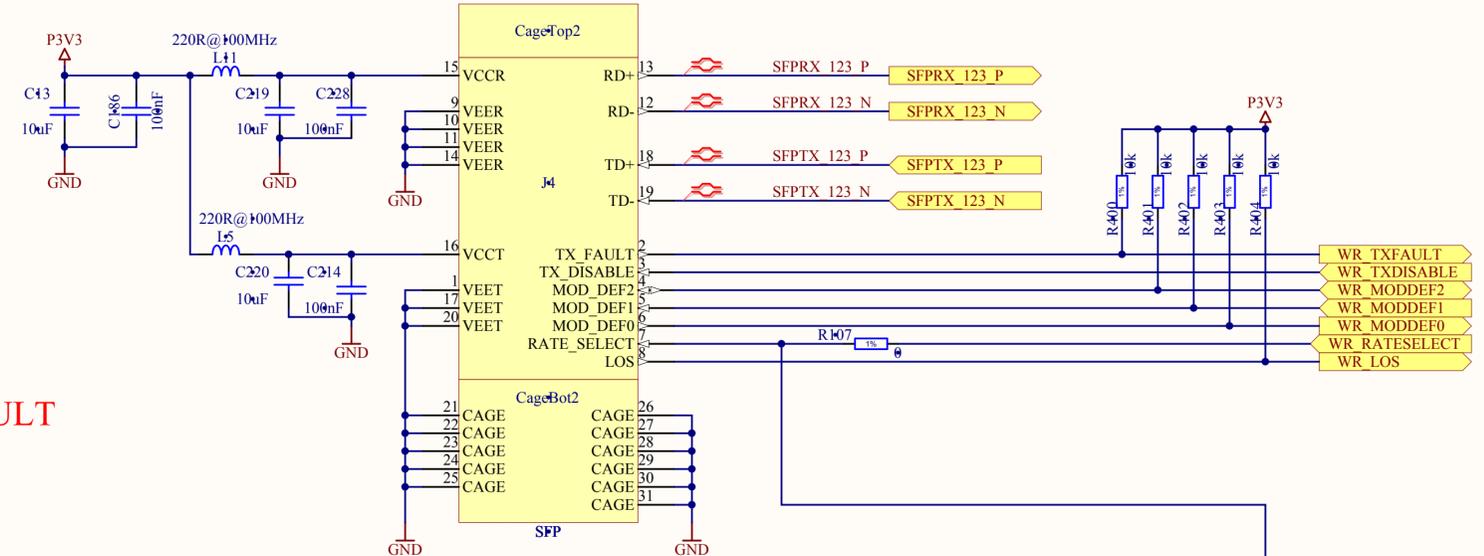
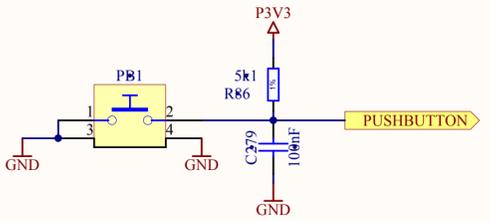
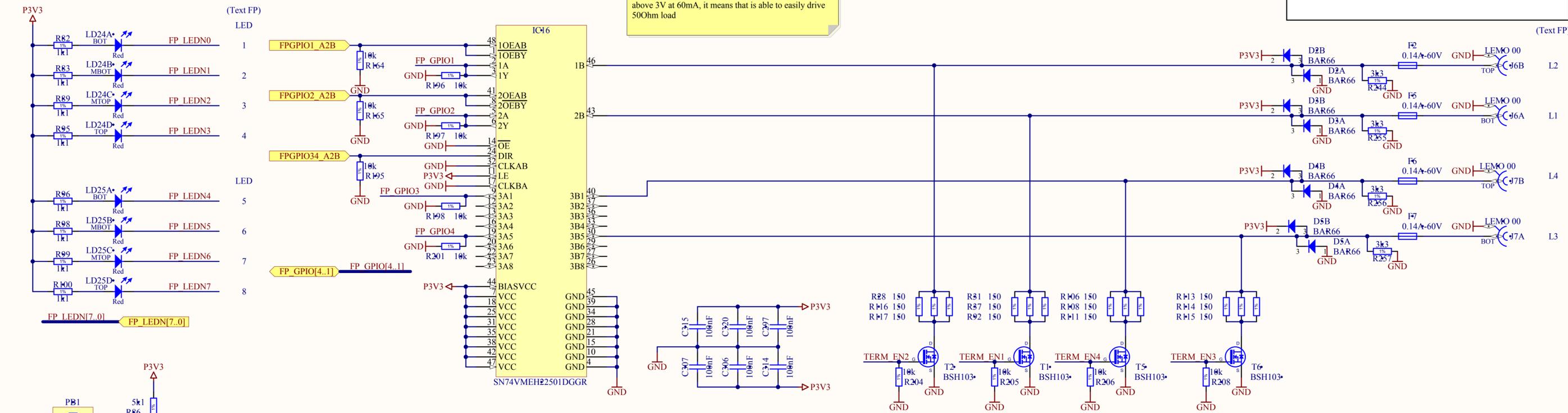
Project/Equipment		Simple VME FMC Carrier	
Document		GTP and SATA	
BE-CO		Designer	G.Kasprowicz
CERN		Drawn by	G.Kasprowicz
		Check by	T.Janicke
		Last Mod.	2012-05-01
		File	FPGA_GTP.SchDoc
		Print Date	2012-05-01 22:22:57
		Sheet	11 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-xxxx	Size Rev A3 -

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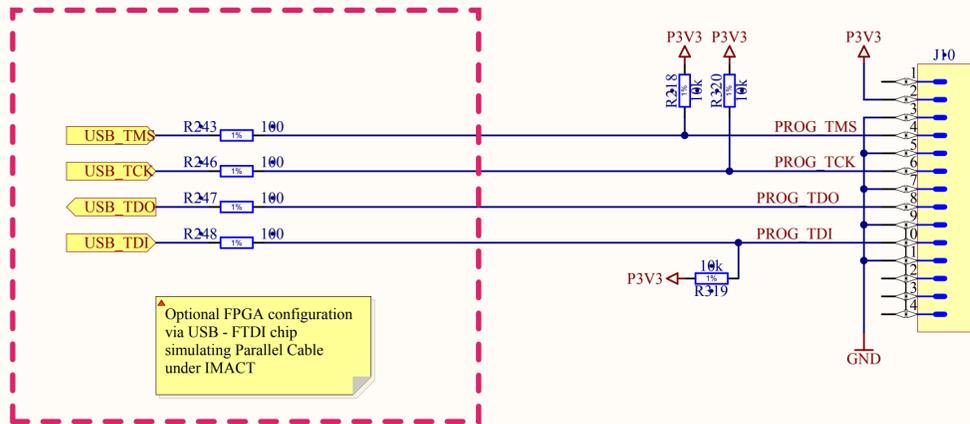
SN74VMEH22501DGGR is able to source 66mA and sink up to 48mA. Supplied from 3.3V delivers still above 3V at 60mA, it means that is able to easily drive 500ohm load



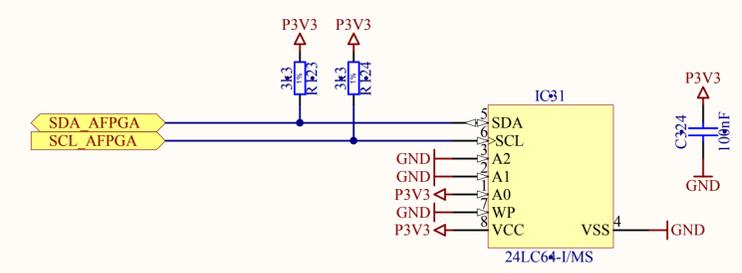
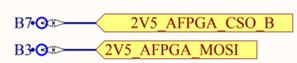
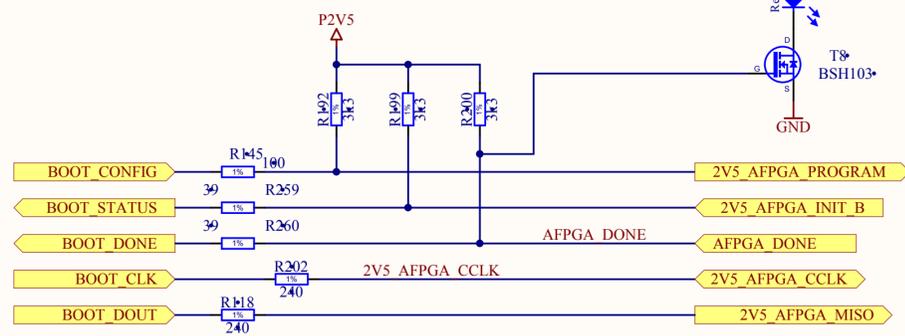
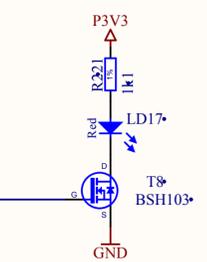
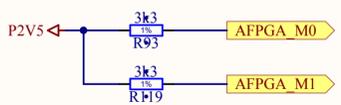
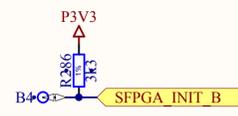
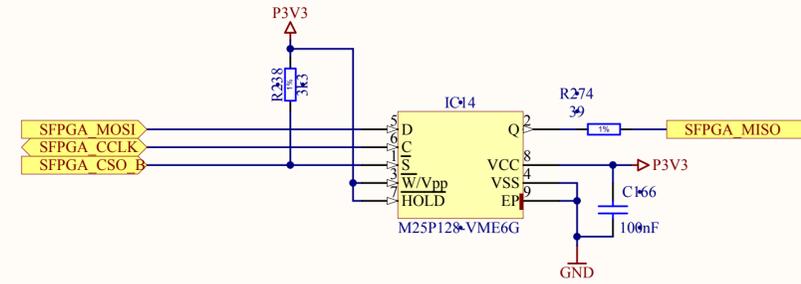
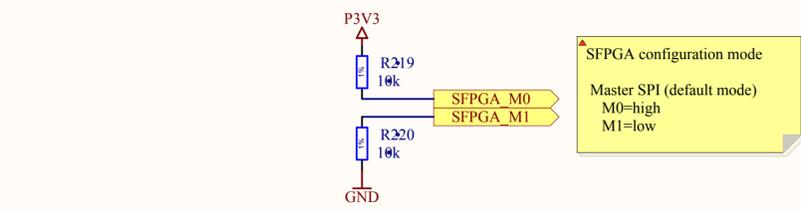
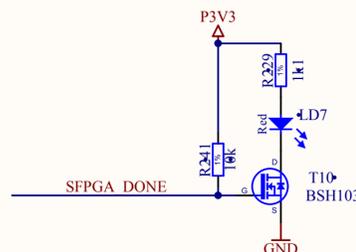
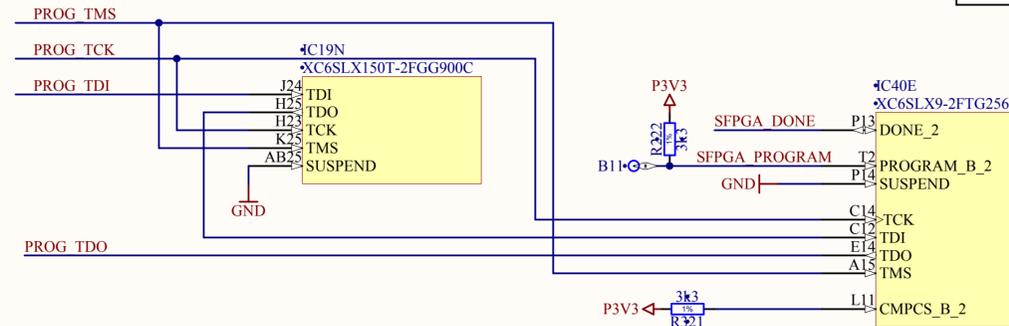
Project/Equipment	Simple VME FMC Carrier	Designer	G.Kasprowicz	20/11/2012
Document	BE-CO	Drawn by	G.Kasprowicz	30/04/2012
		Check by	T.Janicke	2012-05-01
		Last Mod.	-	-
		File	Front_panel.SchDoc	Sheet 12 of 21
		Print Date	2012-05-01 22:22:58	Size A3
			European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland	Rev -
			EDA-xxxx	

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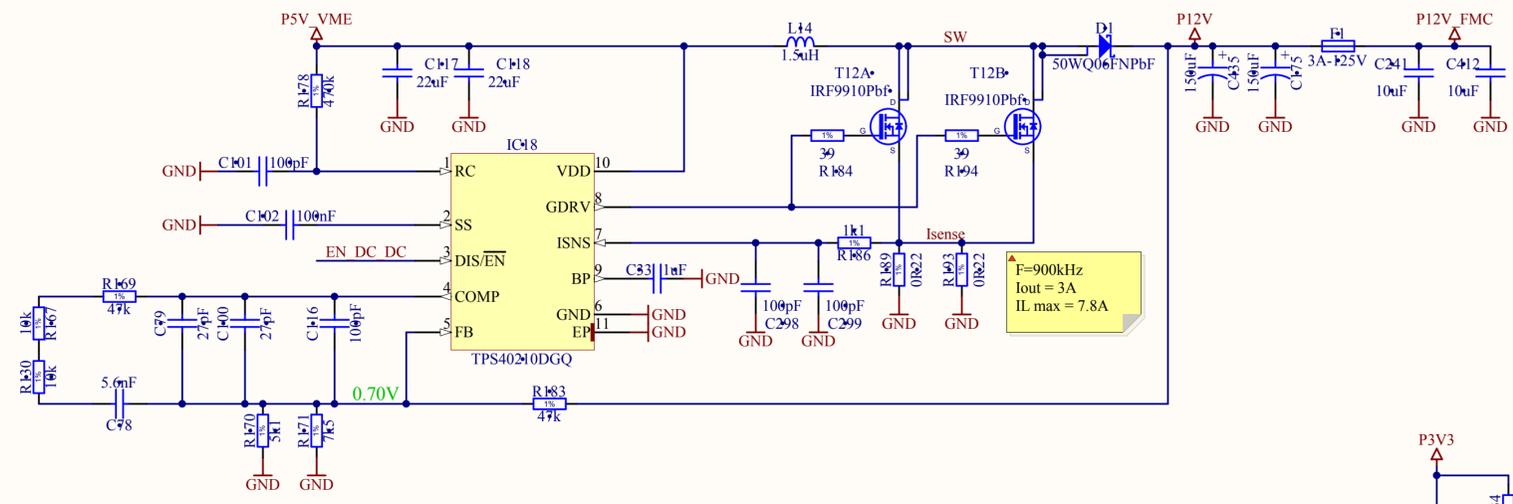


Optional FPGA configuration via USB - FTDI chip simulating Parallel Cable under IMACT



Project/Equipment		Simple VME FMC Carrier	
Document		Designer G.Kasprowicz	
BE-CO		Drawn by G.Kasprowicz	
CERN		Check by T.Janicki	
		Last Mod. 2012-05-01	
		File JTAG Chain + SFPGA Flash.SchDoc	
		Print Date 2012-05-01 22:22:58	
		Sheet 13 of 21	
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-xxxx	
		Size A3	
		Rev -	

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F=900kHz
Iout = 3A
IL max = 7.8A

Power estimation:
P1V2
AFPGA 3A
SFPGA 500mA

P1V5
AFPGA 1A + 2x DDR3 (max 2x 530mW)
(http://download.micron.com/pdf/technotes/ddr3/TN41_01DDR3%20Power.pdf)
estimated power from P1V5 is about 1.5A

P2V5
AFPGA 2A

P2V5_FMC1
FMC slot 2A (HPC = 4A, LPC = 2A)

P2V5_FMC2
FMC slot 2A (HPC = 4A, LPC = 2A)

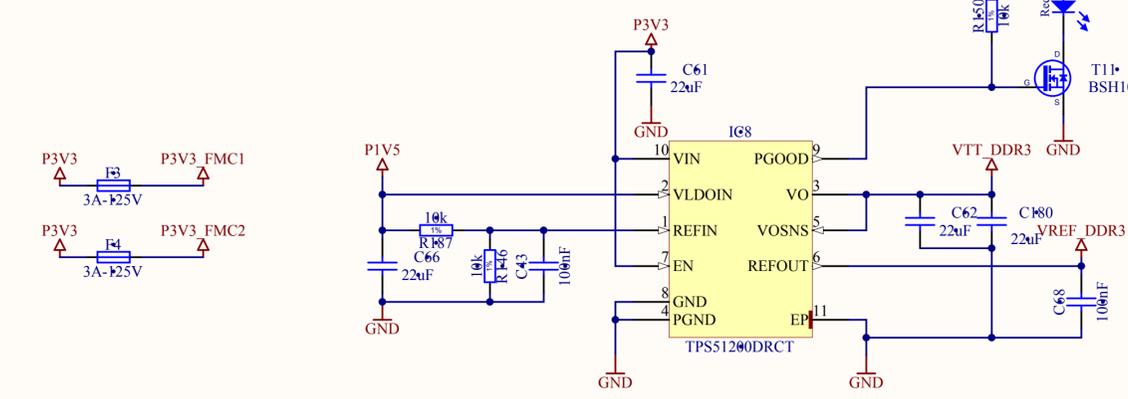
P3V3_FMC1
FMC slot 3A

P3V3_FMC2
FMC slot 3A

P12V_FMC1 1A
P12V_FMC2 1A

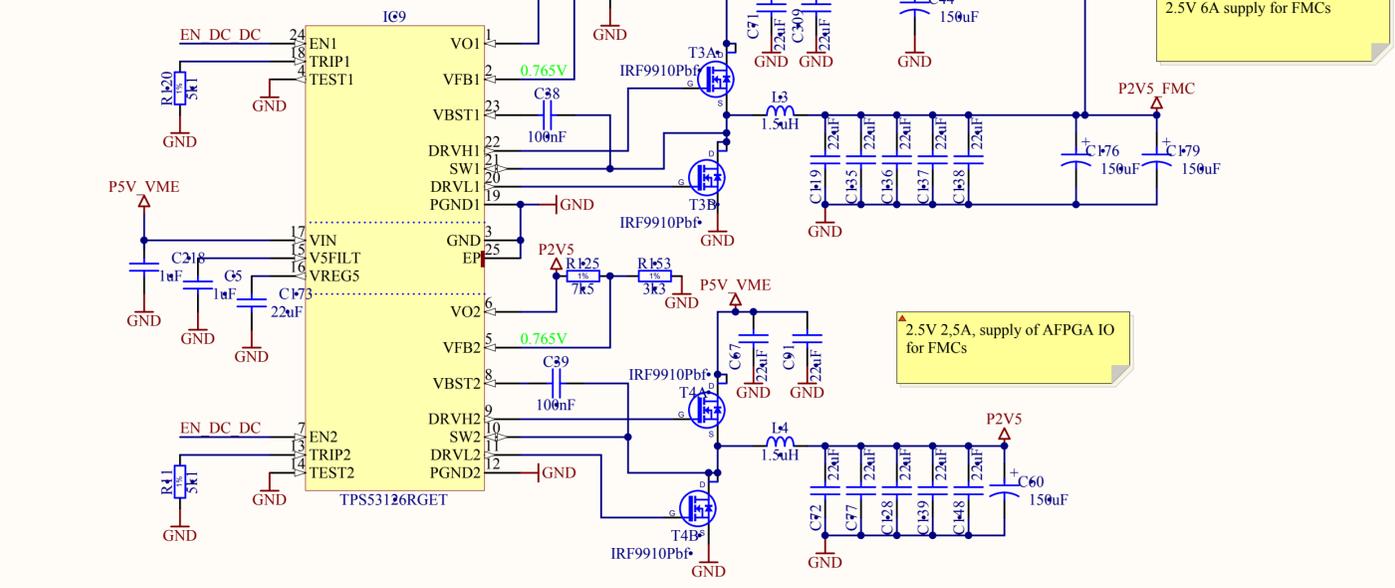
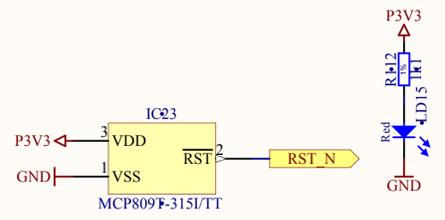
P3V3
AFPGA+SFPGA (Vccaux, IO) 3A
VME interface 1A

LAYOUT NOTES:
- Place the input capacitor close to the top switching FET. The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions Kelvin connections should be brought from the output to the feedback pin (FBx) of the device.
- Make a single point connection from the signal ground to power ground
- Do not allow switching current to flow under the device



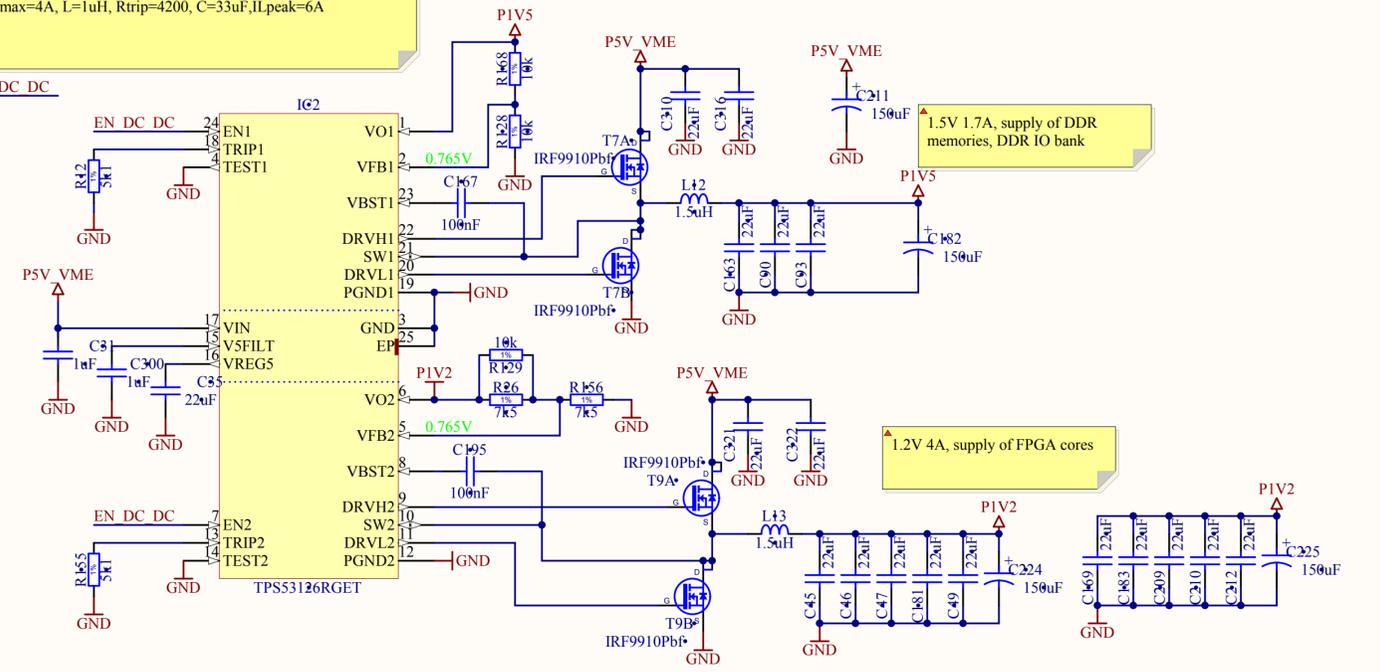
DC/DC calculations, Voripple=30mV
2.5V, I_{max}=5.4A, L=1uH, R_{trip} = 5670, C=50uF, I_{Lpeak}=3.75A
1.2V, I_{max}=4A, L=1uH, R_{trip}=4200, C=80, I_{Lpeak}=6A
2.5V, I_{max}=4A, L=1uH, R_{trip} = 4200, C=80uF, I_{Lpeak}=6A
1.5V, I_{max}=4A, L=1uH, R_{trip}=4200, C=33uF, I_{Lpeak}=6A

- B1 → P5V_VME
- B6 → P1V2
- B2 → P1V8
- B5 → P12V
- B8 → P3V3
- B9 → P2V5
- B10 → GND



2.5V 6A supply for FMCs

2.5V 2.5A, supply of AFPGA IO for FMCs



1.5V 1.7A, supply of DDR memories, DDR IO bank

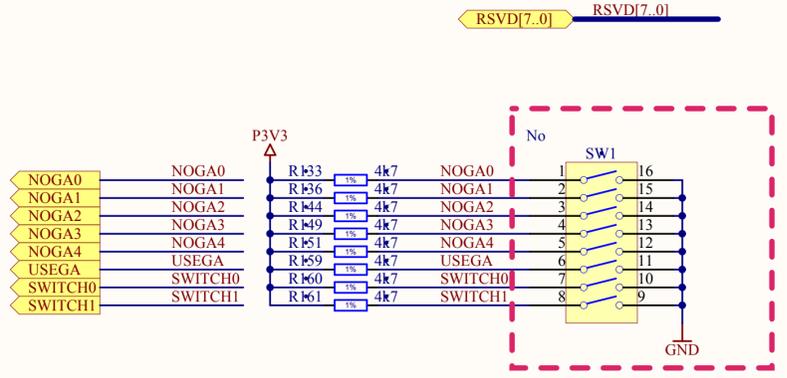
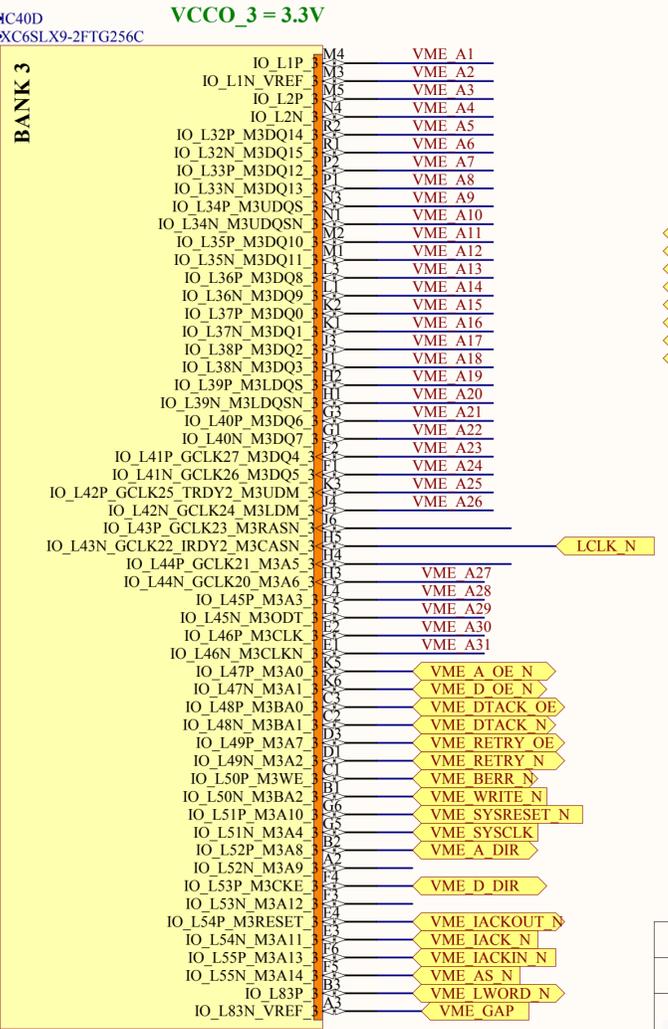
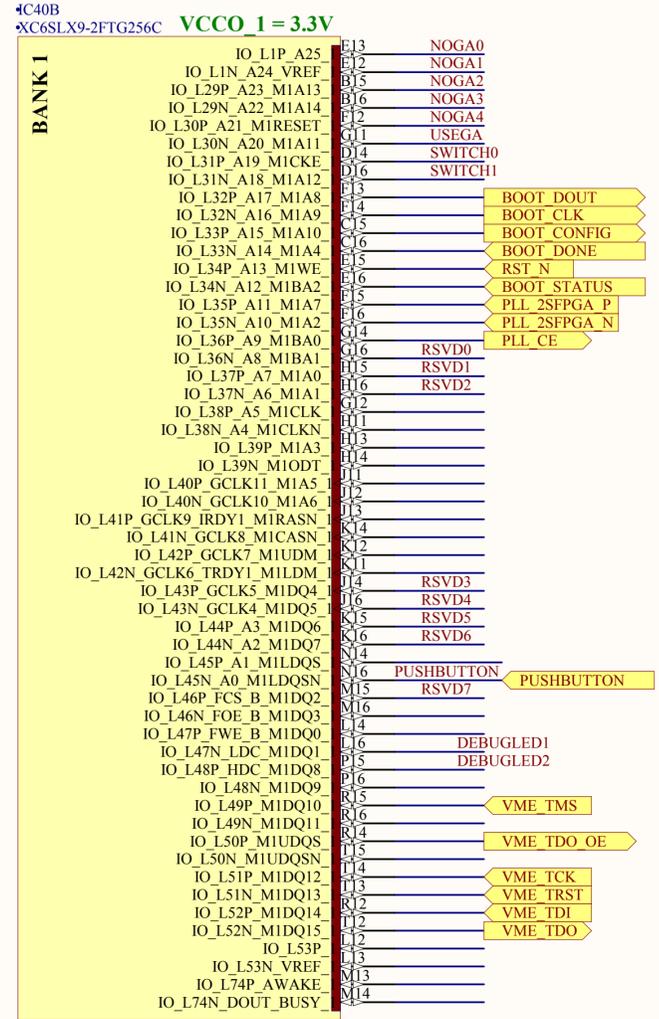
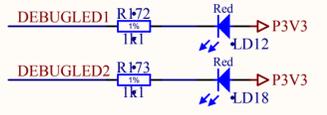
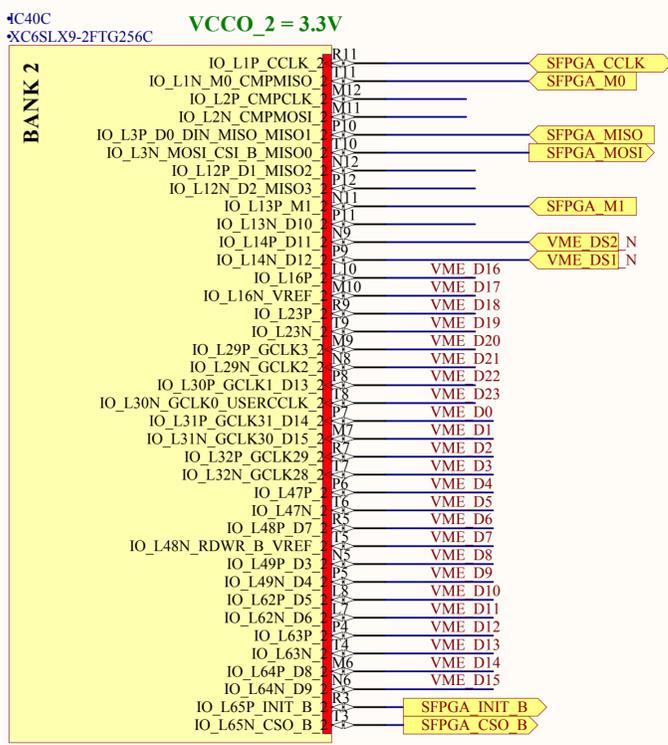
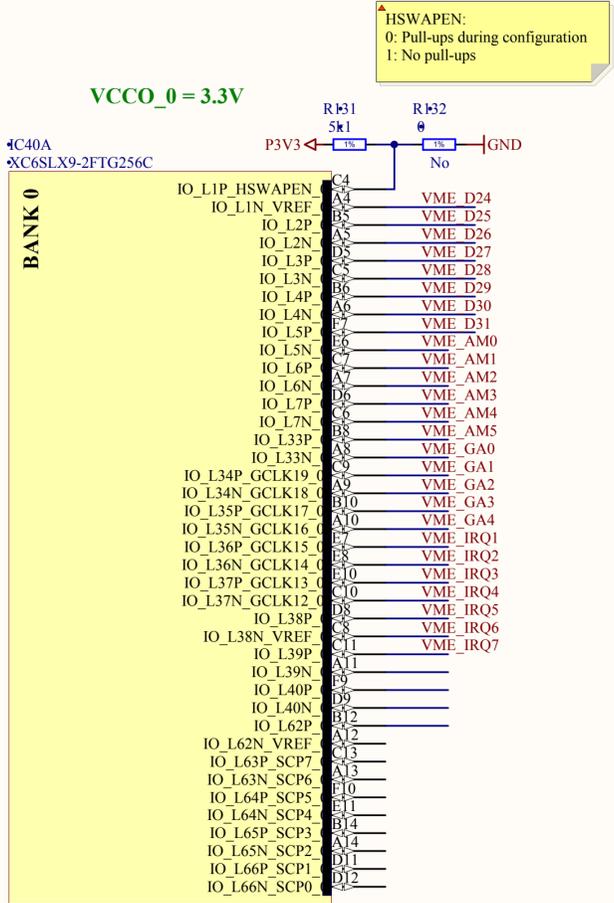
1.2V 4A, supply of FPGA cores

Project/Equipment	Simple VME Carrier Board	Designer	G.Kasprowicz	30/11/2011
Document	Switching power supply	Drawn by	G.Kasprowicz	30/04/2012
BE-CO		Check by	T.Janiczyk	2012-05-01
CERN		Last Mod.		
File	Power_supplies.SchDoc	Print Date	2012-05-01 22:22:58	Sheet 14 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-xxxx	Size	A3

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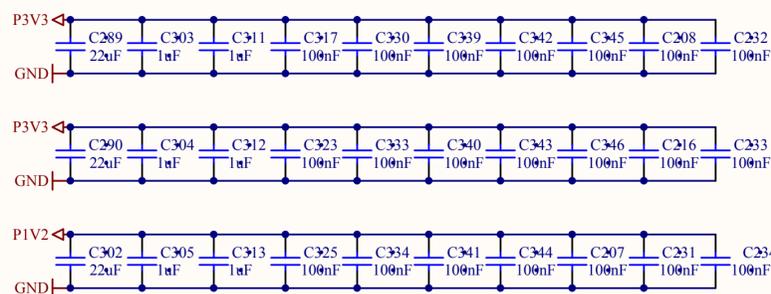
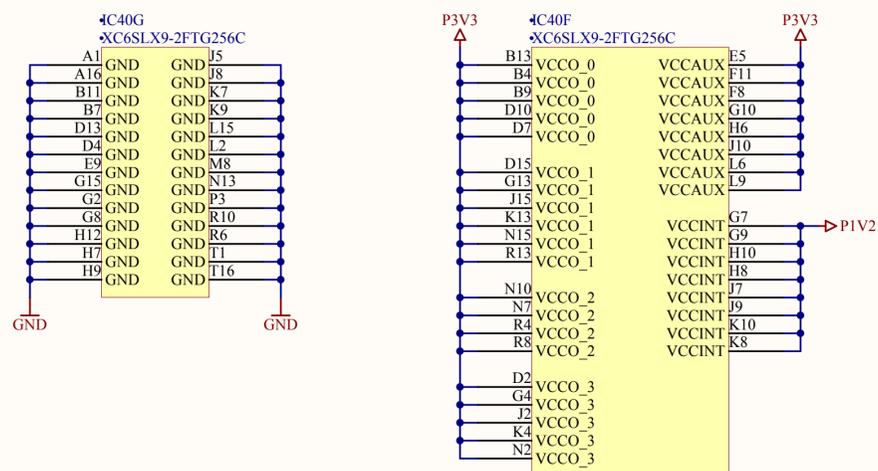
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Project/Equipment		Simple VME FMC Carrier	
Document		System FPGA	
BE-CO		CERN	
Designer	G.Kasprowicz	Drawn by	G.Kasprowicz
Check by	T.Janicke	Last Mod.	2012-05-01
File	SFPGA.SchDoc	Print Date	2012-05-01 22:22:58
Sheet	15 of 21	Size	A3
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-xxxx	

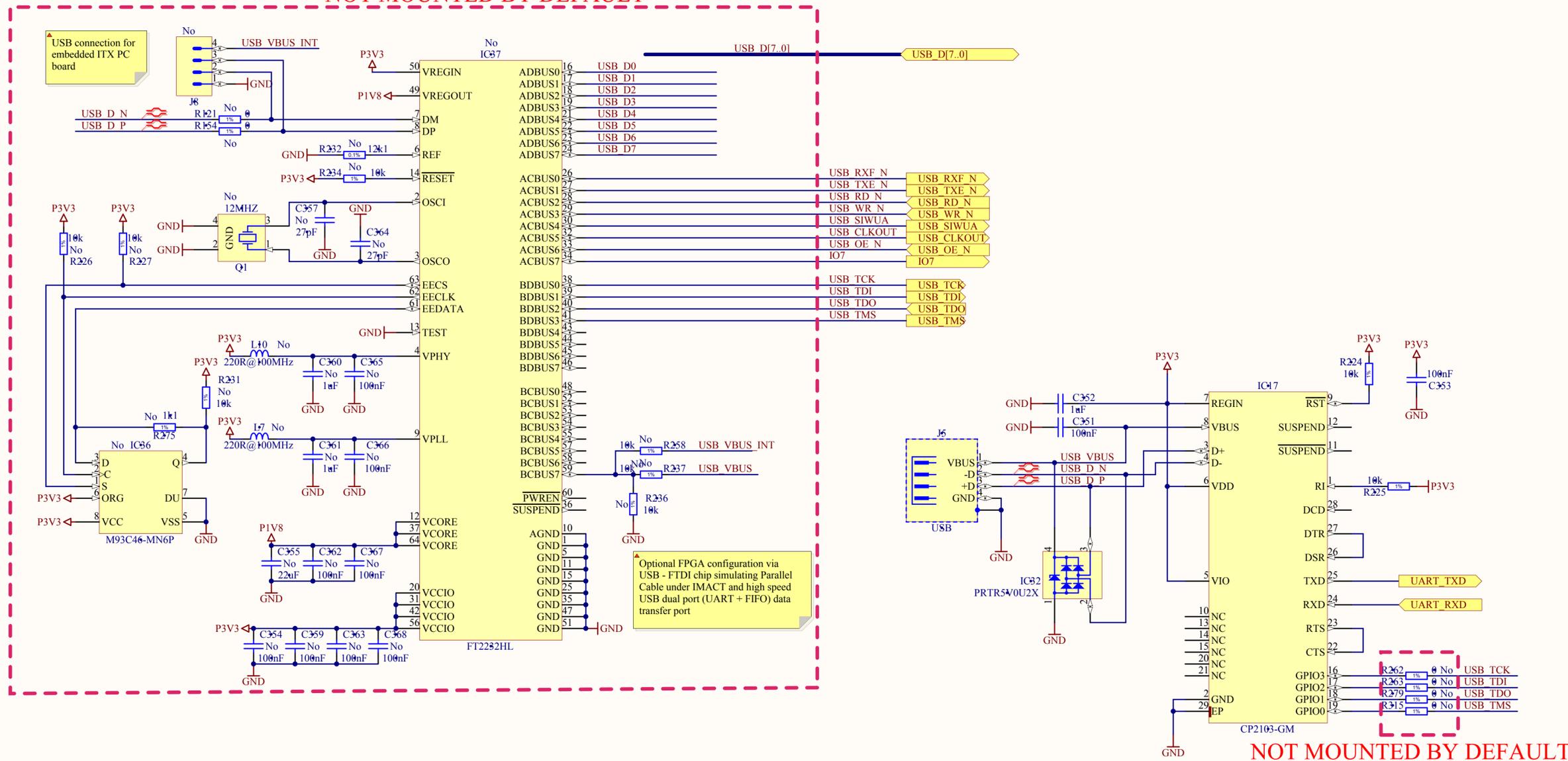
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Project/Equipment		Simple VME FMC Carrier	
Document		System FPGA power	
BE-CO	CERN	Designer	G.Kasprowicz
		Drawn by	G.Kasprowicz
		Check by	T.Janicki
		Last Mod.	2012-05-01
		File	SFPGA_power.SchDoc
		Print Date	2012-05-01 22:22:58
		Sheet	16 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-xxxx	Size A3 Rev -

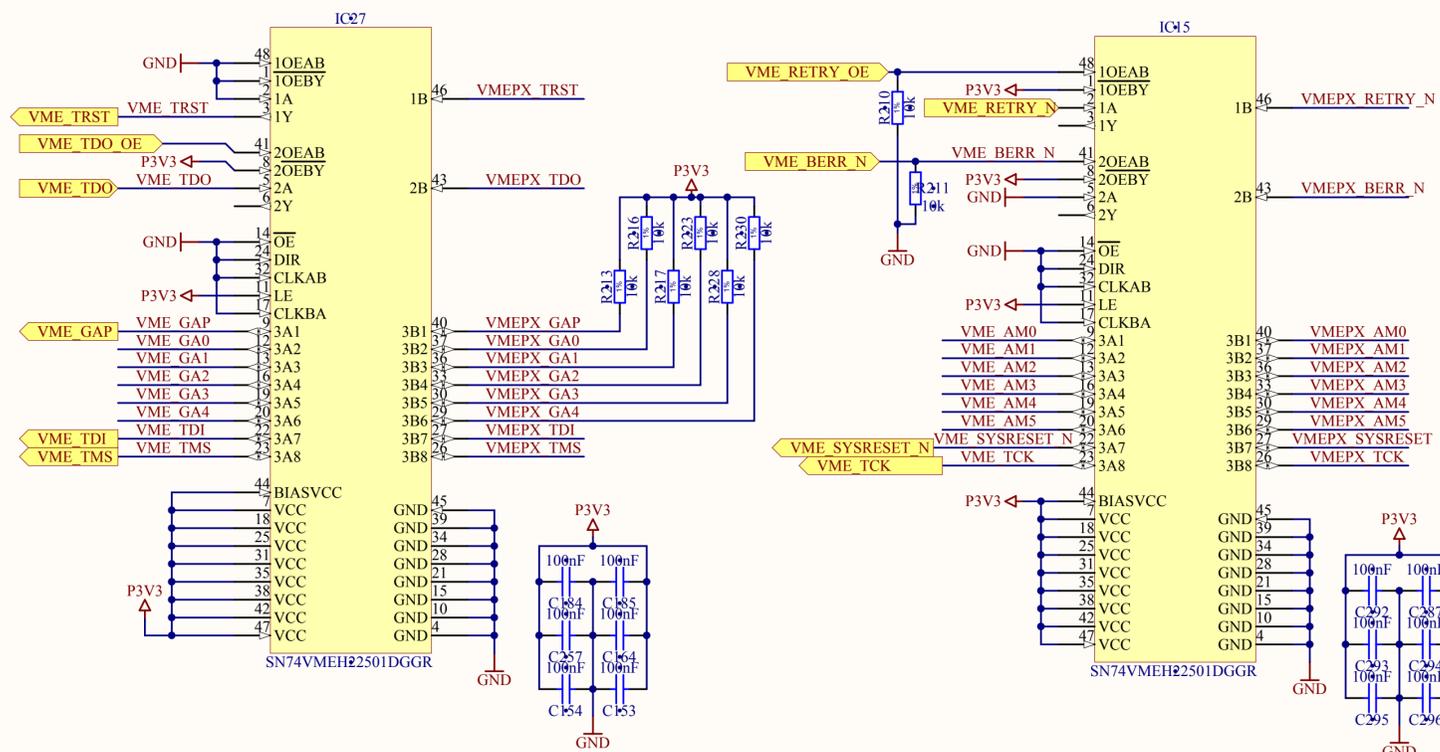
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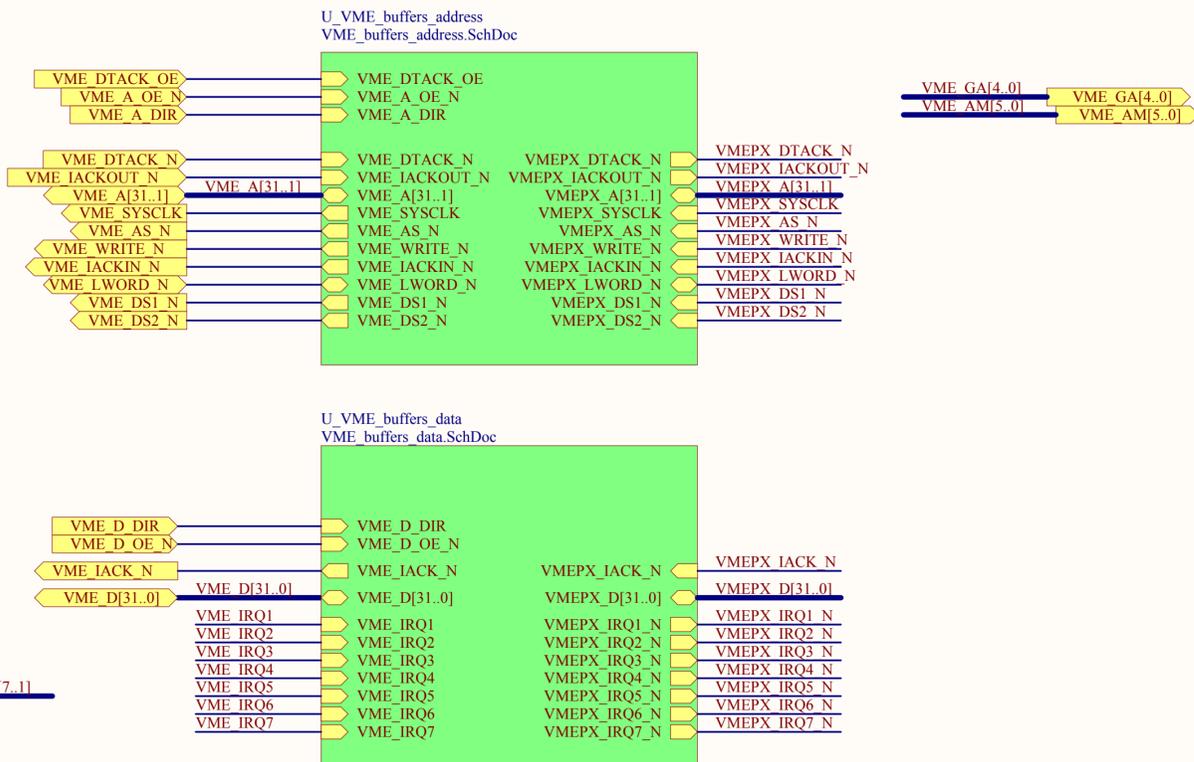
Project/Equipment		Simple VME FMC Carrier	
Document		USB interface	
BE-CO		CERN	
Designer	G. Kasprowicz	20/11/2012	
Drawn by	G. Kasprowicz	30/04/2012	
Check by	T. Janicki	2012-05-01	
Last Mod.			
File	USB_interface.SchDoc		
Print Date	2012-05-01 22:22:59	Sheet	17 of 21
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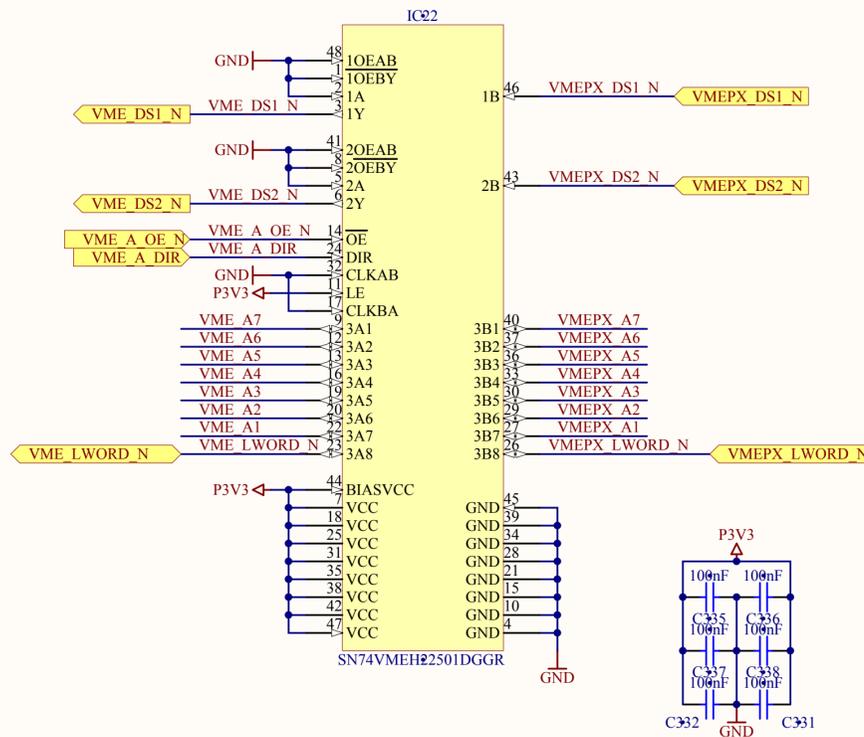
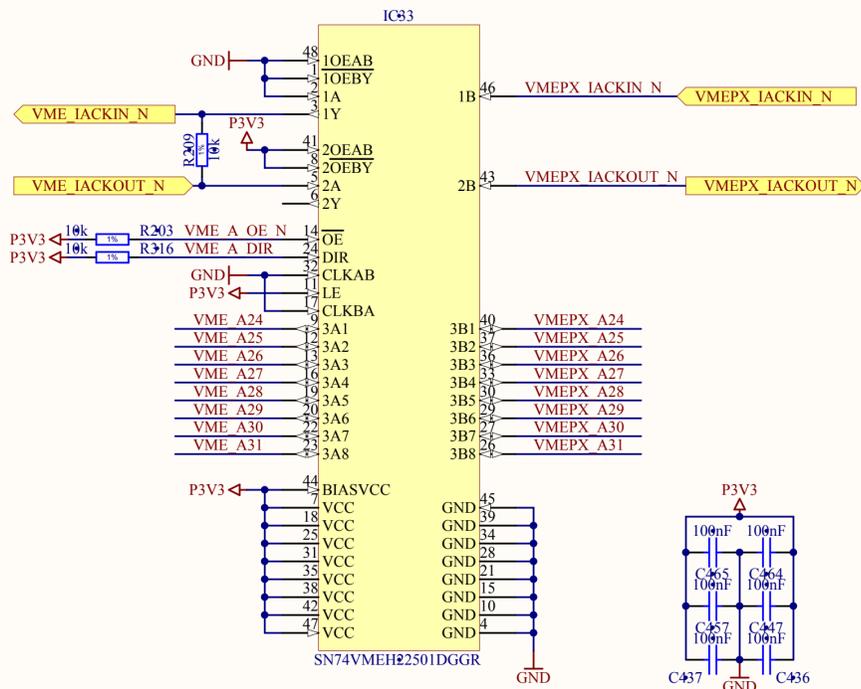
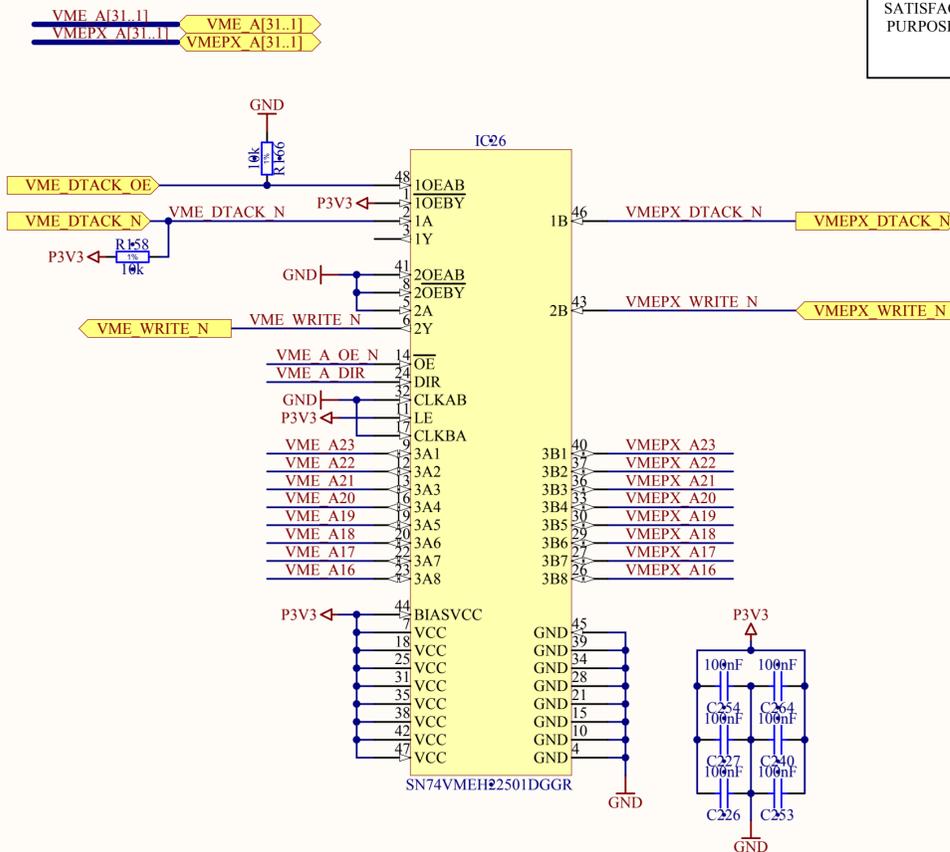
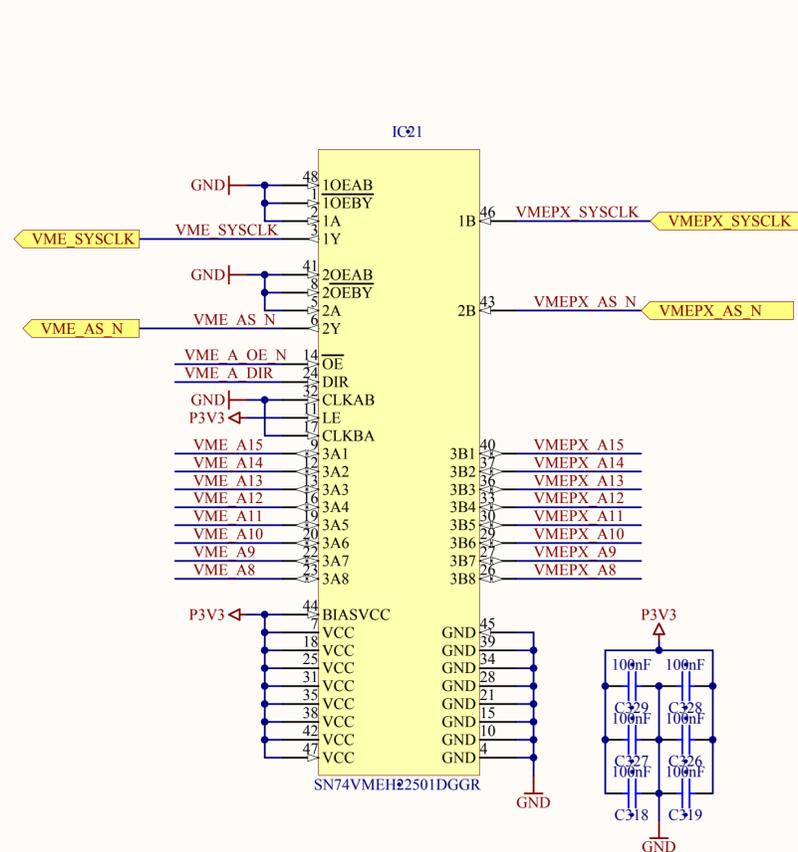
VME_signals

VMEPX_AS_N	VMEPX_AS_N
VMEPX_IACK_N	VMEPX_IACK_N
VMEPX_IACKIN_N	VMEPX_IACKIN_N
VMEPX_IACKOUT_N	VMEPX_IACKOUT_N
VMEPX_IACKOUT_N	VMEPX_IACKOUT_N
VMEPX_SYSCLK	VMEPX_SYSCLK
VMEPX_DS1_N	VMEPX_DS1_N
VMEPX_DS2_N	VMEPX_DS2_N
VMEPX_WRITE_N	VMEPX_WRITE_N
VMEPX_DTACK_N	VMEPX_DTACK_N
VMEPX_D[31..0]	VMEPX_D[31..0]
VMEPX_SYSFAIL	VMEPX_SYSFAIL
VMEPX_BERR_N	VMEPX_BERR_N
VMEPX_SYSRESET	VMEPX_SYSRESET
VMEPX_LWORD_N	VMEPX_LWORD_N
VMEPX_RETRY_N	VMEPX_RETRY_N
VMEPX_GAP	VMEPX_GAP
VMEPX_A[31..1]	VMEPX_A[31..1]
VMEPX_GA[4..0]	VMEPX_GA[4..0]
VMEPX_AM[5..0]	VMEPX_AM[5..0]
VMEPX_BR[3..0]	VMEPX_BR[3..0]
VMEPX_IRQ7_N	VMEPX_IRQ7_N
VMEPX_IRQ6_N	VMEPX_IRQ6_N
VMEPX_IRQ5_N	VMEPX_IRQ5_N
VMEPX_IRQ4_N	VMEPX_IRQ4_N
VMEPX_IRQ3_N	VMEPX_IRQ3_N
VMEPX_IRQ2_N	VMEPX_IRQ2_N
VMEPX_IRQ1_N	VMEPX_IRQ1_N
VMEPX_BBSY	VMEPX_BBSY
VMEPX_BCLR	VMEPX_BCLR
VMEPX_ACFAIL	VMEPX_ACFAIL
VMEPX_SERA	VMEPX_SERA
VMEPX_SERB	VMEPX_SERB
VMEPX_TRST	VMEPX_TRST
VMEPX_TCK	VMEPX_TCK
VMEPX_TDO	VMEPX_TDO
VMEPX_TDI	VMEPX_TDI
VMEPX_TMS	VMEPX_TMS



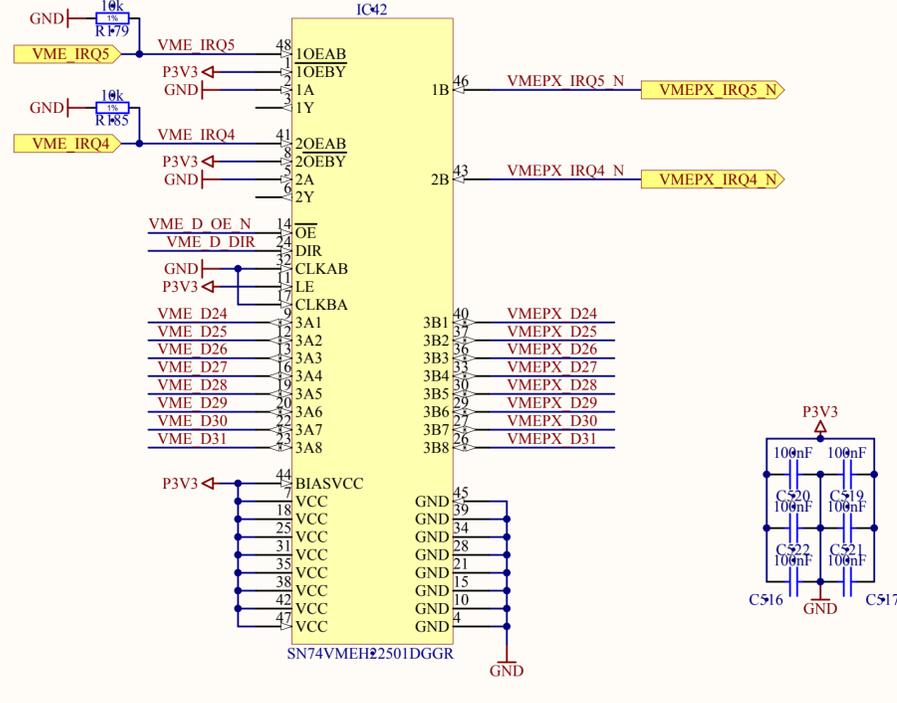
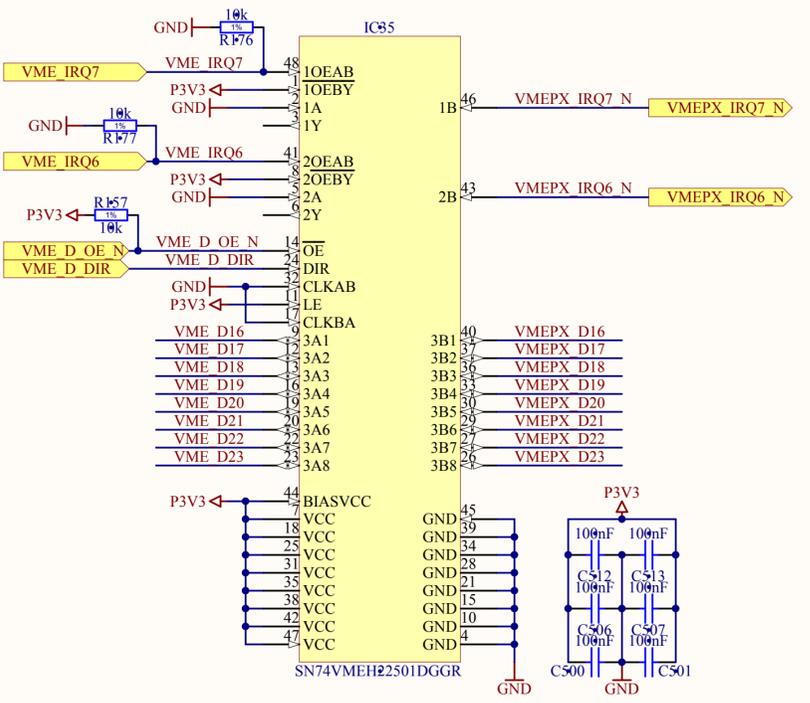
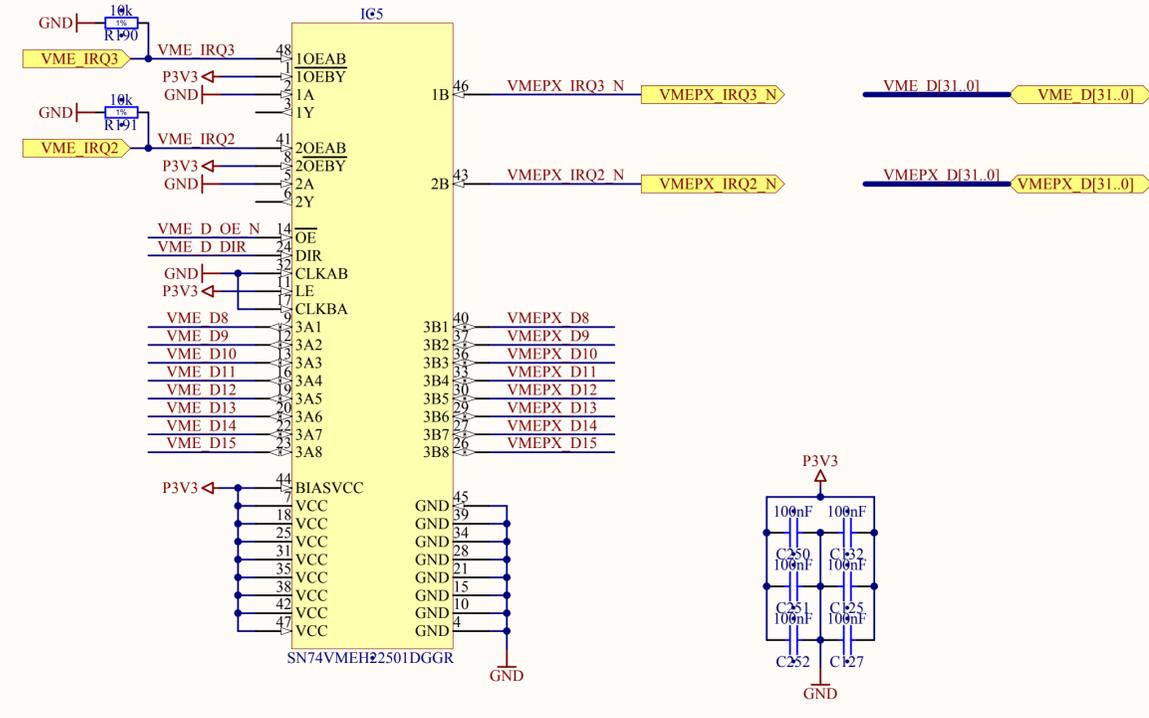
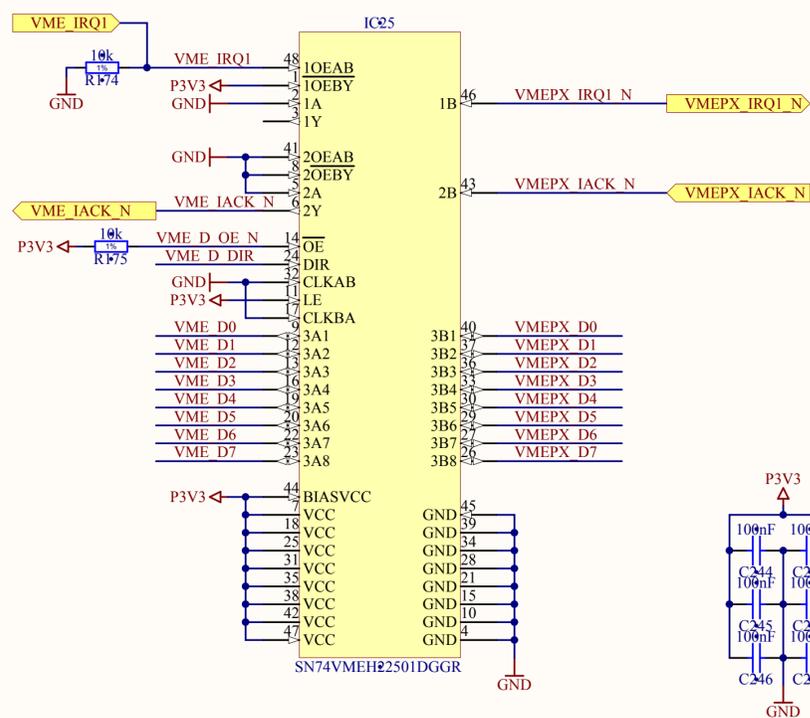
Project/Equipment	Simple VME FMC Carrier	Designer	G.Kasprowicz
Document	VME buffers	Drawn by	G.Kasprowicz
BE-CO	CERN	Check by	T.Janicki
		Last Mod.	-
File	VME_buffers.SchDoc	Print Date	2012-05-01 22:22:59
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		Sheet	19 of 21
EDA-xxxx		Size	A3
		Rev	-

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Project/Equipment		Simple VME FMC Carrier	
Document		VME buffers - address part -	
BE-CO			
CERN		Designer	G.Kasprowicz
		Drawn by	G.Kasprowicz
		Check by	T.Janicke
		Last Mod.	2012-05-01
		File	VME_buffers_address.SchDoc
		Print Date	2012-05-01 22:22:59
		Sheet	20 of 21
		Size	A3
		Rev	-
		European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland	
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Project/Equipment		Simple VME FMC Carrier	
Document		Designer G.Kasprowicz	
BE-CO		Drawn by G.Kasprowicz	
CERN		Check by T.Janicke	
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		File VME_buffers_data.SchDoc	
		Print Date 2012-05-01 22:22:59	
		Sheet 21 of 21	
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-xxxx	
		Size A3	
		Rev -	