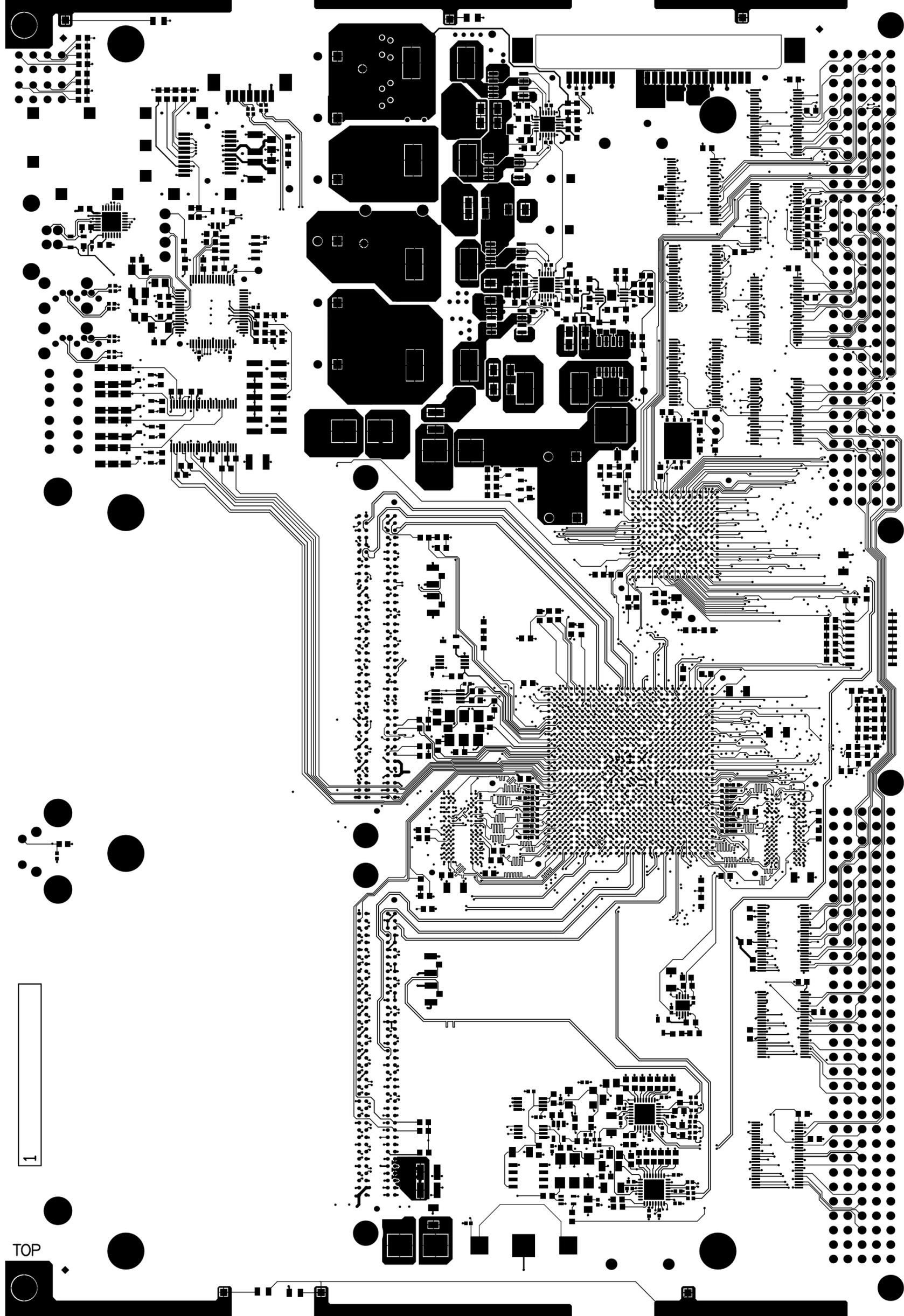


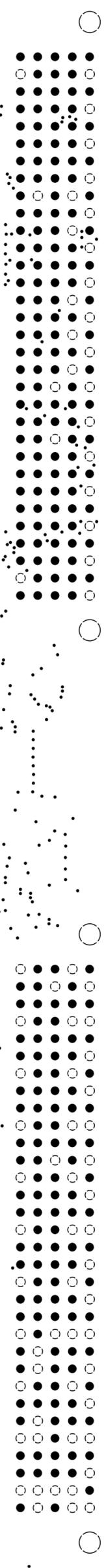
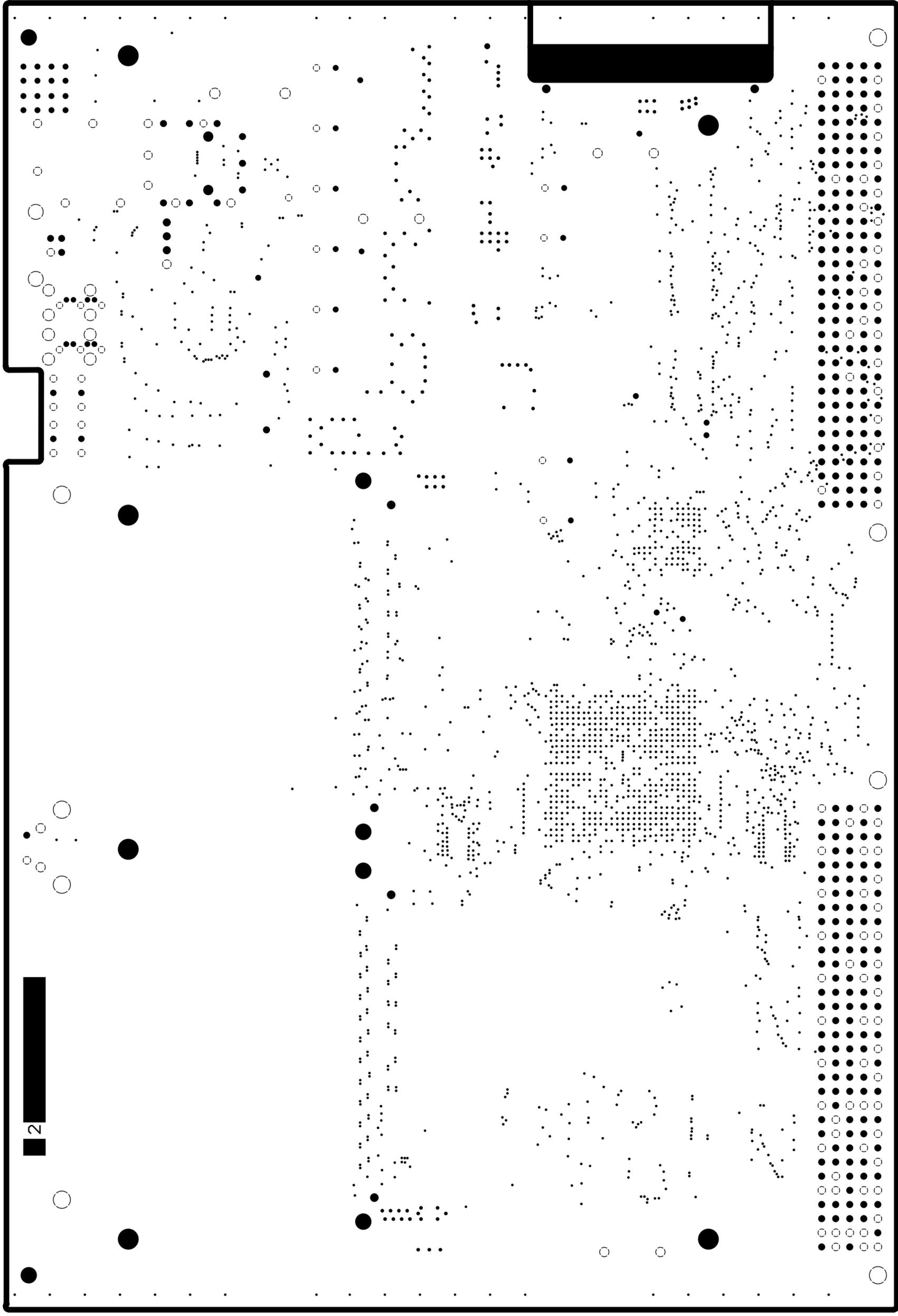
TOP

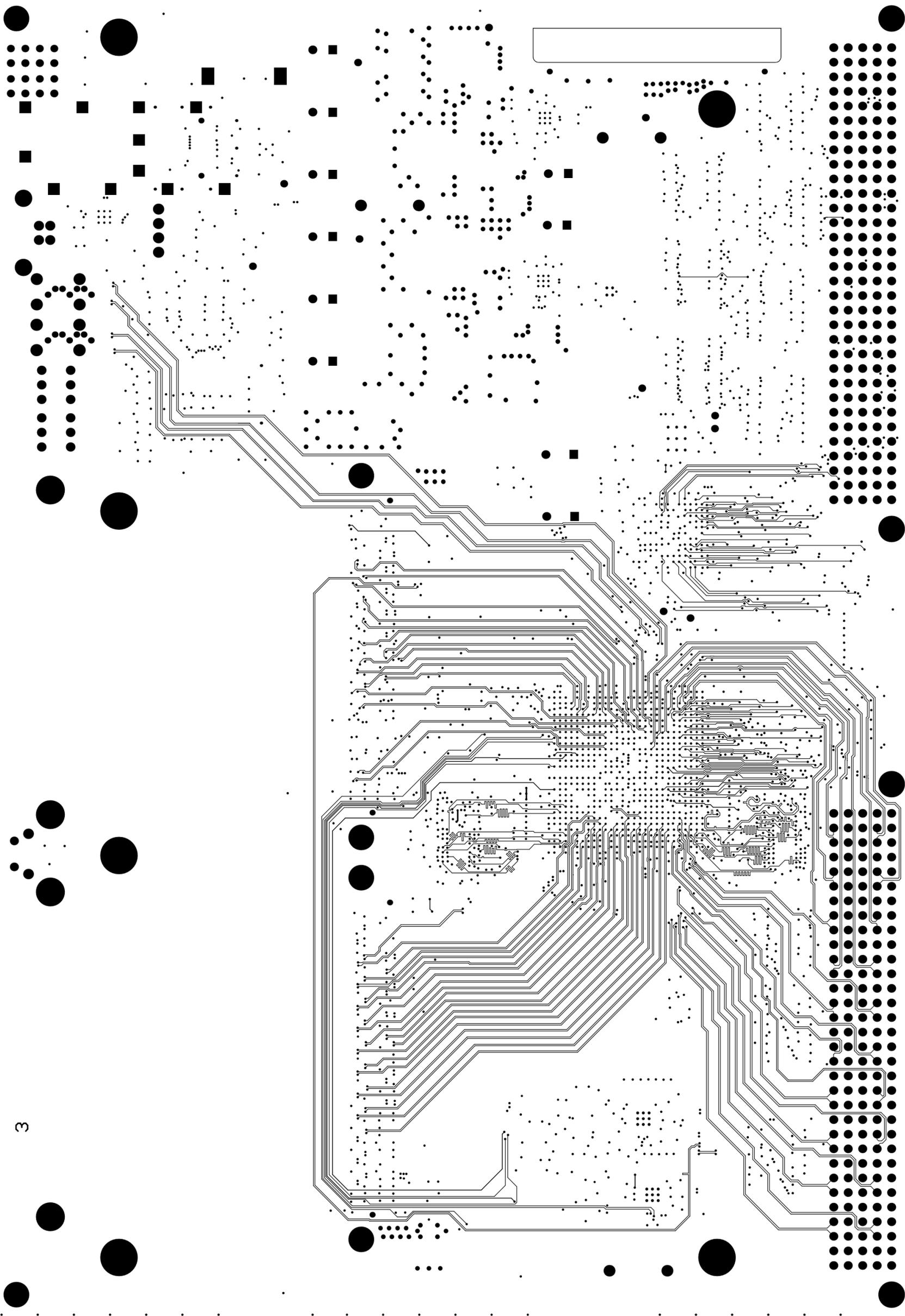
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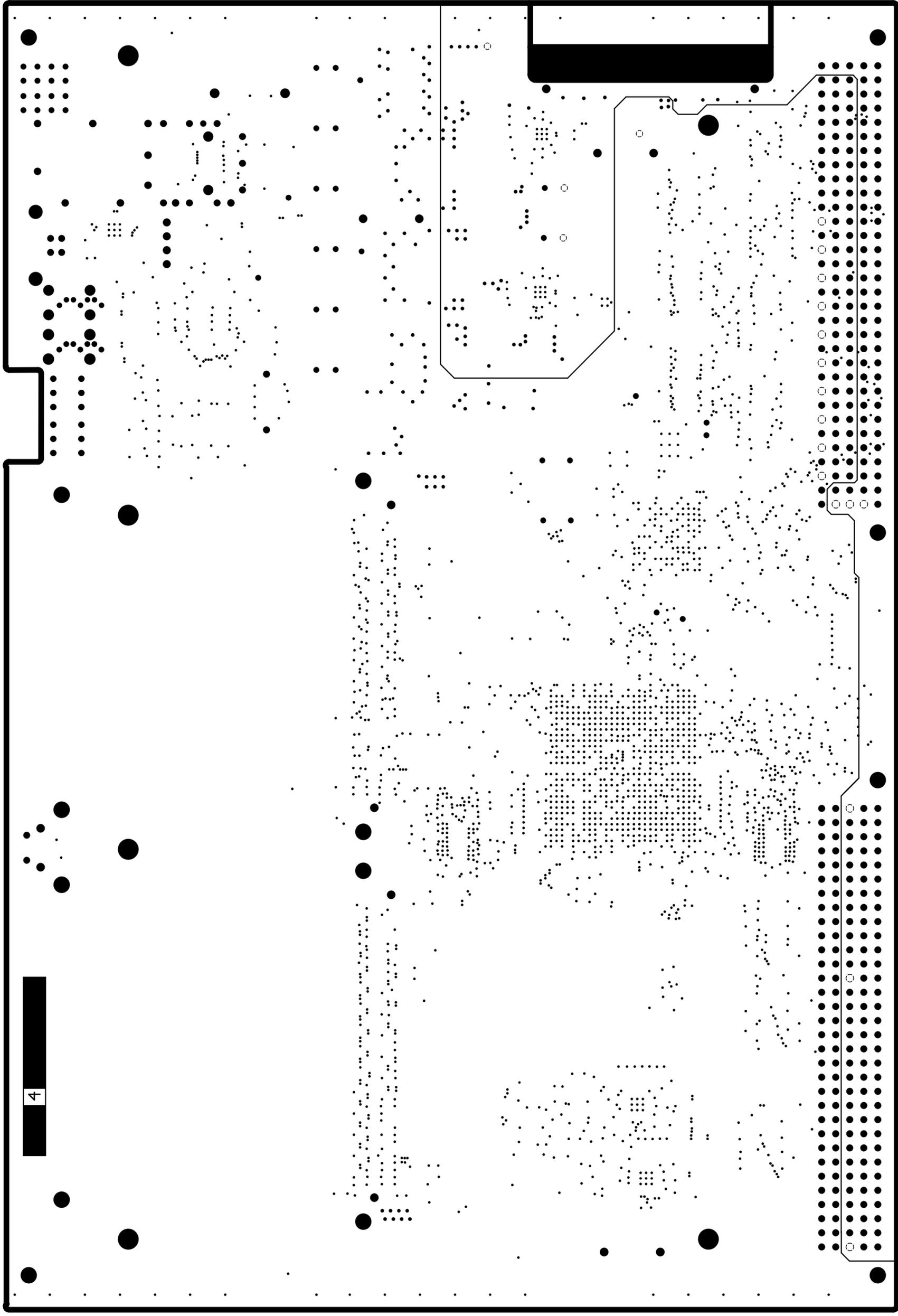


**Layer Stack Up Detail for: SVEC.pcbdoc**

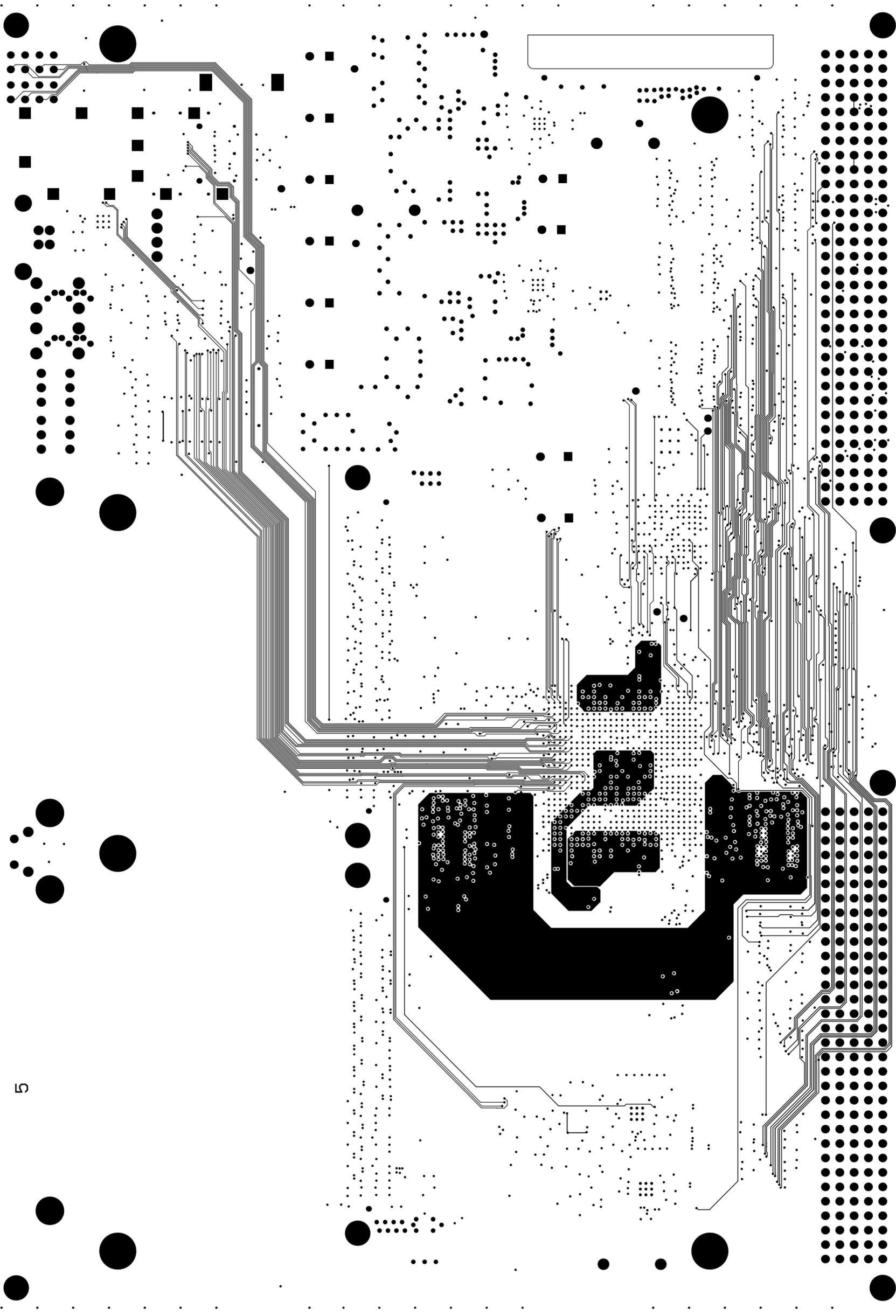
Layer Name	Gerber Document	Copper Thickness	Dielectric Height	Dielectric Material	Dielectric Constant	Dielectric Type
Top Solder Mask	(.GTS)		0.394mil	Solder Resist	3.50	
Top Layer	(.GTL)	0.709mil	3.937mil	FR-4	4.60	Core
L2 GND	(.GP1)	0.709mil	5.905mil	FR-4	4.80	PrePreg
L3	(.G1)	0.709mil	5.905mil	FR-4	4.80	Core
L4 PWR3.3	(.GP2)	0.709mil	3.937mil	FR-4	4.80	PrePreg
L5	(.G2)	0.709mil	11.811mil	FR-4	4.80	Core
L6	(.G3)	0.709mil	3.937mil	FR-4	4.80	PrePreg
L7 GND	(.GP3)	0.709mil	5.905mil	FR-4	4.80	Core
L8	(.G4)	0.709mil	5.905mil	FR-4	4.80	PrePreg
L9 PWR	(.GP4)	0.709mil	3.937mil	FR-4	4.80	Core
Bottom Layer	(.GBL)	0.709mil	0.394mil	Solder Resist	3.50	

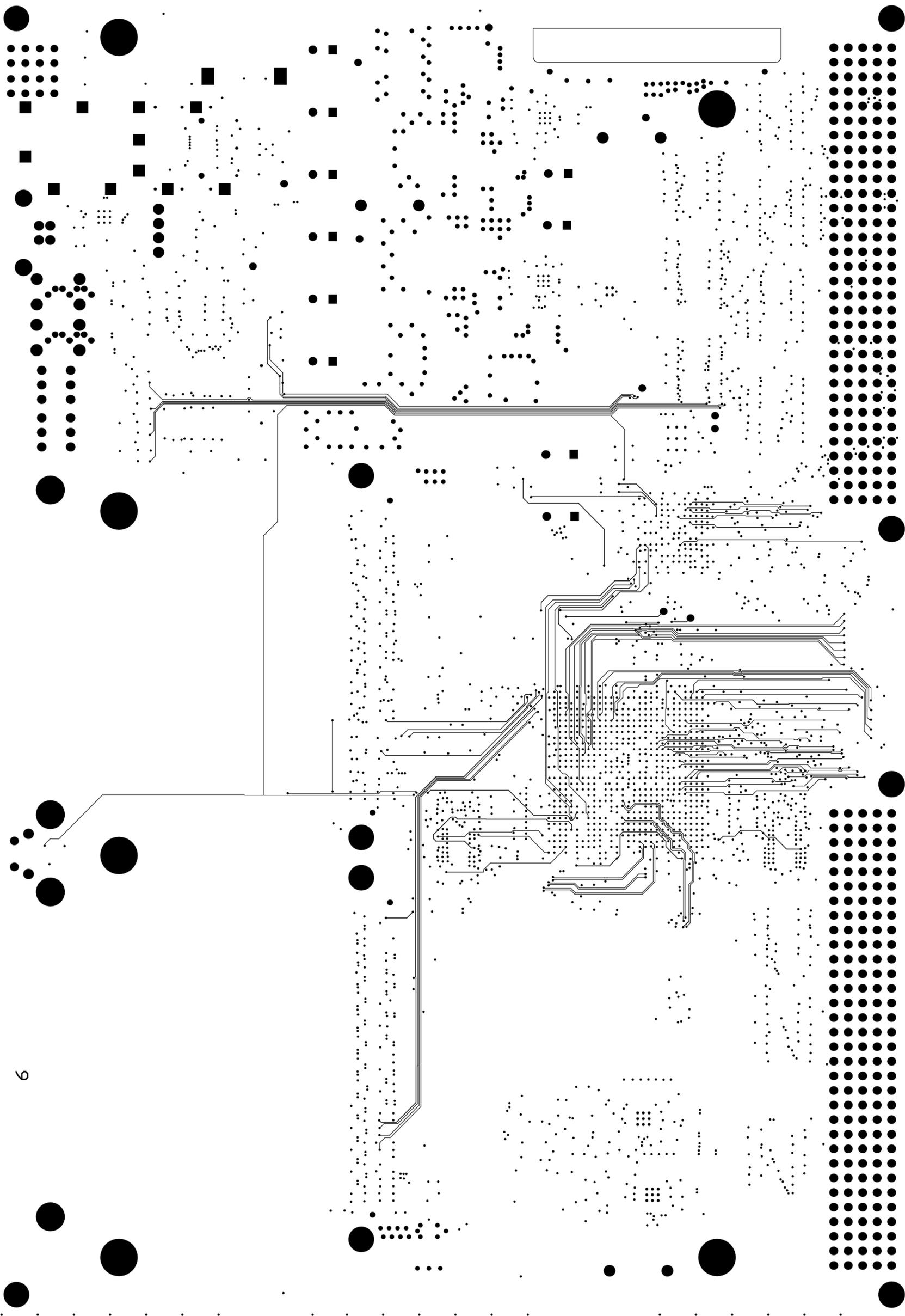


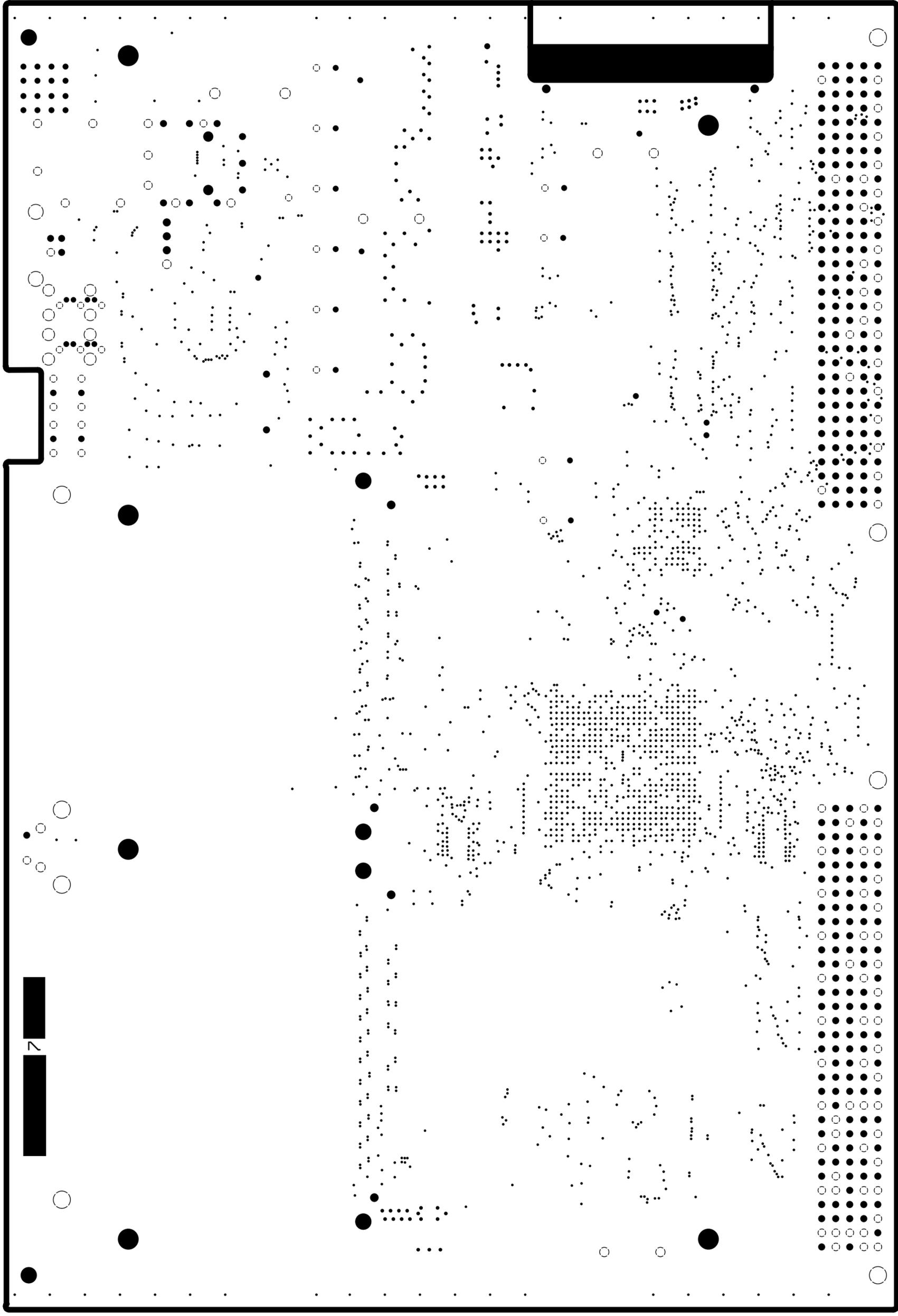


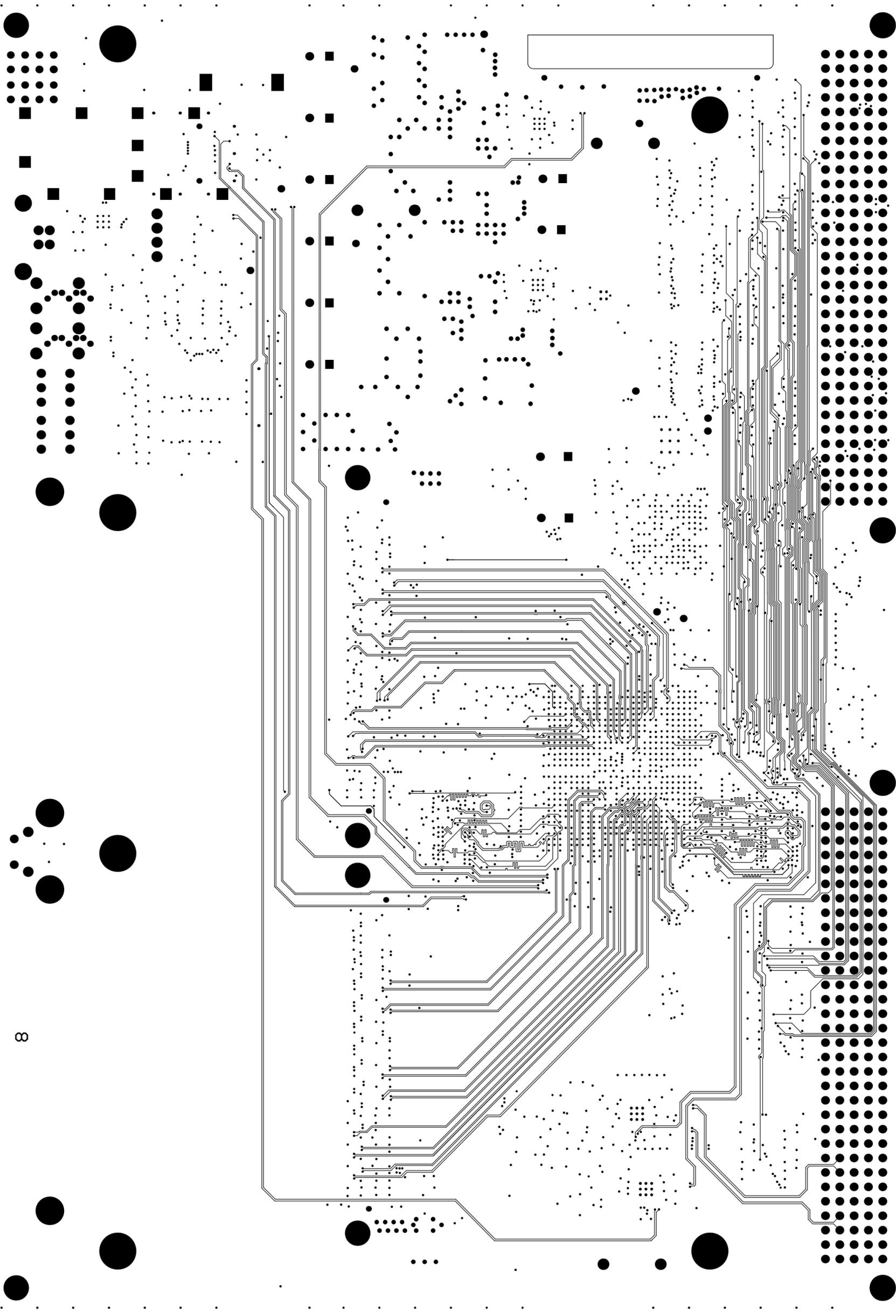


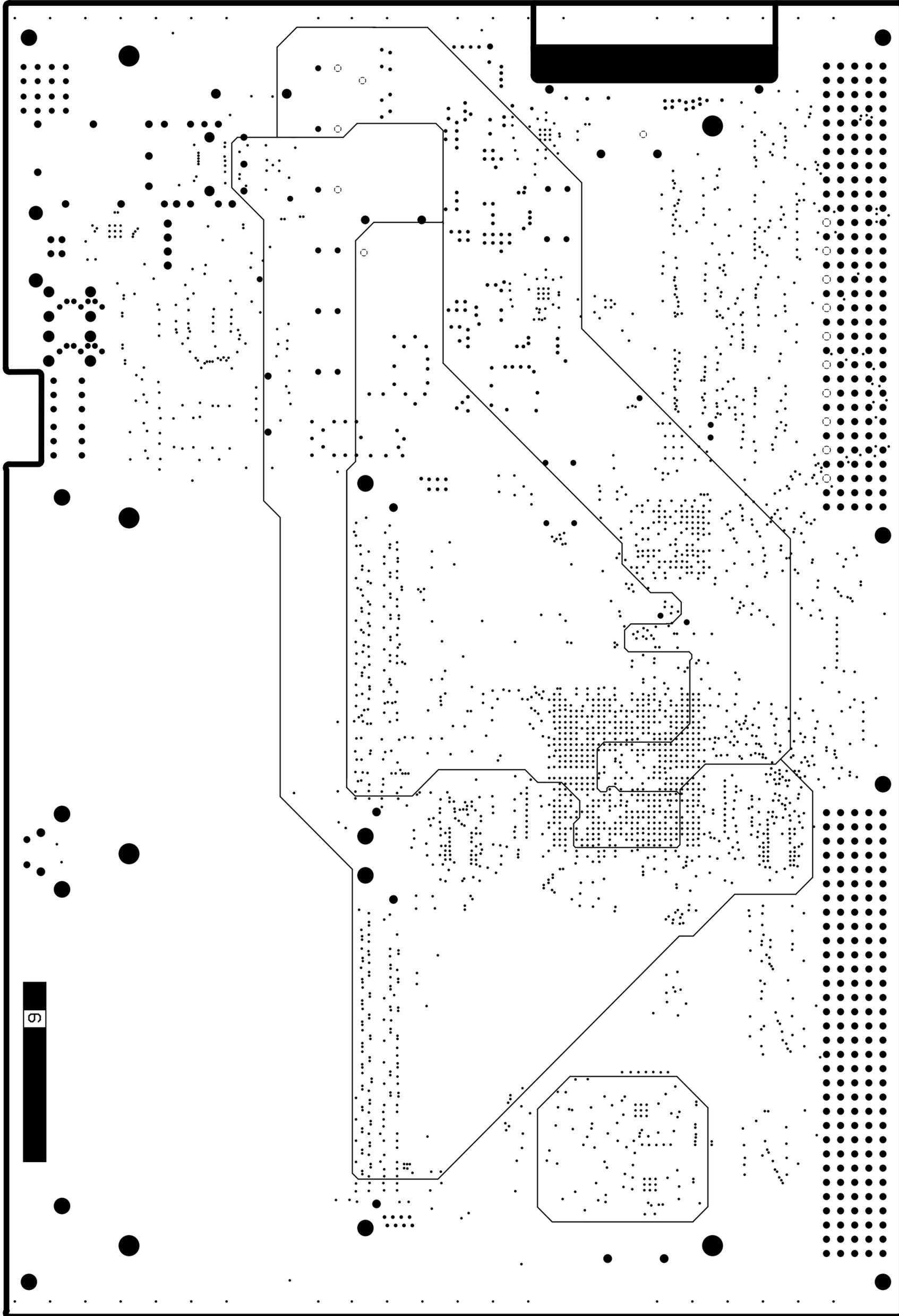
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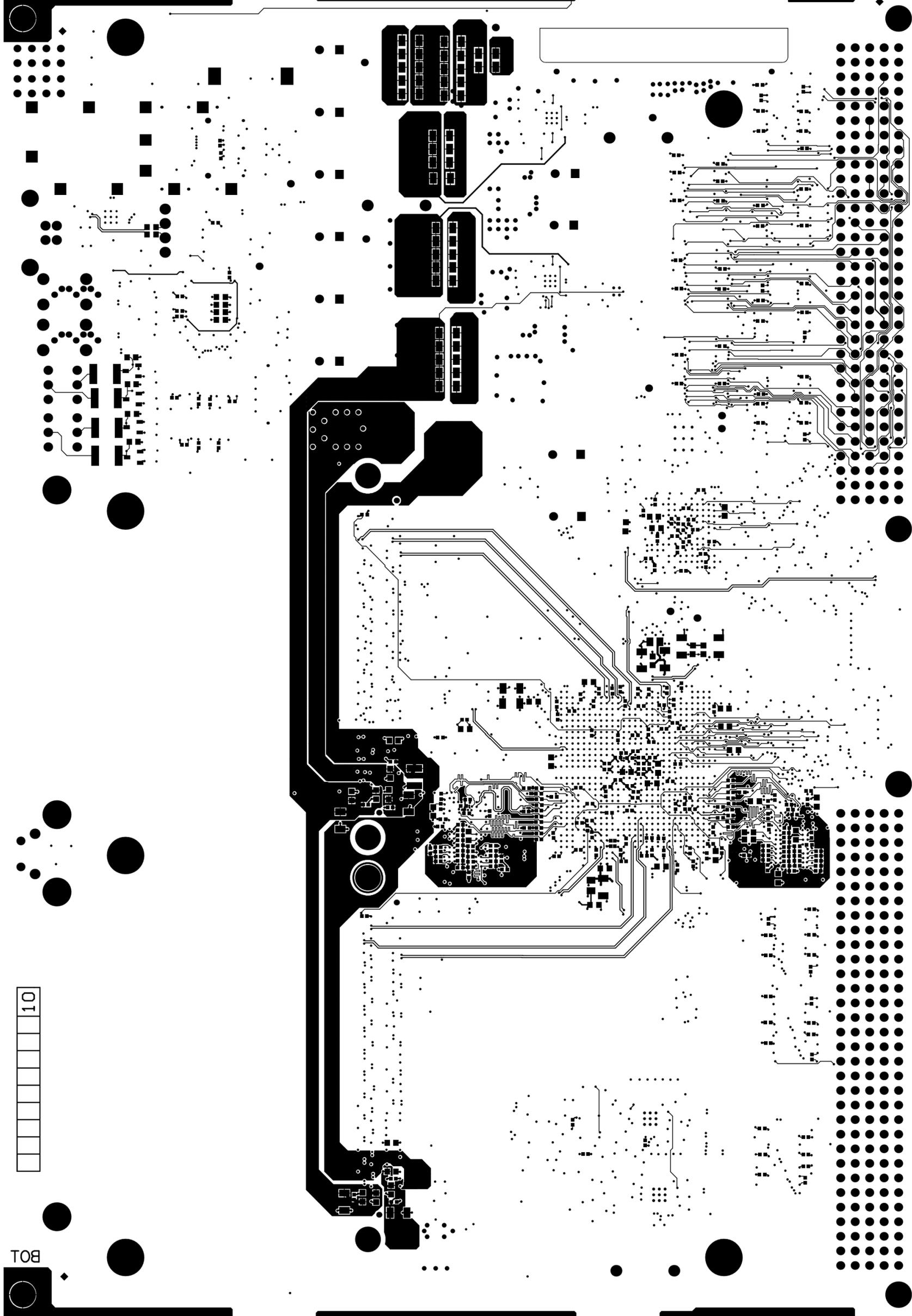






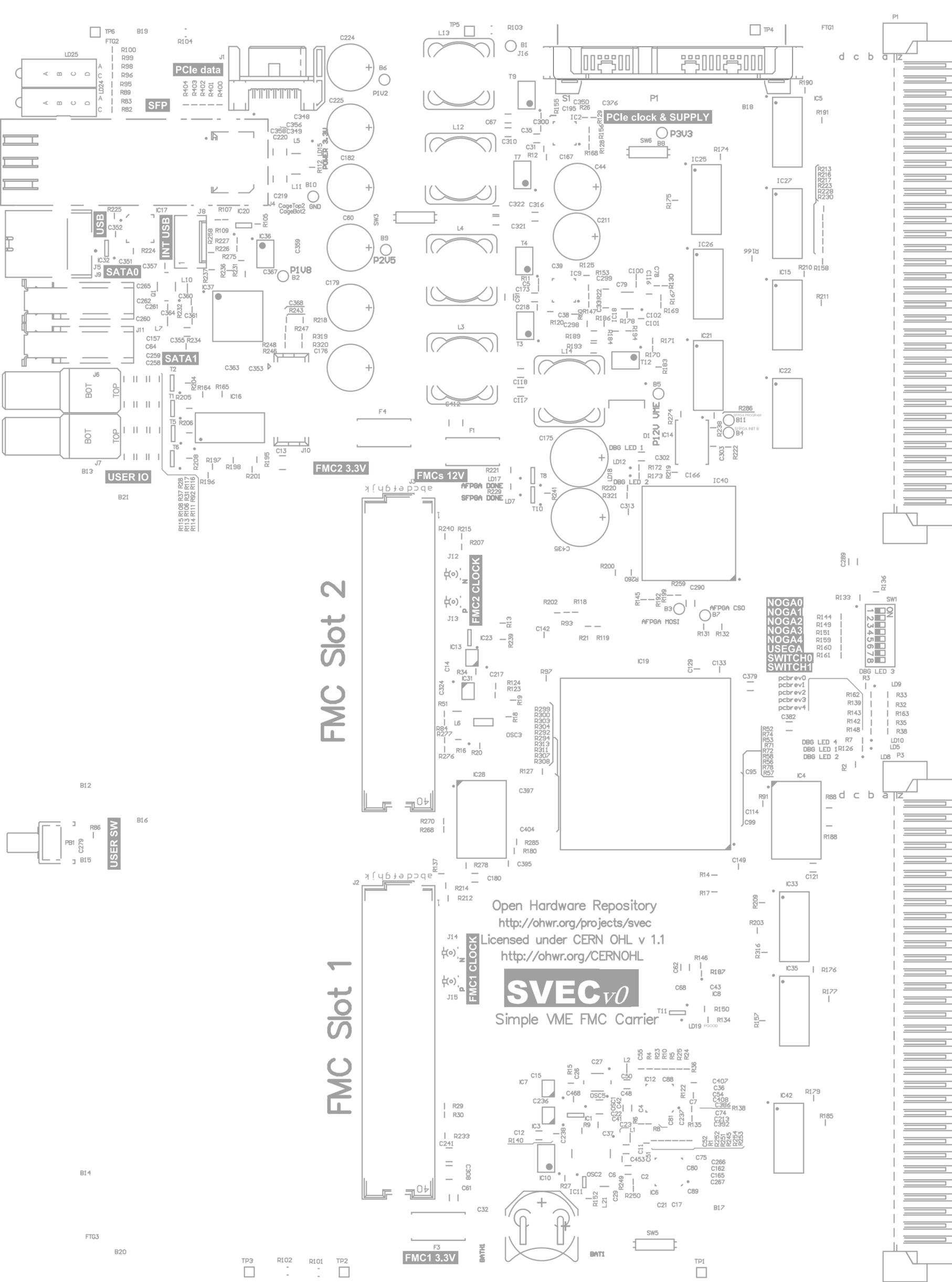






10

BOT



FMC Slot 2

FMC Slot 1

Open Hardware Repository  
<http://ohwr.org/projects/svec>  
 Licensed under CERN OHL v 1.1  
<http://ohwr.org/CERNOHL>

**SVEC v0**

Simple VME FMC Carrier

F3 FMC1 3.3V

F4 FMCs 12V

F5 FMC2 3.3V

F6 FMC2 CLOCK

F7 FMC1 CLOCK

F8 BATT1

F9 BATT2

F10 TP1

F11 TP2

F12 TP3

F13 TP4

F14 TP5

F15 TP6

F16 TP7

F17 TP8

F18 TP9

F19 TP10

F20 TP11

F21 TP12

F22 TP13

F23 TP14

F24 TP15

F25 TP16

F26 TP17

F27 TP18

F28 TP19

F29 TP20

F30 TP21

F31 TP22

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