SPEC7 V2

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# Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
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<th>Description</th>
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<td>0.0</td>
<td>13-03-2020</td>
<td>G C Visser</td>
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<td>P Jansweijer</td>
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<td>0.2</td>
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<td>P Jansweijer</td>
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</tr>
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<td>P Jansweijer</td>
<td>SPEC7.git origin set to ohwr.org.</td>
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<td>24-09-2021</td>
<td>P Jansweijer</td>
<td>add note on 10MHz phase noise bump.</td>
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</tbody>
</table>
1 Safety directions

Please read this chapter before using the SPEC7

- Never exceed the maximum rated input voltage, a higher voltage as stated as maximum will damage the device. See section 8 for maximum allowed voltages.
- The electronics is ESD sensitive, use a safe ESD workplace.
- Although ESD protected, SiliconLabs CP2105 (U54, dual UART) seems to be a weak spot. When the SPEC7 is operated stand alone then the chassis of the PC that is connected to the mini USB connector (X2) must be at SPEC7 ground potential. See also section 1.
2 Introduction

The SPEC7 [4] is the successor of the SPEC [5]. SPEC7 stands for Simple PCIe FMC Carrier, based on Xilinx 7-series FPGAs. More specifically the board utilizes a Xilinx Zynq-7000 FPGA (Z030 or Z035) with Dual-Core ARM processor integrated. The FMC PCIe Carrier is an FMC carrier that can hold one FMC card and an SFP connector. As was the case with the SPEC, the SPEC7 is specifically designed to enable White Rabbit deployment. To facilitate this, the board contains Voltage Controlled Crystal Oscillators (VCXOs) and Digital to Analog Converters (DACs).

The design was optimized for low phase noise. For demanding users (like metrology institutes) the SPEC7 can be equipped with an external oscillator in order to further decrease phase noise. It is left to the demanding user how much money is spend on a better external oscillator such that they can make their own trade-offs. An example design that uses a high precision external oscillator is the High Precision External Slave Clock (HPSEC [3]) design which incorporates a SPEC7.
2.1 Overview of the SPEC7

Xilinx Zynq-7000 devices contain a Processing System (PS) and Programmable Logic (PL). Both PS, PL and their respective connections are shown in the SPEC7 block diagram (figure 1).

2.2 White Rabbit Clocking

The SPEC7 contains an LTC6950 PLL which is used to distribute and generate the White Rabbit 125 MHz reference clock. The LTC6960 needs to be configured via SPI by software.

Two LEDs show the status of the LTC6950. LED D74 is lit red when there is no reference clock found. LED D72 is lit green when the PLL is locked. Without configuration and without reference clock LED D74 is on (default after power up with no FPGA image). Mode bits WR_MODE(1:0) determine how clocks are routed. Table 2 and the paragraphs below explain how clocks are routed according to the WR_MODE(1:0) status.
The following sections describe the White Rabbit modes that can be selected.

### 2.2.1 Mode Slave

Traditionally the SPEC7 is used as a WR-node which means that it operates in mode slave. Figure 2 shows how the DAC is selected to tune the VCXO that feeds the LTC6950. In this mode the PLL is switched off and the LTC6950 is only used as a clock distribution system. In this mode LEDs D72 (Lock) and D74 (NoRef) are both off.

![Figure 2: Clock selection for Mode Slave.](image)

The configuration shown in figure 2 also allows for the traditional WR mode master and mode gm where the 125 MHz VCXO is taken as a reference clock or the 125 MHz VCXO is phase locked and aligned to an external 10MHz source, respectively.

### 2.2.2 Mode Master

The SPEC7 can be operated as a free running master. In this mode an on board TCXO 10MHz oscillator is switched on (see figure 3). This clock is fed to the PLL of the LTC6950. The PLL Charge Pump signal is now tuning the VCXO. The PLL divides by 2 and multiplies by 25 to generate and distribute the 125MHz reference clock. In this mode LEDs D72 (Lock) is on and D74 (NoRef) is off.

<table>
<thead>
<tr>
<th>WR_MODE(1:0)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Reserved</td>
</tr>
<tr>
<td>01</td>
<td>Free-running Master</td>
</tr>
<tr>
<td>10</td>
<td>Slave</td>
</tr>
<tr>
<td>11</td>
<td>Grand Master</td>
</tr>
</tbody>
</table>

Table 2: WR_MODE(1:0) (FPGA pins C12, B12) select White Rabbit Clocking options.
2.2.3 Mode Grand Master

The SPEC7 can be operated as Grand Master. In this mode and external 10MHz (sine-wave) reference (and 1PPS) is applied (see figure 4). This clock is fed to the PLL of the LTC6950. The PLL Charge Pump signal is now tuning the VCXO. The PLL divides by 2 and multiplies by 25 to generate and distribute the 125MHz reference clock. When a reference clock is present then LED D74 (NoRef) should be off. When a reference clock has the proper frequency and the PLL can lock then LED D72 (Lock).

![Figure 4: Clock selection for Mode Grand Master.](image)

2.3 JTAG Header J9

The JTAG chain on the SPEC7 is routed through the Zynq FPGA and the FMC. By default the JTAG chain is connected to the PL of the Zynq FPGA (see table 3). This enables a JTAG connection between the logic in the FPGA and devices JTAG present on the FMC.
The presence of an FMC is detected by the PRSNT_M2C signal. When an FMC card is absent then the FMC connector TDI and TDO are automatically connected by an electronic switch.

A Xilinx Download Cable can be plugged in connector J9 to configure the FPGA. Once a Download Cable is plugged into J9 the JTAG chain it is automatically connected. Presence of a Download Cable is detected by pin 1 of J9 (see figure 5). Most\(^1\) programming cables have pin 1 grounded.

\(^1\)Download cables that do not have pin 1 grounded are Xilinx Platform Cable USB II and Digilent JTAG-HS2. This causes an error “no device detected on target” in Vivado.
3 Specifications

3.1 General

- 2-lane PCIe Gen2
- Xilinx Zynq-7000 FPGA (XC7Z030-1FBG676C) with Dual-Core ARM processor integrated
- Possible upgrade to XC7Z035-1FBG676C or XC7Z045-1FBG676C
- 4 GTX Transceivers (2 used for PCIe, 1 for SFP, 1 external accessible)
- 2 GTX Reference Clocks (1 for PCIe, 1 for WR Clock)
- FMC slot with High Pin Count (HPC) connector (only fully populated as LPC)
- Z035 and Z045 support 4 GTX transceivers DP[3:0], M2C/C2M and 2 extra GTX Reference Clocks
- JTAG accessible from the FPGA. JTAG switches automatically to the download cable when it is plugged.

3.2 Clocking resources

- 1x Fixed frequency 33.33 MHz oscillator for Application Processor Unit (APU)
- 1x 10-280 MHz VCXO controlled by I2C and a DAC with SPI interface. Starts up at 125 MHz (Silicon Labs Si570/Si571, freely usable)
- 1x 125.000 MHz VCXO controlled by a DAC with SPI interface (used by White Rabbit PTP core)
- 1x 124.992 MHz VCXO controlled by a DAC with SPI interface (used by White Rabbit PTP core)
- Low jitter external 10MHz via LTC6950 (supporting mode Grand Master & AbsCal)
- 10MHz TCXO for IEEE1588 v2.1 compliance (see J5.6.1) in Free-running Master mode.

3.3 On board memory

- 1x 8 Gbit (1 GByte) DDR3 connected to the 32-bit wide Memory Interface (main use for the APU)
- 1x 8 Gbit (1 GByte) DDR3 connected to the programmable logic (32 bit wide)
- 2x QSPI 256 Mbit flash PROM for multi-boot FPGA power-up configuration, storage of the FPGA firmware.
- 64K (8K x 8-bit) I2C Serial EEPROM (24AA64T-I/MC) for storing serial number, calibration parameters and other critical data such as the MAC address of the card
- 2x 2K (128 x 8-bit) I2C Serial EEPROM (24AA025E48) which provides EUI-48 (2 MAC addresses for APU and for WR)
- MicroSD slot for flash memory for storing programs

3.4 Miscellaneous

- Thermometer (XADC) and semi-unique ID (DNA_PORTe2) provided by the FPGA
3.5 Front panel containing

- 1x Small Formfactor Pluggable+ (SFP+) cage for fiber-optic transceiver (White Rabbit support).
- Programmable Red and Green LEDs
- FMC front panel

3.6 Internal connectors

- 1x JTAG header for Xilinx programming during debugging
- 1x mini USB Type B connector (serves 2 UARTs, one UART interface of the ARM and one to user logic, e.g. PTP core; Warning! See chapter 1.)
- 1x USB Type A connector connected to USB 2.0 port of the ARM
- Ethernet RJ45 connector, magnetics and MicroChip KSZ9031RNX, 10/100/1000 Mbps PHY (interface to ARM GigE)
- Samtec Bulls Eye connector (BDRA)
- 2x connector for optional cooling fans
- FPGA configuration via JTAG header, via ARM (i.e. Dual QSPI or using [PS PCAP / ICAP] (see chapter 6.1.8 Zynq-7000 SoC Technical Reference Manual)

3.7 Stand-alone features

- External 12V 150W-ATX power supply connector
- USB Type A connector
- mini USB Type B connector (Warning! See chapter 1.)
- 10/100/1000 Mbps copper Ethernet RJ45
- SFP+ cage for fibre-optic transceiver (White Rabbit support)
- 7x LEDs (2x front panel, 4x on PCB, 1x PCI SMB-bus)
- 5x buttons
- 1 PS_POR connected to reset controller
- 1 PS_SRTS_B
- 1 PL system reset
- 1 general purpose
- 1 PROGram button for FPGA
4 SPEC7 Firmware

4.1 SPEC7 reference design and SPEC7 HPSEC design

There are two designs, a SPEC7 reference design and a SPEC7 HPSEC design that have many things in common. Figure 6 is a block diagram which that focuses on the PCIe connections common to both.

As explained in the introduction (see: 2.1) the Zynq FPGA contains a Processing System (PS) and a Programmable Logic (PL) section. A basic processing system is a minimum requirement for FPGA configuration from QSPI (see also Appendix C).

The PCIe endpoint, located in PL, has three BARs:

- **BAR0 (1 MB)** is divided in two 512 KB sections. The lower 512 KB of the address space is connected to A WR PTP Core (WRPC [7]). This connection enables direct access to the DPRAM (that contains the LM32 executable), the virtual UART and other registers that are mapped on the WRPC wishbone bus (for details, please refer to [7]). The upper 512 KB of the address space is reserved. Currently 64 KB (of which only a small portion is used) is connected to a UART that enables a connection to UBoot-UART1 via PCIe.
- **BAR2 (64 KB)** is connected to a DMA engine that is looped back via its AXI stream interface. For the time being, it is implemented for test purposes.
• BAR4 (16 MB) is mapped to DDR memory via the PS. This enables to write PL configuration file from PCIe to DDR such that PL can be configured from DDR using UBoot.

4.1.1 SPEC7 reference design

The SPEC7 reference design operates the SPEC7 like users were used to with the SPEC [5] reference design. A Digital IO FMC [6] can be plugged onto the SPEC7 so 1PPS/10MHz in and 1PPS out signals are available. Table 4 shows which reference design signal is assigned to what DIO LEMO connector.

<table>
<thead>
<tr>
<th>DIO LEMO nr.</th>
<th>Reference design signal</th>
<th>direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PPS</td>
<td>out</td>
</tr>
<tr>
<td>2</td>
<td>n.a.</td>
<td>n.a.</td>
</tr>
<tr>
<td>3</td>
<td>abscal_txts</td>
<td>out</td>
</tr>
<tr>
<td>4</td>
<td>PPS</td>
<td>in</td>
</tr>
<tr>
<td>5</td>
<td>10 MHz</td>
<td>in</td>
</tr>
</tbody>
</table>

Table 4: DIO LEMO connector reference design signal assignment.

4.1.2 SPEC7 HPSEC design

The SPEC7 reference design operates the SPEC7 without DIO card. The design aims for lower phase noise than the "standard" SPEC7 reference design. Differential timing signals (PPS and 10MHz) are routed to the Bulls Eye connector J4. The PPS out signal is re-clocked to remove FPGA switching phase noise. In Grand Master mode the design accepts 10MHz and 1PPS input via connector J4.

Bulls Eye connector J4 provides a well defined high bandwidth connection to the outside world. It should be used when the SPEC7 is deployed in demanding applications where users aim for the highest quality signals, for example when SPEC7 is used in combination with a high precision external oscillator (like the HPSEC design [3]).

4.2 HDL synthesis

Before running the synthesis process you have to make sure your environment is set up correctly. You will need Vivado 2019.2 from your Xilinx vendor.

4.2.1 Downloading the sources

The SPEC7 sources are part of the wr-cores repository. Usually the hdlmake tool is used to gather the sources needed to build the firmware. Unfortunately hdlmake does not support .tcl, "Block Memory Mapping" (.bmm) or Memory Mapping Information (.mmi) files. Tcl scripting is needed for automatic ARM processing system block diagram generation. The .bmm and .mmi files are needed to merge software into the FPGA configuration bitfile without the need for re-synthesis of the firmware.

A top SPEC7 repository facilitates the above. The wr-cores repository, containing the sources, is its submodule:
git clone https://ohwr.org/project/spec7.git
  cd spec7
  git checkout proposed_master
  git submodule init
  git submodule update
  cd hdl/wr-cores
  git submodule init
  git submodule update

Synthesis is started in the corresponding project syn directory. It is important to source the script from the project/syn directory because it contains the project specific files:

- `proj_properties.tcl`: project specific settings (for example target FPGA)
- `proj_file_list.txt`: list of files needed by the project (i.e. the output of `hdlmake list-files` plus a few files that are not supported by `hdlmake`.)

4.2.2 Building the SPEC7 reference design

To build the firmware for the reference design:

```bash
%cd hdl\syn\spec7_ref_design
```

Start Vivado and source the tcl script.

```bash
vivado
%source ..\.\..\..\sw\scripts\viv_do_all.tcl
```

Synthesis en bitfile generation may take quite some time. If the process is successful then you will end up with:

- `spec7_ref_design_z035 YYDDMM HHMM.bit`
- `spec7_ref_design_z035 YYDDMM HHMM.mmi`
- `spec7_ref_design_z035 YYDDMM HHMM.log`

in the syn directory, where YYMMDD HHMM is the build date and time. The .log file contains the SHA codes from the repositories and sub-modules that were used for the build.

4.2.3 Building the SPEC7 HPSEC design

The SPEC7 reference design operates the SPEC7 without DIO card. Timing signals are routed to the Bulls Eye connector J4. In Grand Master mode the design accepts 10MHz and 1PPS input via this connector. The design also generates 10MHz and 1PPS out via this connector.

```bash
%cd hdl\syn\spec7_ref_design
```

Edit “proj_properties.tcl” to select the HPSEC design for build:

```bash
# ==============================================================
# SELECT DESIGN TO BUILD:
# ==============================================================
# Reference Design (using fmc-dio-5chttla => https://ohwr.org/project/fmc
# -dio-5chttla.wikis/home)
# HPSEC Design (using Bulls-Eye connector)
#set spec7_design spec7_ref_top
set spec7_design spec7_hpsec_top
# ==============================================================
```

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Start Vivado and source the tcl script.

```tcl
vivado
%source ..\..\..\..\sw\scripts\viv_do_all.tcl
```

If the process is successful then you will end up with:

- `spec7_hpsec_design_z035 YYDDMM HHMM.bit`
- `spec7_hpsec_design_z035 YYDDMM HHMM.mmi`
- `spec7_hpsec_design_z035 YYDDMM HHMM.log`

in the syn directory, where YYMMDD HHMM is the build date and time. The .log file contains the SHA codes from the repositories and sub-modules that were used for the build.

### 4.2.4 Merging .bit and .elf files

The Vivado installation contains an `updatemem` command. An FPGA configuration .bit file that contains a memory space (like the LM32 memory embedded in wr-cores) can be updated with new memory content (i.e. executable software) using `updatemem`. In order to be able to do this, `updatemem` needs information to locates all BRAM blocks that build up the memory space. This information is provided by the generated Memory Mapping Information .mmi file. One can merge new compiled software in Executable Loader Format .elf with the .bit without the need for time consuming re-synthesis. A script is available to merge an .elf file with a .bit and .mmi file using `updatemem`.

First get into the project directory; the location of the new build .bit and .mmi.

```cmd
cd ..
next
```

```cmd
..\..\sw\scripts\do_vivado_mmi_elf.cmd <bitfile>.bit <elffile>.elf
```

which will generate a `bitfile_elf.bit`. 

---

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5 Connector pinout

This section describes the various connectors which are available on the SPEC7.

5.1 J4: Samtec Bulls Eye connector

Table 5 shows the pinout of Bulls Eye connector J4. The pin number assignment is shown in figure 7. On the PCB the connector is just a land pattern that accepts a Samtec BDRA assembly (see figure 8).

To order a BDRA assembly the following part number is recommended BDRA-92SPP-02-12-0500 (12 pairs, 2.0 ps phase matched, 2.92 mm Straight Plug, length 0.5 m). Individual coaxial cables (BE23) can be extracted by a special tool with part number CAT-EX-SCC-03.

<table>
<thead>
<tr>
<th>Pin Nr</th>
<th>Description</th>
<th>Levels</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>P PPS_OUT</td>
<td>LVPECL</td>
<td>DC coupled</td>
</tr>
<tr>
<td>A2</td>
<td>N PPS_OUT</td>
<td>LVPECL</td>
<td>DC coupled</td>
</tr>
<tr>
<td>A3</td>
<td>P 10 MHz_OUT</td>
<td>LVPECL</td>
<td>AC coupled</td>
</tr>
<tr>
<td>A4</td>
<td>N 10 MHz_OUT</td>
<td>LVPECL</td>
<td>AC coupled</td>
</tr>
<tr>
<td>A5</td>
<td>P 125 Reference Clock out</td>
<td>LVPECL</td>
<td>AC coupled</td>
</tr>
<tr>
<td>A6</td>
<td>N 125 Reference Clock out</td>
<td>LVPECL</td>
<td>AC coupled</td>
</tr>
<tr>
<td>A7</td>
<td>P TX Spare GTX OUT</td>
<td></td>
<td>AC coupled</td>
</tr>
<tr>
<td>A8</td>
<td>N TX Spare GTX OUT</td>
<td></td>
<td>AC coupled</td>
</tr>
<tr>
<td>A9</td>
<td>P ABSCAL_TXTS OUT</td>
<td>LVDS</td>
<td>DC coupled</td>
</tr>
<tr>
<td>A10</td>
<td>N ABSCAL_TXTS OUT</td>
<td>LVDS</td>
<td>DC coupled</td>
</tr>
<tr>
<td>A11</td>
<td>P General Purpose Spare out</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A12</td>
<td>N General Purpose Spare out</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1</td>
<td>P PPS_IN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B2</td>
<td>N PPS_IN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B3</td>
<td>P 10 MHz_IN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B4</td>
<td>N 10 MHz_IN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B5</td>
<td>P Reference Clock in GTX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B6</td>
<td>N Reference Clock in GTX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B7</td>
<td>P RX Spare in GTX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B8</td>
<td>N RX Spare in GTX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B9</td>
<td>P DMTD Spare IN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B10</td>
<td>N DMTD Spare I</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B11</td>
<td>PPS IN Single ended, 5V TTL, DC coupled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B12</td>
<td>NC Not Routed</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 5: J4, Samtec bulls eye connector
5.2 X4: ATX power connector

The SPEC7 can be powered stand-alone via connector X14 which is compliant with the PCI Express x16 Graphics 150W ATX specification see [9], [10]. Additional power may also be applied via X4 when the maximum allowed PCI-express slot power, that can be delivered by the motherboard, is exceeded. Molex part number 0455590002 is recommended as mating connector. Maximum input voltage and current ratings are stated in the following chapter 8.
5.3 J3: FMC connector

In order to be compatible with the previous version of the SPEC [5] Vadj is fixed to 2.5V. Note that the IO lines of the FMC connector have no additional ESD protection. Therefore, please respect ESD rules.

The FMC connector is fully populated according to the Low Pin Count (LPC) signal definitions [8]. The SPEC7 FMC connector is a High Pin Count (HPC) type which allows for the possibility to access 4 additional GTX transceivers on signal pins DP[3:1]. The pin list is show in table 7 and the pin potions are shown in figure 10.

Table 7: Pinout FMC

<table>
<thead>
<tr>
<th>Pin Nr</th>
<th>Pin Name</th>
<th>Remark</th>
<th>Pin Nr</th>
<th>Pin Name</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>DGND</td>
<td></td>
<td>B1</td>
<td>-</td>
<td>NC</td>
</tr>
<tr>
<td>A2</td>
<td>DP1_M2C_P</td>
<td></td>
<td>B2</td>
<td>DGND</td>
<td></td>
</tr>
<tr>
<td>A3</td>
<td>DP1_M2C_N</td>
<td></td>
<td>B3</td>
<td>DGND</td>
<td></td>
</tr>
<tr>
<td>A4</td>
<td>DGND</td>
<td></td>
<td>B4</td>
<td>-</td>
<td>NC</td>
</tr>
</tbody>
</table>

Continued on next page
<table>
<thead>
<tr>
<th>Pin Nr</th>
<th>Pin Name</th>
<th>Remark</th>
<th>Pin Nr</th>
<th>Pin Name</th>
<th>Remark</th>
</tr>
</thead>
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Figure 10: FMC Connector J3.
6 Measured Data

The following chapter presents measured results. All measurements are done with the default firmware for the SPEC7.

6.1 Phase Noise

The following setup is used to measure the phase noise of the SPEC7 card as shown in figure 11. For more information about the custom 125 MHz reference generator see appendix A. Phase noise is measured at point C using a Rohde & Schwarz phase noise analyzer (FSWP). Point C is the Bulls Eye connector.

![Diagram of phase noise measurement setup]

Figure 11: Phase noise measurement setup

![Phase noise 10 MHz output plot]

Figure 12: Phase noise 10 MHz output (J4 A03/A04).

A small bump around 13 KHz can be seen in the phase noise plot of figure 12. The cause of the phase noise around 13KHz can also be seen in the spectrum and spectrogram of figure 13. The noise sources are the 2V5 and 1V8 Switched Mode Power Supplies (N6, N5: Intel EN6347QA). Keep in mind that this noise has no major effect since it only reaches -135 dBc/Hz over a limited bandwidth.
Figure 13: Spectrum of the 10 MHz with some noise at 13 KHz distance from the carrier.

The phase noise between $10^5$ and $10^6$ in figure 12 is caused by the 500 MHz MMCME2_ADV PLL in the FPGA that is used in the spec7_ref_design to create a White Rabbit phase aligned 10MHz.

![125 MHz Phase Noise](image)

Figure 14: Phase noise 125 MHz output (J4 A05/A06).

### 6.2 Spurs

The figures below show the frequency spectrum for the 10 MHz and 125 MHz outputs.
Figure 15: Spectrum 10 MHz Output.

Figure 16: Spectrum 125 MHz Output.

6.3 Time Domain
6.4 Restart Error

![Figure 17: PPS Restart Error measurement setup.](image)

6.5 PPS Pulse to Pulse Jitter

6.6 Boot time on board flash memory

The SPEC7 is capable of booting from a dual Quad-SPI flash memory setup. Two Micron [2] chips (2x MT25QL256ABA8E12-1SIT in a Dual QUAD SPI configuration) are present on the card and connected to the Zynq Processor System. The SPEC7 can reach boot times down to 735 milliseconds. This can be seen in figure 19, where the 12V supply voltage (red) is depicted along an user application (green), the yellow line is a probed qspi clock signal to display when the memory is being accessed.

![Figure 18: PPS Restart Error.](image)
Figure 19: QPSI boot time of an uncompressed bitfile. Notice how the QSPI clock signal (yellow) is divided into two “stages”. The first is the Bootloader being loaded into the Zynq, the second stage is the bitstream being loaded into the programmable logic.

These 735 milliseconds are currently a worst case scenario. Boot times can be greatly reduced by enabling bitsream compression [13], along with other optimizations [12]. An example of booting a compressed bitstream is depicted in figure 20 where the boot time is reduced to 265 milliseconds.

Figure 20: QPSI boot time of a compressed bitfile.
7 PCIe interface

The PCIe interface is only tested on the physical level for transaction rates 2.5GT/sec and 5GT/sec. The device under test is a Zynq Z035 device. The 2.5GT/sec eye diagram is shown in figure 21. The 5GT/sec eye diagram is shown in figure 22.

Figure 21: PCIe 2.5GT/sec eye diagram.

Figure 22: PCIe 5GT/sec eye diagram.

More information about the test setup can be found in appendix D. Figure 23 shows the SPEC7 being recognized by the operating system (i.e. “lspci”).
Figure 23: Example result of lspci: SPEC7 is recognized
8  Power & Maximum Ratings

8.1 Power Ratings

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Unit</th>
<th>Tolerance</th>
<th>Note</th>
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<td>Input voltage Range</td>
<td>12</td>
<td>V</td>
<td>+/-5%</td>
<td></td>
</tr>
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<td>Absolute Maximum input voltage</td>
<td>12.65</td>
<td>V</td>
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<td>Note 1</td>
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<td>Nominal current draw</td>
<td>1</td>
<td>A</td>
<td></td>
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</table>

Table 8: ATX power connector

1. **Stress above the stated voltage will damage the SPEC7 and/or a possible connected FMC mezzanine.**
2. **The stated current is only when a White rabbit core is loaded, the actual current consumption heavily depends on your end application**

8.2 Power Up Sequence

The SPEC7 can either be powered when plugged into a PCIe slot or it can be used standalone by using an external 12V power supply. When plugged into a PCIe slot then the main power of the SPEC7 is derived from 12V on the PCIe connector while the FMC card is powered by 3V3 on the PCIe connector. This is done in order not to exceed the maximum power that may be drawn per PCIe slot.

Many different voltages are needed by the Zynq FPGA and DDR3 memories. The power supplies are enabled sequentially. Figure 24 shows the power sequence after 12V is applied. First 3V3 non-switched (3V3_NWS) is created by the 10A switched mode power supply N2. Next 1V35 is enabled which serves as a pre-regulator for the 1V0 VCCINT regulator. Finally VCCINT is supplied by a linear regulator in order to create a low noise 1V0 voltage since the phase noise performance of the FPGA depends on the quality of VCCINT.

![Power Sequence Diagram](image)

Figure 24: Power Sequence: 12V input ⇒ 3V3 Non Switched ⇒ 1V35 PreCore ⇒ 1V0 VCCINT

Figure 25 shows the power sequence of power supplies for the FPGA. After VCCINT is applied then the FPGA BANK voltages 1V8, 1V35 and 2V5 are supplied.
When all FPGA voltages are supplied then finally 3V3 is enabled. In order to lower the inrush current MOSFET V3 is switched on gradually as can be seen in figure 26.

Depending on whether the SPEC7 is powered by a PCIe slot or by an external power supply, either MOSFET V2 or V4 is gradually switch on to enable 3V3 for the FMC card (see figure 27).
8.3 Power Down Sequence

Xilinx DS191 [11] paragraph “PS Power-On/Off Power Supply Sequencing” states: “Before VCCINT reaches 0.80V the reference clock to the PS_CLK input is disabled to ensure PS eFUSE integrity.” Figure 28 shows that this condition is met.

![Power Down Sequence Diagram](image)

Figure 28: Power Down Sequence
9 Optional Heatsink, Fans and RF-Shielding

The SPEC7 may be optionally be equipped with a heatsink, fans or an Clip-On EMI Shielding Can. Table 9 shows manufacturers and part numbers that will fit the SPEC7 design.

9.1 Heatsink

Depending on the application the Zynq FPGA on the SPEC7 may need a heatsink and/or a fan. The type of heatsink that will fit on the SPEC7 is a "Square Skived Fin 50mmx50mm, Height=14mm, mounted on PCB", Manufacturer AAVID, Part Number 342943 (see figure 29). Note that the total height of the heatsink (14 mm) plus Zynq (2.44 mm) is now 16.44 mm while the PCIe specification restricts the total height to 14.47mm. Unfortunately this is inevitable since a market survey showed that there were no other suitable cooling profiles found on the market. If a cooling profile is necessary and the total height poses a problem then a work around is to mill-off 2 mm from the profile.

Figure 29: Heatsink AAVID 342943

9.2 Fans

A 5V DC fan for the FPGA can be connected to connector X3. The FPGA fan can be controlled via FPGA pin AD26.

For FMC cards that need cooling, a 5V DC fan can be mounted in at the back of the SPEC7 at the location of the hole in the PCB. Both a fan from Sunon Fans, part number "UB5U3-700" (see figure 30) or "Delta Electronics", part number "KDB0305HA3-00C1J" will fit. The fan can be connected to X1 and can be controlled via FPGA pin AD25.

Figure 30: Sunon Fan UB5U3-700
The counterpart for X1 and X3 is a Molex connector, part number 0022013027.

9.3 RF-Shielding Can

The SPEC7 is equipped with RF Shield Clips such that a Clip-On EMI Shield can be placed over the clocking circuits to minimize phase noise degradation due to external EMI noise sources. Placing of this EMI shield is optional. All measurements that are reported in this document are performed without a shield.

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<td>Holland Shielding</td>
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Table 9: Optional Heatsink, Fans, Connecto, RF-Shielding Can
10 Known bugs & Errors

1. The EN pin of U28 is '1' which enables OUT0/1 but disables OUT2/3. In contrast to what is stated in the schematics, Table 1 of datasheet CDCLVD2102 see [1] shows that both outputs are enabled when EN is "open"

2. Although ESD protected, SiliconLabs CP2105 (U54, dual UART) seems to be a weak spot. When the SPEC7 is operated stand alone then the chassis of a PC that is connected to the mini USB connector (X2) must be at SPEC7 ground potential.

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Appendices

A  125 MHz reference generator

Figure 31 shows a block diagram of the 125 MHz reference generator that is custom made and build around a 10 MHz master source (Morion MV336M-A005D-10.0MHz-ULN-1.5E-13). This is an OCXO with exceptional low phase noise, very good short term stability (Allan deviation) of up to $1.5 \times 10^{-13} \delta(t)$ per 1 sec.

![Block Diagram of 125 MHz Reference Generator](image)

Figure 31: Phase noise measurement setup 125 Mhz reference generator.

The phase noise of the OCXO is plotted in the following figure 32. This is measured on position A. For completeness the phase noise at position B (1 GHz) is show in figure 33. The final output frequency 125MHz on position C is shown in figure 34.
Phase noise power levels (in dB) will increase when multiplying and decrease when dividing frequency, according to equation (1) where $N$ is the multiplication factor.

$$20 \times \log_{10}(N)$$  \hspace{1cm} (1)

Phase noise power level at 1 GHz is expected to be 40 dB higher than at 10 MHz ($N = 1\text{GHz}/10\text{MHz} = 100$). In addition the PLL phase noise is added.

It can be seen that the oscillator phase noise at 10 Hz (where the plateau starts) is approximately -142 dBc/Hz (figure 32) so the phase noise to be expected at 1 GHz is at least -102 dBc/Hz. The actual measured phase noise at 1 GHz (figure 33) at 10 Hz is approximately -92 dBc/Hz. This leads to the conclusion that additive phase noise of the PLL (HMC 704) is 10 dB. For a next design it should be considered to use a PLL that performs better.

The bandwidth of the PLL is set to $\approx 500$ Hz hence the bump in the phase noise plot.
Phase noise power level at 125 MHz is expected to be 18 dB lower than at 1 GHz ($N = \frac{1}{8}$). The actual measured phase noise at 125 MHz (figure 34) at 10 Hz is approximately -110 dBC/Hz.

Figure 34: Phase noise @C: 125 MHz OCXO MV336M
B SPEC7 10 MHz phase noise output HPSEC versus WR-LJ

Figure 35 shows the 10 MHz phase noise when using the SPEC7 as a slave device, either:

- connected to a White Rabbit Low Jitter switch (WRS-LJ), or
- connected to a SPEC7 in master mode that is clocked by a 125 MHz reference generator (see Appendix A)

10 MHz Phase Noise comparsion

![Graph showing 10 MHz phase noise comparison between HPSEC and WRS-LJ](image)

Figure 35: Compare SPEC7 slave 10MHz phase noise when using a HPSEC versus a WRS-LJ as master
C How to boot from QSPI

The SPEC7 is capable of booting from on board dual QSPI flash. In order to do so, a HDL design containing a ZYNQ Processing System (PS) IP core must be used. This section describes the process of flashing your design into the QSPI flash memory. This “How-to” uses Vivado 2019.2 and Vitis 2019.2.

1. Make sure that your design has the Zynq Processing System IP core. The IP core does not need to “do” anything. The PS is needed to transfer the FPGA configuration from QSPI via the PS to the Programmable Logic (PL). After the transfer it may idle.

2. Generate your bitfile as you would do normally.

3. In Vivado, go to: File → Export → Export Hardware. Check “Include bitfile” and click “OK”. Remember the path provided here.

![Figure 36: Export Hardware window in Vivado.](image)

4. In Vitis, go to: File → New → Platform project. Make up a name for your platform (for example “SPEC7.Z035”) and hit “Next”.

5. Check “Create from hardware specification (XSA)” and hit “Next”.

6. Click “Browse” and provide the XSA file on the path specified in step 3. And click on “Finish”.

7. Include the Xilffs package by clicking on the “platform.spr” file and modify the BSP in the standalone domain to include xilffs. As can be seen in figure 37.
8. Build the project by clicking on the build icon in the menu bar, or press Ctrl+B.

9. Now to build a First Stage BootLoader (FSBL), go to: File → New → Application project. Make up a name for your bootloader (for example “SPEC7_FSBL”) and click “Next” three times.

10. Select “Zynq FSBL” as template and click “Finish”.

11. (Optional) To significantly decrease boot time, change line 251 in the file qspi.c in the bootloader project from “XQSPIPS_CLK_PRESCALE_8” to “XQSPIPS_CLK_PRESCALE_2”.

12. Build the bootloader by clicking on the build icon in the menu bar, or press Ctrl+B.

13. Go to: Xilinx → create boot image. Specify a location for the .bif file by clicking on “Browse”. Select MCS as output format.

14. Click on “Add” in Boot Image Partitions to specify the first stage bootloader (.elf) file, generated in step 12”. Set the partition type to “Bootloader” and click on “OK”.

15. Click on “Add” another time and specify your bitfile and click on “OK”. Your “Create Boot Image” window should look something like figure 38.
16. Click on “Create Image” and wait for the MCS file to be generated.

17. Make sure the SPEC7 is in JTAG mode by checking the DIP switches of S3. switch 2,3 and 4 should be “zero” by facing the right side of the pcb (towards the printed numbers on the switch). See figure ?? how they look.

18. Go to: Xilinx → Program Flash. Double check if the .MCS and .elf files are the same as the ones generated in step 16 and 12. Then check if the flash type is set to “qspi-x8-dual-parallel”. As can be seen in figure 39.
19. Click on “Program” and wait (a while) for the programmer to write the flash memory.

20. After the flash operation has finished, power down the board. Change the number two Switch on S3 to the “one” position, facing the left side of the board.

21. Finally power on the SPEC7, booting should be finished within one second.

22. See how to program or flash the following section ??

D Physical layer PCIe test set up

It should be noted that not all PCIe compliance tests are performed, only basic transmitter eye diagram measurements where performed for data rates 2,5GT/S and 5GT/S. The card is inserted in the PCI Express GEN-3 Compliance Base Board (CBB [9]) see figure 40, the CBB is test fixture where all the high speed differential lines are routed to SMP coax connectors to hook up test equipment.
Figure 40: PCIe CBB setup

For reference purposes the schematic of the spec 7 is shown.

E Schematics
Note: Bank 111 reference clocks can be routed and used in Bank 112 GTX.

If high precision external oscillator is used then BE_REFCLK is the used as 125 MHz reference Clock.

Available in:
Z035, Z045

General GTX remark:
See also UG476 Table 5-7
GTX/GTH Transceiver PCB Design Checklist.
LPC FMC

Note that only LPC FMC signals are implemented.

In addition, partial HPC multi-gigabit transceiver data pairs and all HPC grounds implemented.

Vadj fixed 2V5

The HR/HR of the 2V5 only allow 13 DB_25 at VCCO 2V5

(U9471 table 1-43).

Notes
Avoid floating TXD outputs when CP2102 is in "Suspend" mode. See paragraph 5 of CP2102 data sheet.
High speed signal Impedance 101 Ohms DIFF

INF-8074 (SFP) Pin7 = Rate Select (High=Fall B0), Pin9 = VeeR
SFF-8431 (SFP+) Pin 7 = RS0, Pin9 = RS1 (See SFF-8431 2.4.3)

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PL_SFP_Connector 11300.01.05.2 SPEC7 v2 crystek Powered

G. Visser & P. Bos & P. Jansweijer
WRITE 2020-01-31

L17 1uH
L18 1uH
C483 22uF
C484 100nF
C485 1uF
C486 1uF
C487 100nF
C504 1uF

ESDM3031MXT5G V14
ESDM3031MXT5G V15
ESDM3031MXT5G V16
ESDM3031MXT5G V17
ESDM3031MXT5G V18
ESDM3031MXT5G V19
ESDM3031MXT5G V20
ESDM3031MXT5G V21

High speed signal Impedance 101 Ohms DIFF

Bank M (1V8) via 3V3 / 1V8 level shifter

High speed signal Impedance 101 Ohms DIFF

INF-8074 (SFP) Pin7 = Rate Select (High=Fall B0), Pin9 = VeeR
SFF-8431 (SFP+) Pin 7 = RS0, Pin9 = RS1 (See SFF-8431 2.4.3)
DNP 1MEG, Write Protect default False.

The Board Version can be hardcoded with the register array and readback via the FPGA. Current version = 1

Bank 35 (1V8)

Molex 502774-0891 datasheet:
- pin 9: "Detect Nail (ground side)"
- pin 10: "Switch Nail"

Bank 501 (2V5)

UG585, Table 6-4 MIO[8:2]

PCB Design GuideUG933, Par. SDIO

UG585 Chapter 6.3.7: "In SD card boot mode, the BootROM does not perform a header search and does not support multiboot."

Notes

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Designed by
G. Visser & P. Bos & P. Jansweijer

Drawn by

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Drawn by
ZYNQ always in JTAG chain

Note 2V5 > Vih_min (0.7*3V3) on JTAG chain switch

Possibility to put 0 ohm for FMC mezzanines that do not connect TDI-TDO

Optional TRST_L control using the HALT signal (see DS593).

'0' when JTAG cable is plugged
ELSE '1' => JTAG control from FPGA PL

TRST_L Default

IEEE-1149.1 Par. 4.2.2
IEEE-1149.1 Par. 4.3.2
IEEE-1149.1 Par. 4.4.2

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Default Reset sources force a PS_POR, i.e., PL is configured from Flash using standard ZYNQ boot via CPU0. Exchange 1MRG and 0 MHz to direct PL configuration (i.e., without using CPU0).

Subline 31 = Reset threshold 3.08V. Csur=22mF -> 60 ms.

SMBus 10 Falling Edge triggers FPGA reconfiguration

SMBus I/O Expander Falling Edge triggers FPGA reconfiguration

At Reset the I/Os are configured as inputs with 100K pullup.

For example check SMBus connection.

The optional low speed signals are defined to use the +3.3V or +3.3Vaux supplies

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Onboard EEPROM for Calibration parameter storage.

48 bit Unique ID (WWID MAC Address)
1V8 capable but fmax = 100 KHz for VCC < 2v5
See datasheet 24AA025E48

Device Selection Table Note 1

<table>
<thead>
<tr>
<th>VCC</th>
<th>VSS</th>
<th>SDA</th>
<th>SCL</th>
<th>A0</th>
<th>A1</th>
<th>A2</th>
<th>WP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1V8</td>
<td>DGND</td>
<td>DGND</td>
<td>DGND</td>
<td>1V8</td>
<td>DGND</td>
<td>DGND</td>
<td>DGND</td>
</tr>
</tbody>
</table>

On board EEPROM for Calibration parameter storage.

I2C ADDR = 1010.000x
I2C ADDR = 1010.001x

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SPEC7 v2 crystek Powered 2020-01-31

G. Visser & P. Bos & P. Jansweijer

11300.01.05.2

PL_EEPROM_Unique_ID
PS, POR, B, see also DS191 PS and PLI. Power-On/Off Power Supply Sequencing.

UG885 Par 6.1
Immediately after the PS, POR, B reset grounds the lead edge samples the boot string and optionally enables the PS clock PLL. Then, the PS begins executing the BoardROM code in the on-chip ROM to boot the system.

UG885 Par 6.2.4 "External Reset Signal Pin" eFuse integrity
On PCIe superiency circuit ensures that PS_POR_B asserted low before VCCINT reaches 0.80V.

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3V3 @ 10A

Vout max = 3.6 V

Note: POK = Power is ok when Vout is +/- 10%  POK = Open Drain, High is ok.

When EN_3V3 And PCI_3V3 then route 3V3_PCI to 3V3_FMC
When EN_3V3 And NOT PCI_3V3 then route 3V3_NSW to 3V3_FMC

Slowly turn on FET V3 to reduce inrush current.

When EN_3V3 And PCI_3V3 then route 3V3_PCI to 3V3_FMC
When EN_3V3 And NOT PCI_3V3 then route 3V3_NSW to 3V3_FMC

Over Voltage Protection set to 3.45V.
EN_5V is a logic level signal that is enabled when Ven-h > 1V4

LMZM3603 datasheet Table 1:
Vin = 12V, Vout = 5V
Rf = 88.7 K (fsw=450 Khz)
Rfbt = 40.2 K
Ceff = 100 pF
66 uF < Cout <200 uF

EN_5V is a 3V3_NWS powered logic signal

Place as close as possible to switcher

5V @ 3A

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Mechanical Parts

- Frontpanel for SPEC Card  
- Steel Bracket for SPEC Card, Up  
- Steel Bracket for SPEC Card, Down  
- M5x6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated  
- M5x6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated  
- M5x6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated  
- M5x6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated  
- SPEC 7v2 PCB, PCIe, 14Layers  
- FPGA Heatsink

Sheathing for PL WR VCXOs

- MP13 3200-0478  
- MP14 3200-0476LC  
- MP15 3200-0477LC  
- MP16 BN-330-1123238  
- MP17 BN-330-1123238  
- MP18 BN-330-1123238  
- MP20 11300.01.01.2  
- MP21 UB5U3-700  
- DC Fan, 30x30x3mm, 5V/0.35A, 9500RPM  
- MP22 M1.7x? Pan Head Screw  
- MP23 M1.7x? Pan Head Screw  
- MP24 M1.7x? Pan Head Screw  
- MP25 M1.7 Washer  
- MP26 M1.7 Washer  
- MP27 M1.7 Washer  
- MP28 M1.7 Nut  
- MP29 M1.7 Nut  
- MP30 M1.7 Nut  

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