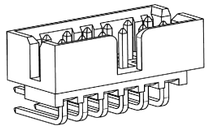
SPEC7_JTAG_Chain
Sheet 26



FMC_JTAG
PRSNT_M2C_L
ZYNQ_JTAG
PL_JTAG

PS_USB_OTG
Sheet 22

USB Type A (2.0)

USB_OTG

PL_USER_IO
Sheet 25

SD_CARD
BOARD_VERSION
PL_User_IO

PL_PS_UART
Sheet 23

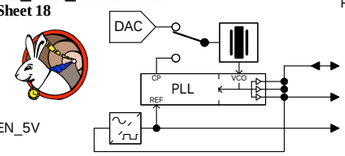
Mini USB Type B

PL_PS_Dual_UART

PL_I2C EEPROM_Unique_ID
Sheet 28

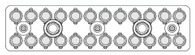
EEPROM_UID

PL_WR_Oscillators
Sheet 18



EN_5V
PL_WR_DACS
PLL_CTRL
BULLS_EYE
WR_CLOCKS
10MHZ_CLK

PL_BullsEye
Sheet 21

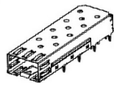


WR_CLOCKS
BULLS_EYE
TIMING_SIGNALS

PL_SI570
Sheet 29

PL_SI57X

PL_SFP_Connector
Sheet 24



PL_SFP

USB_OTG
SD_CARD
BOARD_VERSION
PL_User_IO
PL_PS_Dual_UART
EEPROM_UID
PL_WR_DACS
PLL_CTRL
BULLS_EYE
WR_CLOCKS
10MHZ_CLK
TIMING_SIGNALS
PL_SI57X
PL_SFP

ZYNQ XC7 (Z030) Z035 (Z045) FBG676

Sheet 2

PL_JTAG
ZYNQ_JTAG
Force_PS_POR
RESET_CONFIG
FPGA_CONFIG
PL_DDR
PS_DDR
PL_FMC
PS_RGMII
PL_PCIe_2x
PG_VCCINT

SPEC7_Power_System
Sheet 30

EN_5V
PGOOD

SPEC7_Mechanical_Parts
Sheet 35

FMC_JTAG
ZYNQ_JTAG
PL_JTAG
Force_PS_POR
RESET_CONFIG
FPGA_CONFIG
PL_DDR
PS_DDR
PL_FMC
PRSNT_M2C_L
PG_C2M
R325
0
PS_RGMII
PL_PCIe_2x

SPEC7_Resets
Sheet 27

Force_PS_POR
RESET_CONFIG
FPGA_CONFIG
PL_PCIe_2x
PGOOD

RESET PROG DONE

PL_DDR3 Programmable Logic
Sheet 13

PL_DDR

RAM

PS_DDR3 Processor System
Sheet 12

PS_DDR

RAM

PL_FMC_Connector
Sheet 17

FMC_JTAG
PL_FMC

PS_Phy_CopperEthernet
Sheet 15

PS_RGMII

PL_PCIe_12x_Edge_Con
Sheet 14

PCIe_2x

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Project : WRITE
Sheetname : Top

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Sheet 1 of 35 A3
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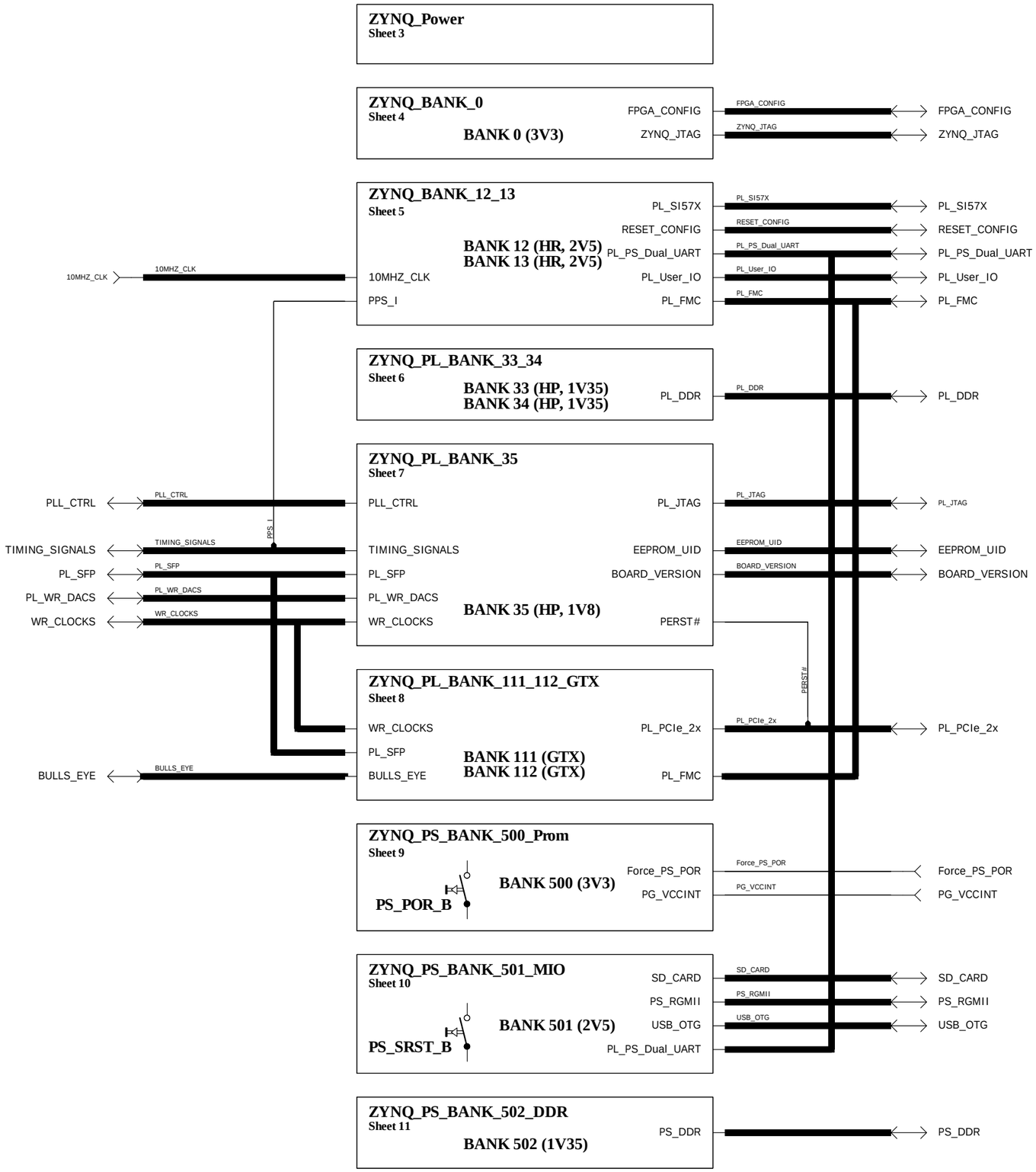

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Sheet 2 of 35 A3

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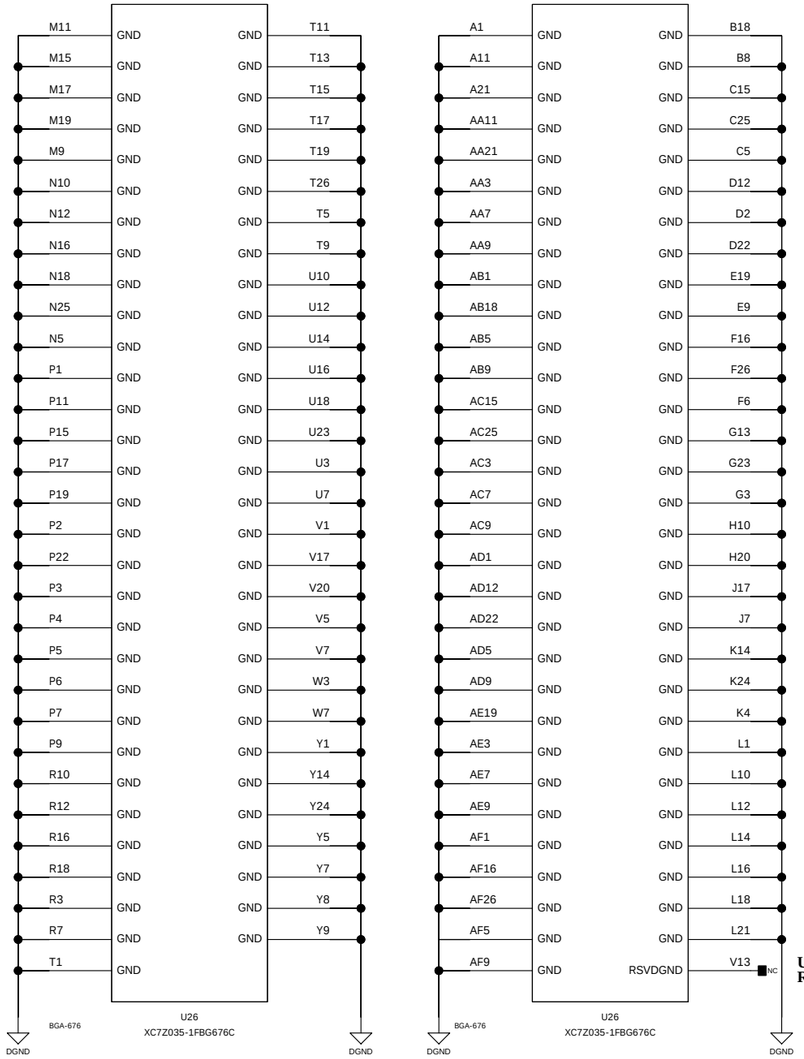
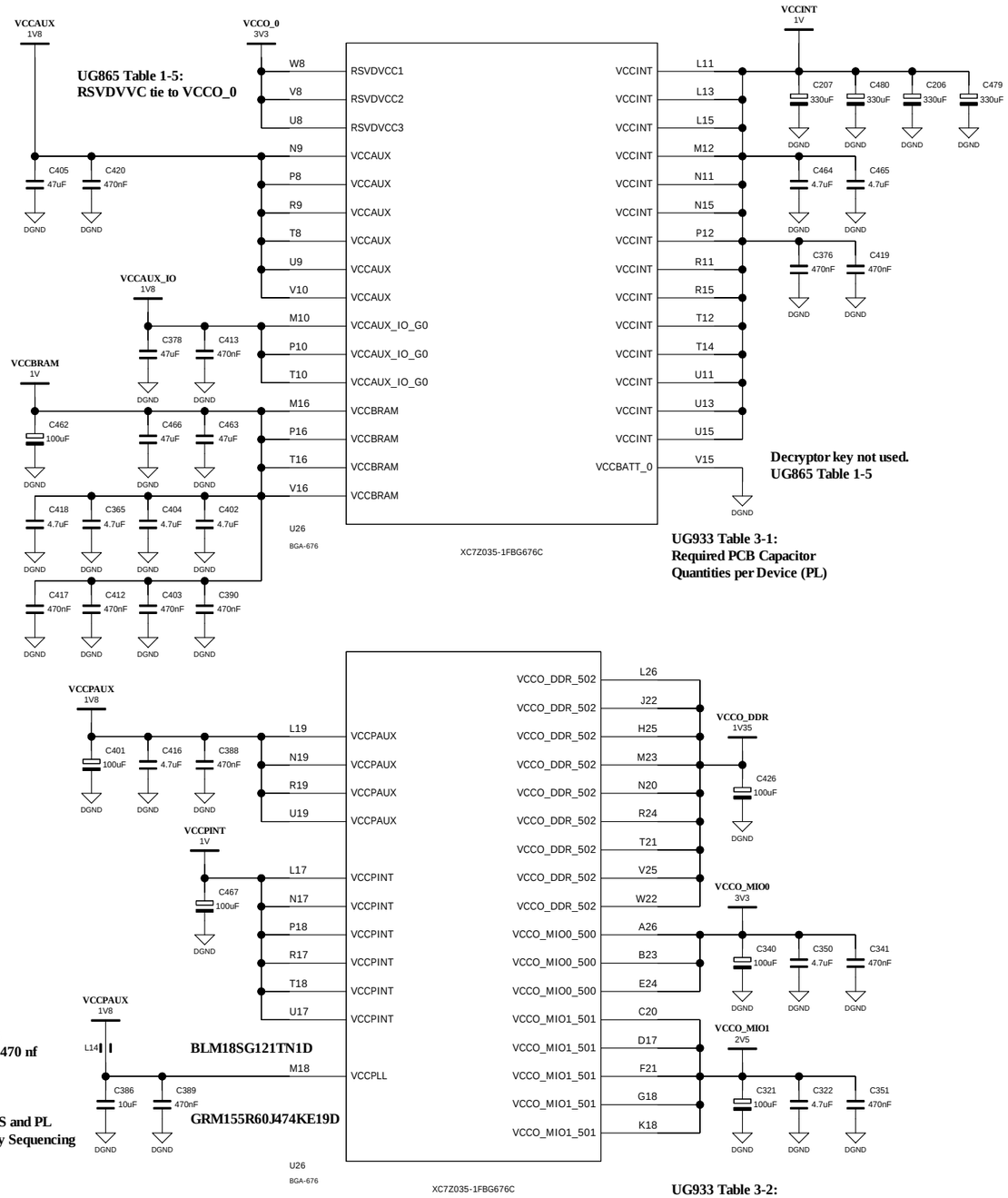


UG865 Table 1-5:
RSVDGND do not connect

Layout recommendation
see UG933 figure 5-2 & 5-3
Note recommended part for 470 nf and ferrite bead!

VCCPLL See also DS191 PS and PL Power-On/Off Power Supply Sequencing



UG933 Table 3-2:
Required PCB Capacitor
Quantities per Device (PS)

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Sheetname : ZYNQ_Power

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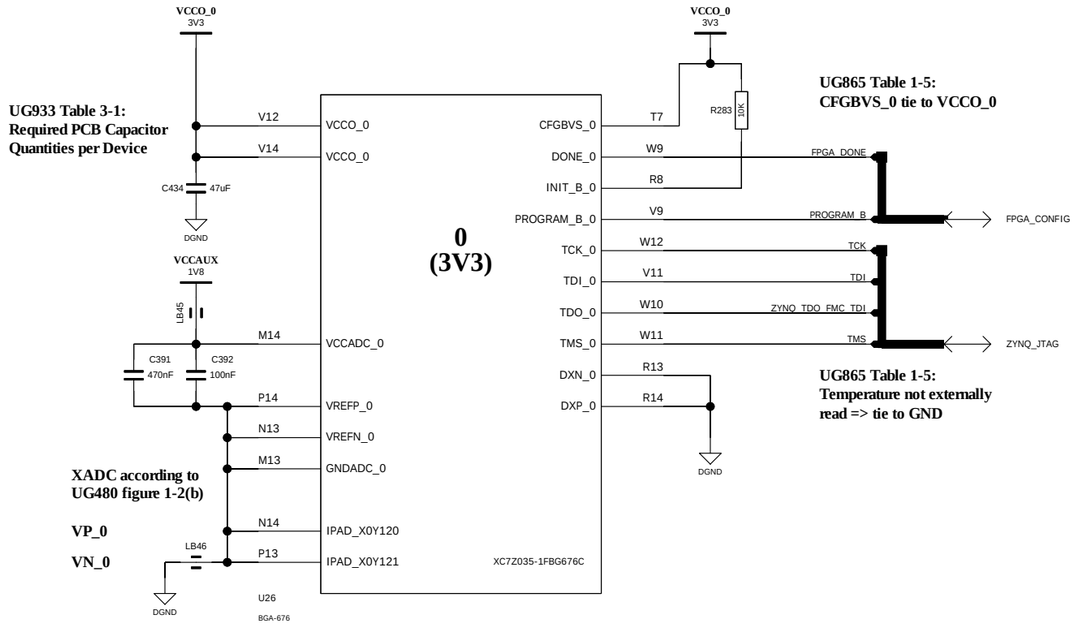
Sheet: 3 of 35 A3
Date: 2020-01-31



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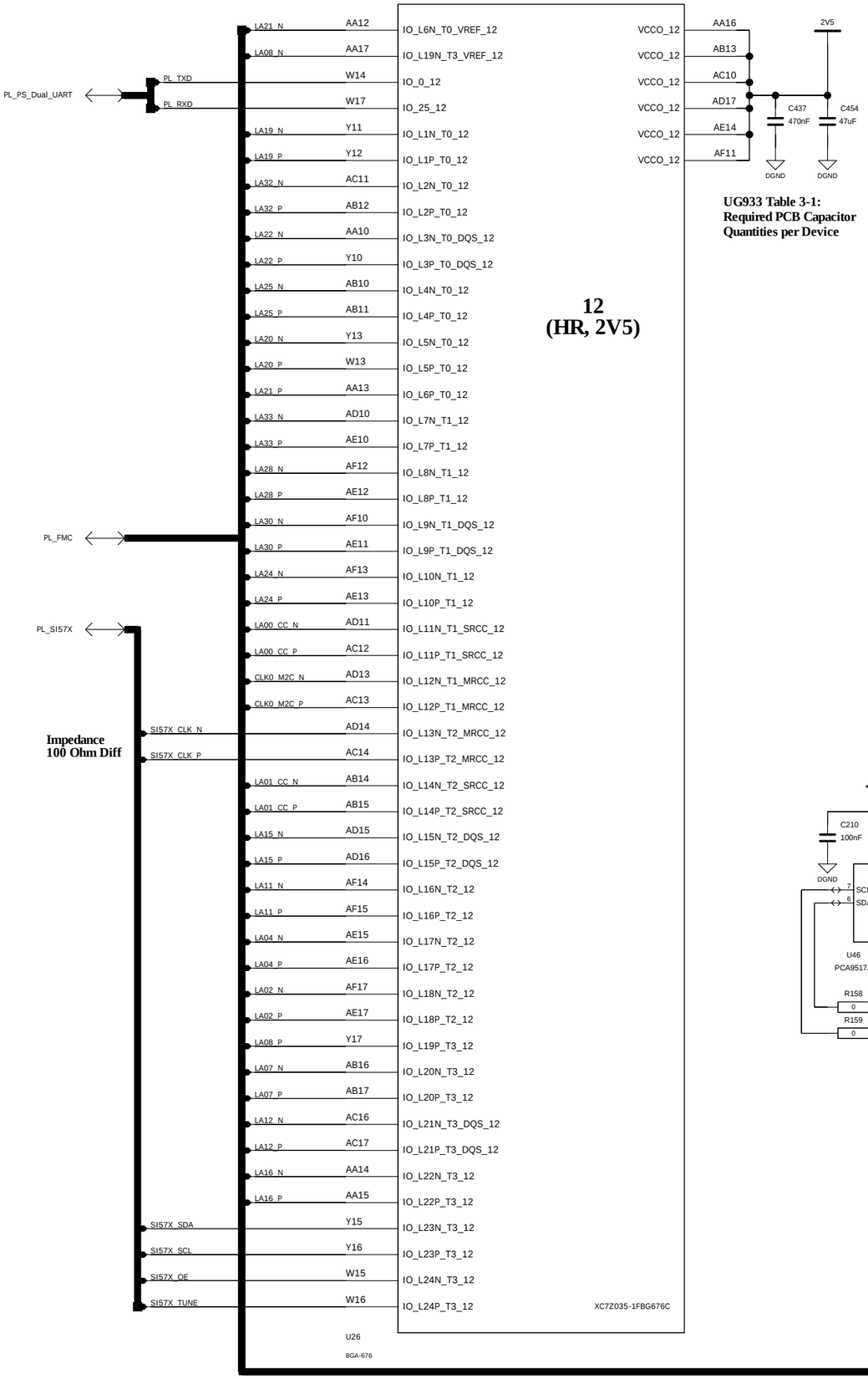
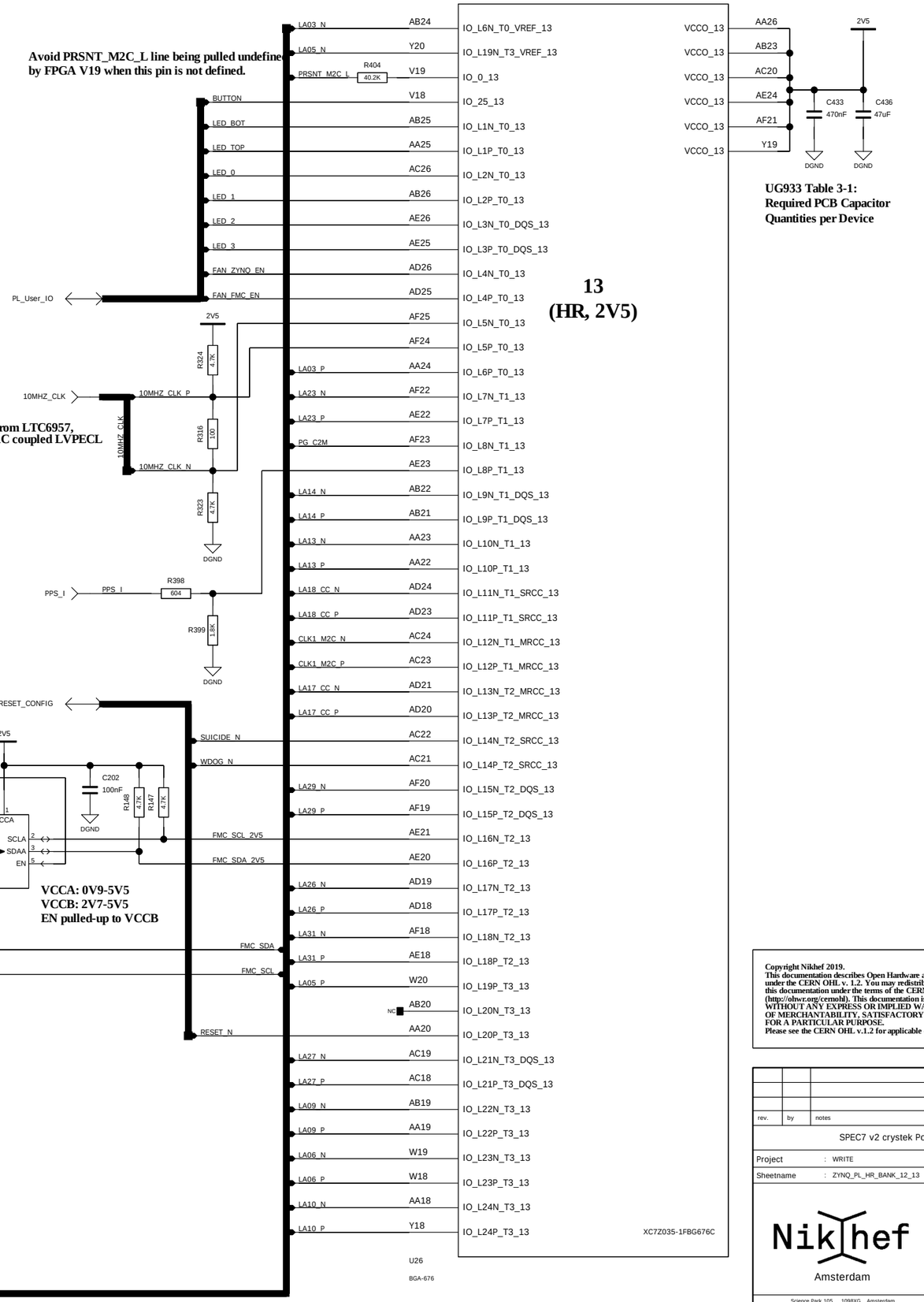
Date 2020-01-31





rev.	by	notes

SPEC7 v2 crystek Powered

Project : WRITE

Sheetname : ZYNQ_PL_HR_BANK_12_13

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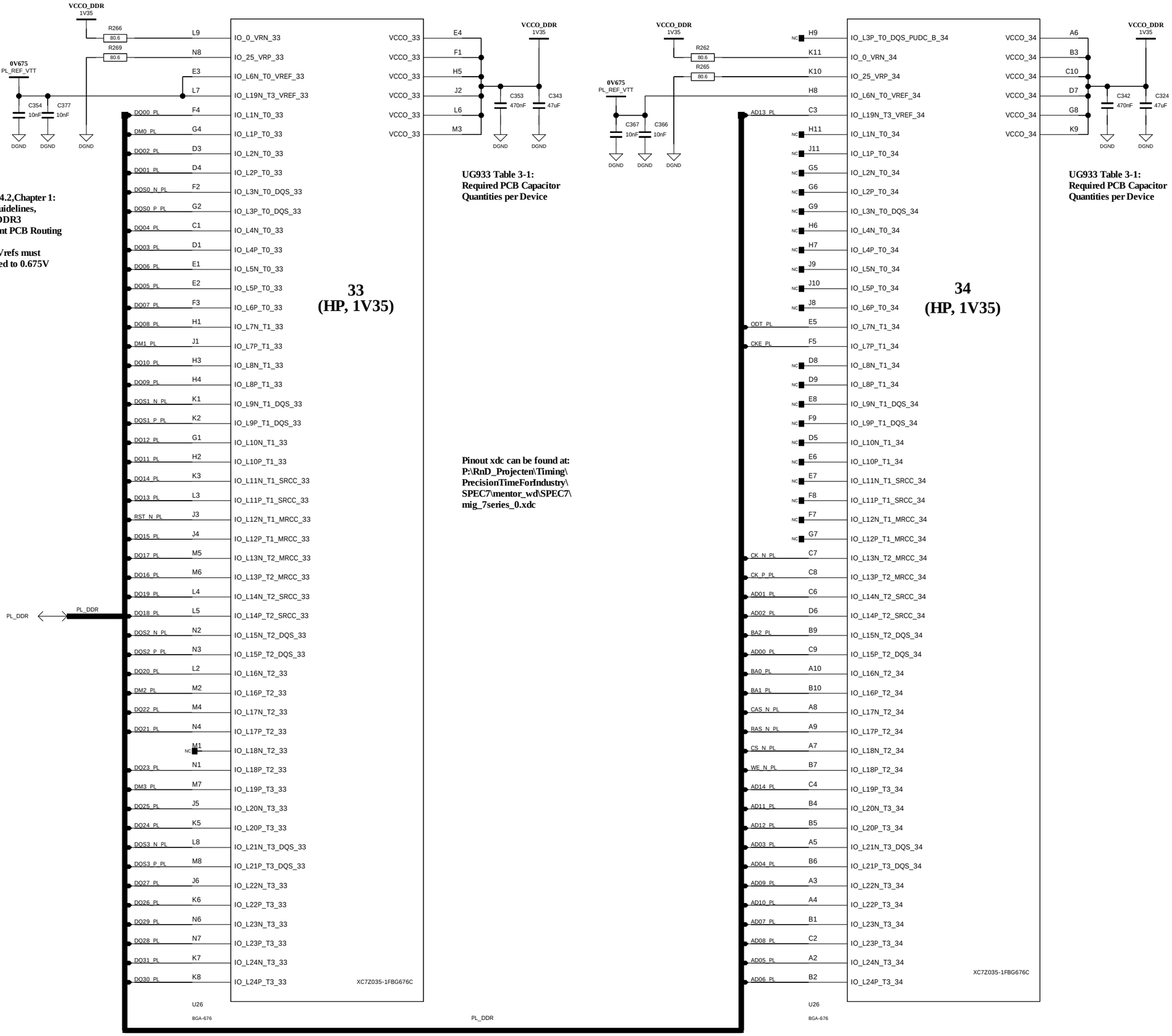
Sheet 5 of 35 A3

Date 2020-01-31


VCCO_DDR
1V35
R266
80.6
R269
80.6
0V675
PL_REF_VTT
C354
10nF
C377
10nF
DGND
L9
N8
E3
L7
IO_0_VRN_33
IO_25_VRP_33
IO_L6N_T0_VREF_33
IO_L19N_T3_VREF_33
DQ00_PL
DM0_PL
DQ02_PL
DQ01_PL
DQS0_N_PL
DQS0_P_PL
DQ04_PL
DQ03_PL
DQ06_PL
DQ05_PL
DQ07_PL
DQ08_PL
DM1_PL
DQ10_PL
DQ09_PL
DQS1_N_PL
DQS1_P_PL
DQ12_PL
DQ11_PL
DQ14_PL
DQ13_PL
RST_N_PL
DQ15_PL
DQ17_PL
DQ16_PL
DQ19_PL
DQ18_PL
DQS2_N_PL
DQS2_P_PL
DQ20_PL
DM2_PL
DQ22_PL
DQ21_PL
DQ23_PL
DM3_PL
DQ25_PL
DQ24_PL
DQS3_N_PL
DQS3_P_PL
DQ27_PL
DQ26_PL
DQ29_PL
DQ28_PL
DQ31_PL
DQ30_PL
F4
G4
D3
D4
F2
G2
C1
D1
E1
E2
F3
H1
J1
H3
H4
K1
K2
G1
H2
K3
L3
J3
J4
M5
M6
L4
L5
N2
N3
L2
M2
M4
N4
M1
N1
M7
J5
K5
L8
M8
J6
K6
N6
N7
K7
K8
IO_L1N_T0_33
IO_L1P_T0_33
IO_L2N_T0_33
IO_L2P_T0_33
IO_L3N_T0_DQS_33
IO_L3P_T0_DQS_33
IO_L4N_T0_33
IO_L4P_T0_33
IO_L5N_T0_33
IO_L5P_T0_33
IO_L6P_T0_33
IO_L7N_T1_33
IO_L7P_T1_33
IO_L8N_T1_33
IO_L8P_T1_33
IO_L9N_T1_DQS_33
IO_L9P_T1_DQS_33
IO_L10N_T1_33
IO_L10P_T1_33
IO_L11N_T1_SRCC_33
IO_L11P_T1_SRCC_33
IO_L12N_T1_MRCC_33
IO_L12P_T1_MRCC_33
IO_L13N_T2_MRCC_33
IO_L13P_T2_MRCC_33
IO_L14N_T2_SRCC_33
IO_L14P_T2_SRCC_33
IO_L15N_T2_DQS_33
IO_L15P_T2_DQS_33
IO_L16N_T2_33
IO_L16P_T2_33
IO_L17N_T2_33
IO_L17P_T2_33
IO_L18N_T2_33
IO_L18P_T2_33
IO_L19P_T3_33
IO_L20N_T3_33
IO_L20P_T3_33
IO_L21N_T3_DQS_33
IO_L21P_T3_DQS_33
IO_L22N_T3_33
IO_L22P_T3_33
IO_L23N_T3_33
IO_L23P_T3_33
IO_L24N_T3_33
IO_L24P_T3_33
33
(HP, 1V35)
XC7Z035-1FBG676C
U26
BGA-676
PL_DDR
PL_DDR
VCCO_33
E4
F1
H5
J2
L6
M3
C353
470nF
C343
47uF
UG933 Table 3-1:
Required PCB Capacitor
Quantities per Device
UG586 V4.2,Chapter 1:
Design Guidelines,
Section: DDR3
Component PCB Routing
Page 195
External Vrefs must
be conected to 0.675V
Pinout xdc can be found at:
P:\RnD_Projecten\Timing\
PrecisionTimeForIndustry\
SPEC7\mentor_wd\SPEC7\
mig_7series_0.xdc
R262
80.6
R265
80.6
C367
10nF
C366
10nF
NC
H9
K11
K10
H8
C3
H11
J11
G5
G6
G9
H6
H7
J9
J10
J8
E5
F5
D8
D9
E8
F9
D5
E6
E7
F8
F7
G7
C7
C8
C6
D6
B9
C9
A10
B10
A8
A9
A7
B7
C4
B4
B5
A5
B6
A3
A4
B1
C2
A2
B2
ODT_PL
CKE_PL
CK_N_PL
CK_P_PL
AD01_PL
AD02_PL
BA2_PL
AD00_PL
BA0_PL
BA1_PL
CAS_N_PL
RAS_N_PL
CS_N_PL
WE_N_PL
AD14_PL
AD11_PL
AD12_PL
AD03_PL
AD04_PL
AD09_PL
AD10_PL
AD07_PL
AD08_PL
AD05_PL
AD06_PL
IO_L3P_T0_DQS_PUDC_B_34
IO_0_VRN_34
IO_25_VRP_34
IO_L6N_T0_VREF_34
IO_L19N_T3_VREF_34
IO_L1N_T0_34
IO_L1P_T0_34
IO_L2N_T0_34
IO_L2P_T0_34
IO_L3N_T0_DQS_34
IO_L4N_T0_34
IO_L4P_T0_34
IO_L5N_T0_34
IO_L5P_T0_34
IO_L6P_T0_34
IO_L7N_T1_34
IO_L7P_T1_34
IO_L8N_T1_34
IO_L8P_T1_34
IO_L9N_T1_DQS_34
IO_L9P_T1_DQS_34
IO_L10N_T1_34
IO_L10P_T1_34
IO_L11N_T1_SRCC_34
IO_L11P_T1_SRCC_34
IO_L12N_T1_MRCC_34
IO_L12P_T1_MRCC_34
IO_L13N_T2_MRCC_34
IO_L13P_T2_MRCC_34
IO_L14N_T2_SRCC_34
IO_L14P_T2_SRCC_34
IO_L15N_T2_DQS_34
IO_L15P_T2_DQS_34
IO_L16N_T2_34
IO_L16P_T2_34
IO_L17N_T2_34
IO_L17P_T2_34
IO_L18N_T2_34
IO_L18P_T2_34
IO_L19P_T3_34
IO_L20N_T3_34
IO_L20P_T3_34
IO_L21N_T3_DQS_34
IO_L21P_T3_DQS_34
IO_L22N_T3_34
IO_L22P_T3_34
IO_L23N_T3_34
IO_L23P_T3_34
IO_L24N_T3_34
IO_L24P_T3_34
34
(HP, 1V35)
XC7Z035-1FBG676C
U26
BGA-676
VCCO_34
A6
B3
C10
D7
G8
K9
C342
470nF
C324
47uF
UG933 Table 3-1:
Required PCB Capacitor
Quantities per Device
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by
notes
SPEC7 v2 crystek Powered
Project : WRITE
Sheetname : ZYNQ_PL_BANK_33_34_DDR
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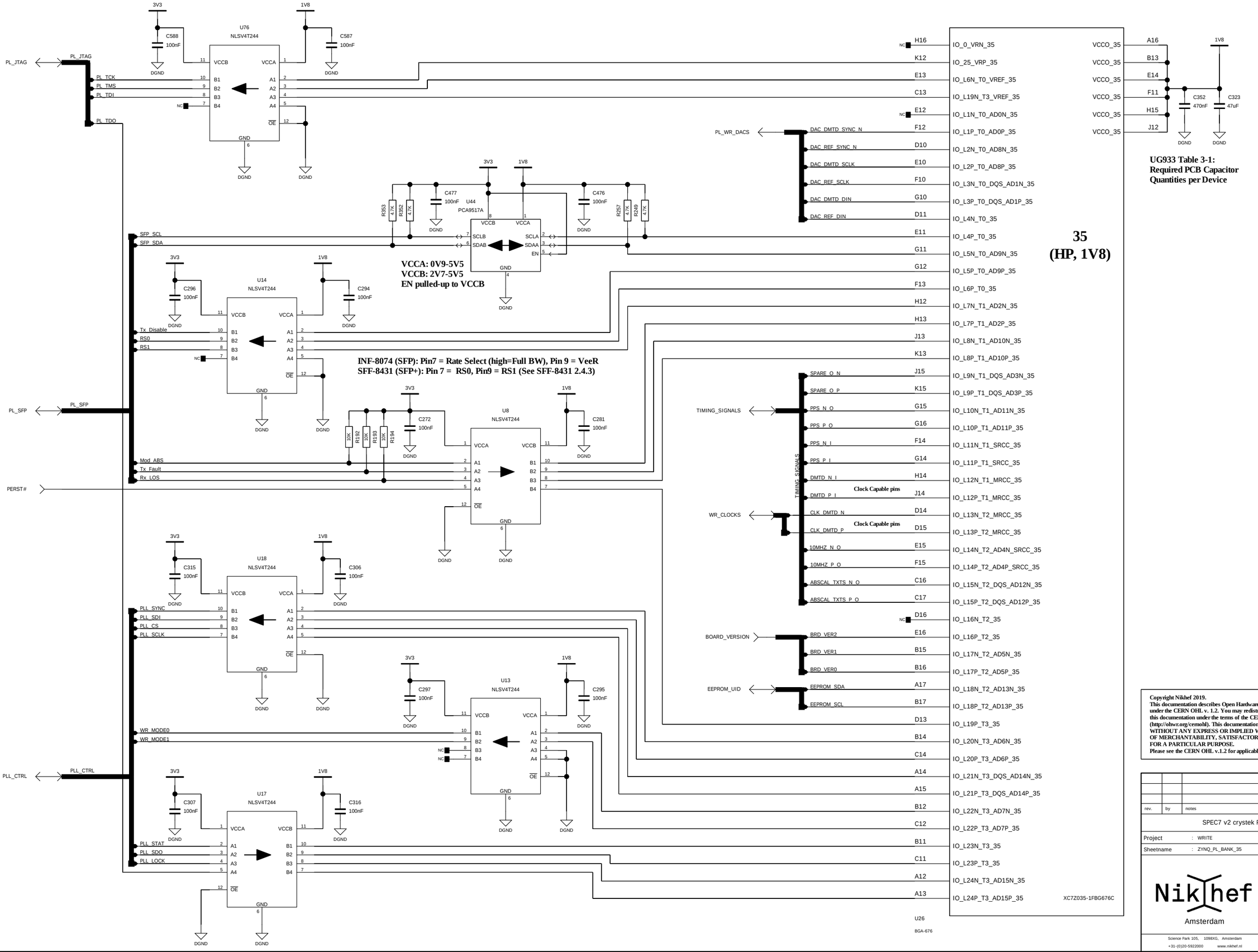
Sheet 6 of 35
A3
Date 2020-01-31



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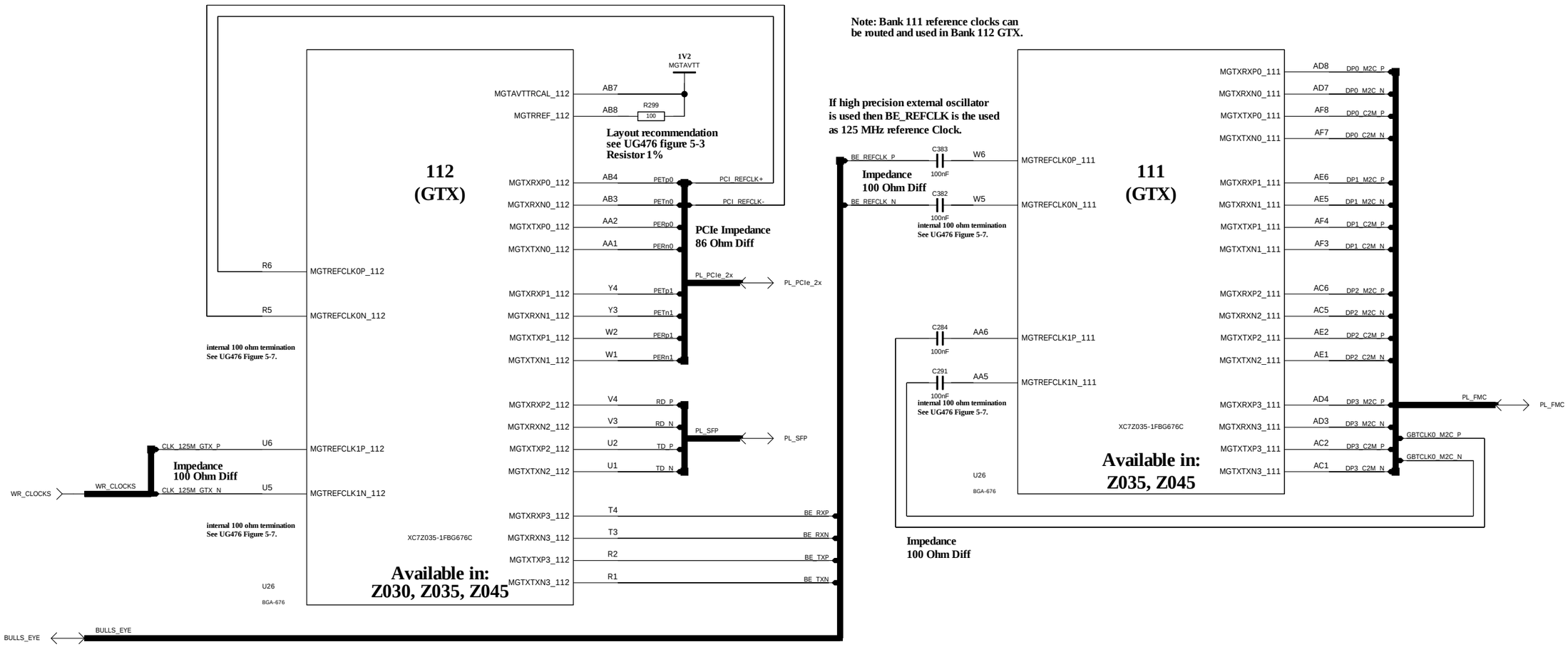
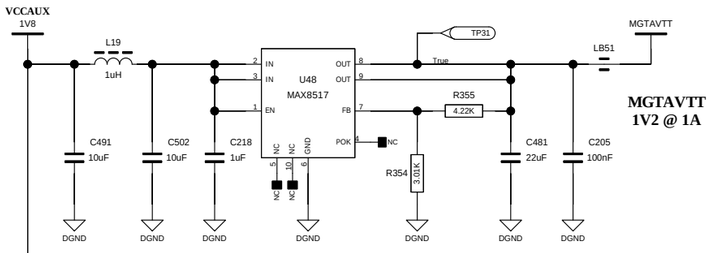
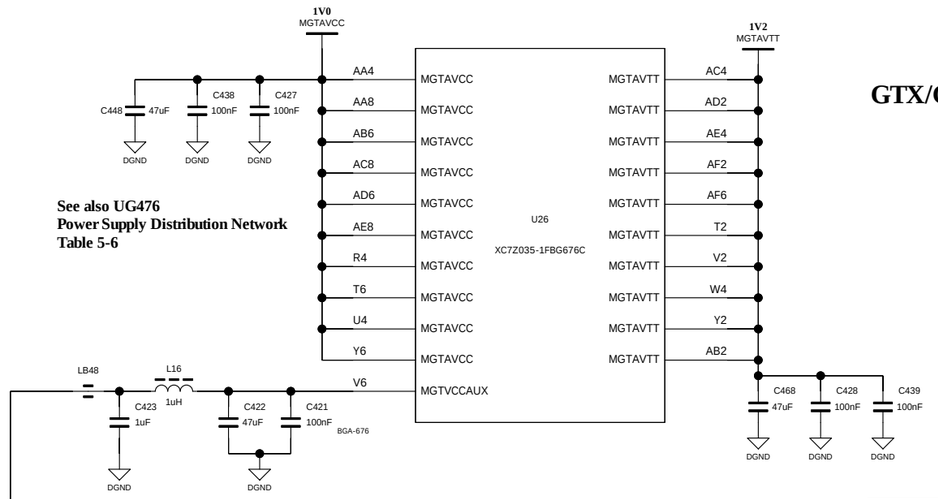
Sheet 7 of 35 A3

Date 2020-01-31







See also UG476
Power Supply Distribution Network
Table 5-6

General GTX remark:
See also UG476 Table 5-7
GTX/GTH Transceiver PCB Design Checklist

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Sheet: 8 of 35 A3

Date: 2020-01-31

UG585, Table 6-4
MIO[5:3] Boot Device Select

DIP switch:
"1234"
"X000" => JTAG Boot Mode
"X001" => NOR Boot
"X010" => NAND
"X100" => Quad-SPI
"X110" => SD Card

UG933 MIO[8:2] Boot Mode Pins
(Avoid "resistor tree")

PS_CLK only runs when VCCINT signals PowerGood
See DS191 "PS Power-On/Off Power Supply Sequencing"
=> eFUSE integrity.

When VCCINT is okay then G1 is not yet powered.
R405 prevents PG_VCCINT from being kept low
by the ESD diode on G1 pin 1.

PS_POR_B See also DS191 PS and PL
Power-On/Off Power Supply Sequencing

Suffix 31 = Reset
threshold 3.08V
Csrt=22nF => 60 ms.

DNP
2x 1MEG

UG585, Table 6-4 MIO[8:2]

MIO[2] JTAG Chain Routing "0" => Cascade Mode

MIO[5:3] Boot Device Select "100" => Quad-SPI

MIO[6] PLL Bypass "0" => Use PLLs

MIO[8:7] = VMODE "00" => 2V5, 3V3

QSPI0

QSPI1

Dual QUAD SPI

500
(3V3)

General: See UG585 Table 2-4 for
MIO signal assignment

UG933 IIC recommends external glitch filter.
Ferrites added on MIO[14:15]
See also: http://www.ti.com/lit/an/slea053/slea053.pdf)

ARM MAC Address
(Unique 48-bit ID)
I2C ADDR = 1010.000x

Notes on PS_POR_B

UG585 Par. 6.1
Immediately after the PS_POR_B reset pin deasserts, the hardware samples the boot strap pins and optionally enables the PS clock PLLs. Then, the PS begins executing the BootROM code in the on-chip ROM to boot the system.

UG585 Par. 6.2.4. "External Reset Signal Pins" eFUSE integrity uPC supervisory circuit ensures that PS_POR_B assrted low before VCCINT reaches 0.80V.

UG 585 Par. 6.3.3 PS_POR_B De-assertion Guidlines. De-assertion of PS_POR_B occurs 60 ms after PL power Supply. See also AR# 63149 PS_POR_B timing window calculator.

AR# 52016
MIO pin 0 must be Low during the SDIO boot process.

Notes on QPI Flash

UG585 Paragraph 6.1
"Optionally, the FSBL/User code can be executed directly from a Quad-SPI or NOR device in a non-secure environment."

3V3 Quad-SPI NOR Flash Memory
64MB (512 Mb) reserved,
32MB (256 Mb) supported
(See DS190, Table 6).

For bitfile sizes, see: Table 21-2, UG585.
Z035, Z045 sizes are 106.571.232 bit
=> 256Mbit Flash can hold two images.

See also AR# 50991 for a list of Xilinx Suppoted Devices.

VCC_MIO0 = 3V3
Note that Micron has 1V8 or 3V3 Flash (no 2V5)

rev.	by	notes

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Sheetname : ZYNQ_PS_BANK_500_Prom

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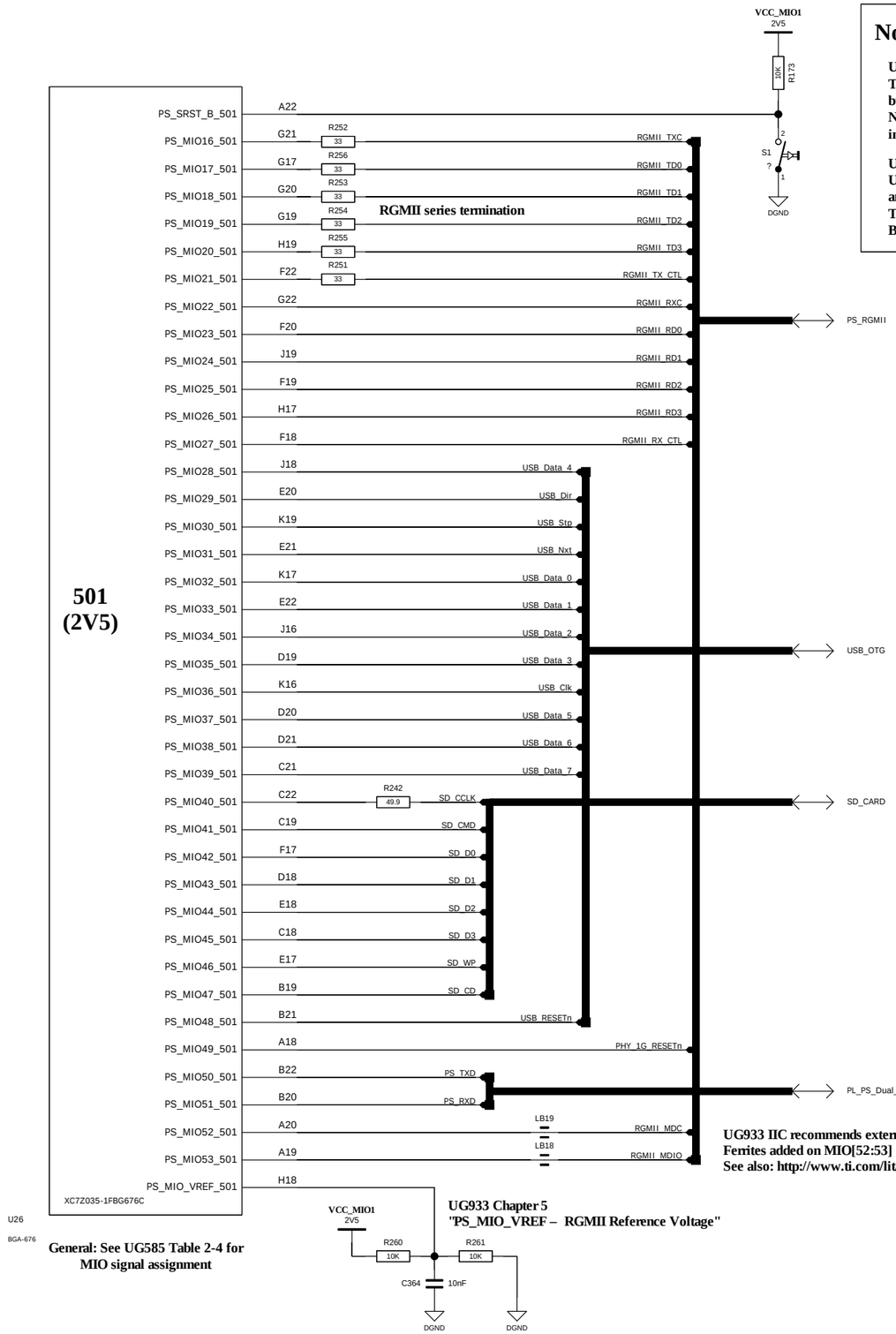
Size: 420 x 297mm
Sheet: 9 of 35 A3
Date: 2020-01-31



Notes on PS_SRTS_B

UG585 Par. 6.1
The non-POR type resets also cause the BootROM to execute, but without the hardware sampling the strap pins.
Non-POR resets include the PS_SRST_B pin and several internal reset sources.

UG585 Par. 6.2.4. "External Reset Signal Pins"
Used to force a system reset. It can be tied or pulled High, and can be High during the PS power supply ramp-up.
The PS_SRST_B signal must not be asserted while the BootROM is executing from a POR reset

Notes on SD Card

PCB Design Guide
UG933, Par. SDIO

UG585, SD Card Boot
Table 6-15 MIO[40:45]

UG585 Chapter 6.3.7:
"In SD card boot mode, the BootROM does not perform a header search and does not support multiboot."

UG585 Par. 13.3.7 (figure 13-8)
card detect (CD) and write protect (WP)

UG933 IIC recommends external glitch filter.
Ferrites added on MIO[52:53]
See also: http://www.ti.com/lit/an/slea053/slea053.pdf)

General: See UG585 Table 2-4 for MIO signal assignment

UG933 Chapter 5
"PS_MIO_VREF – RGMII Reference Voltage"

rev.	by	notes

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Project : WRITE
Sheetname : ZYNQ_PS_BANK_501_MIO

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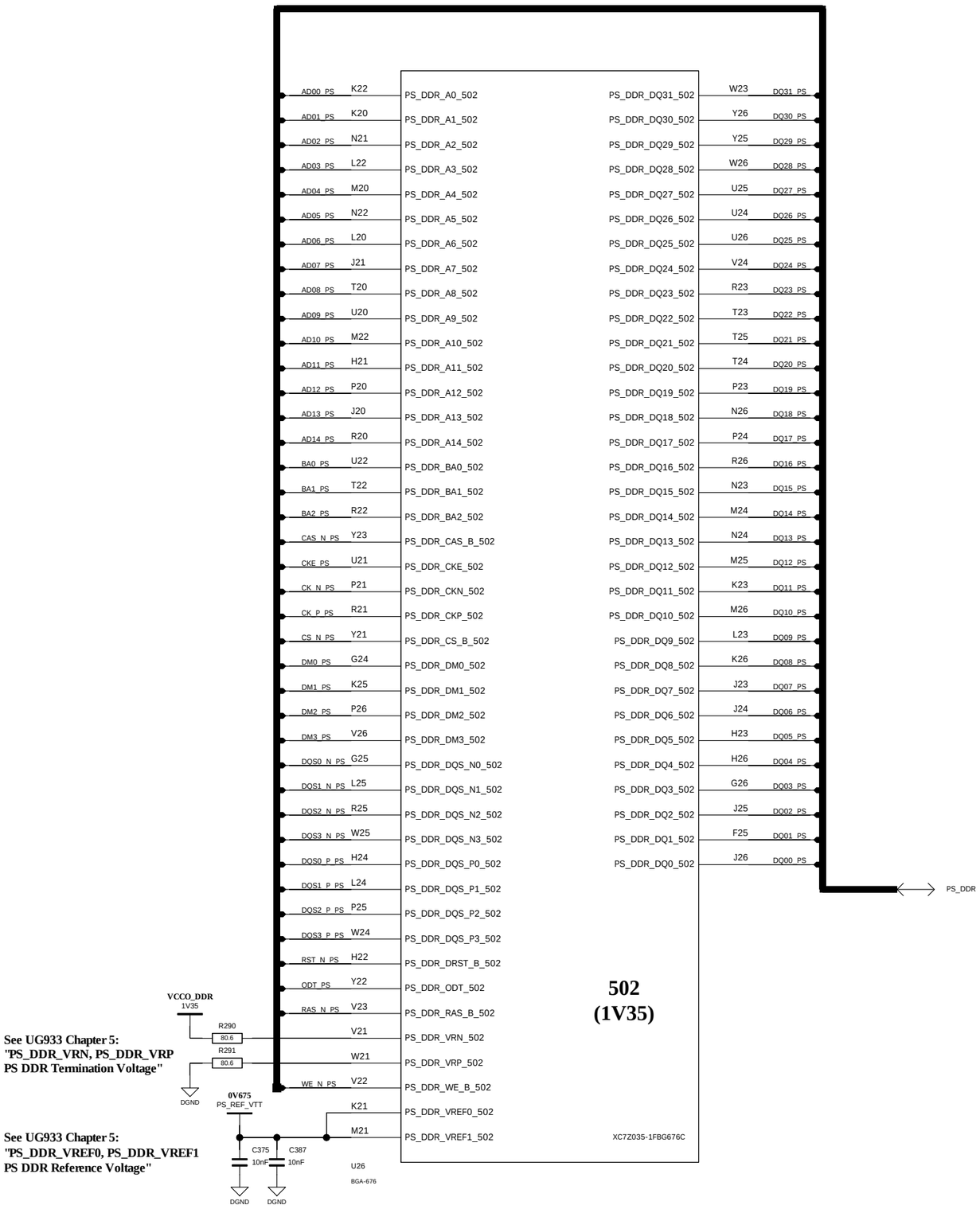
Size 420 x 297mm
Sheet 10 of 35 A3
Date 2020-01-31



rev.	by	notes

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Project : WRITE

Sheetname : ZYNQ_PS_BANK_502_DDR

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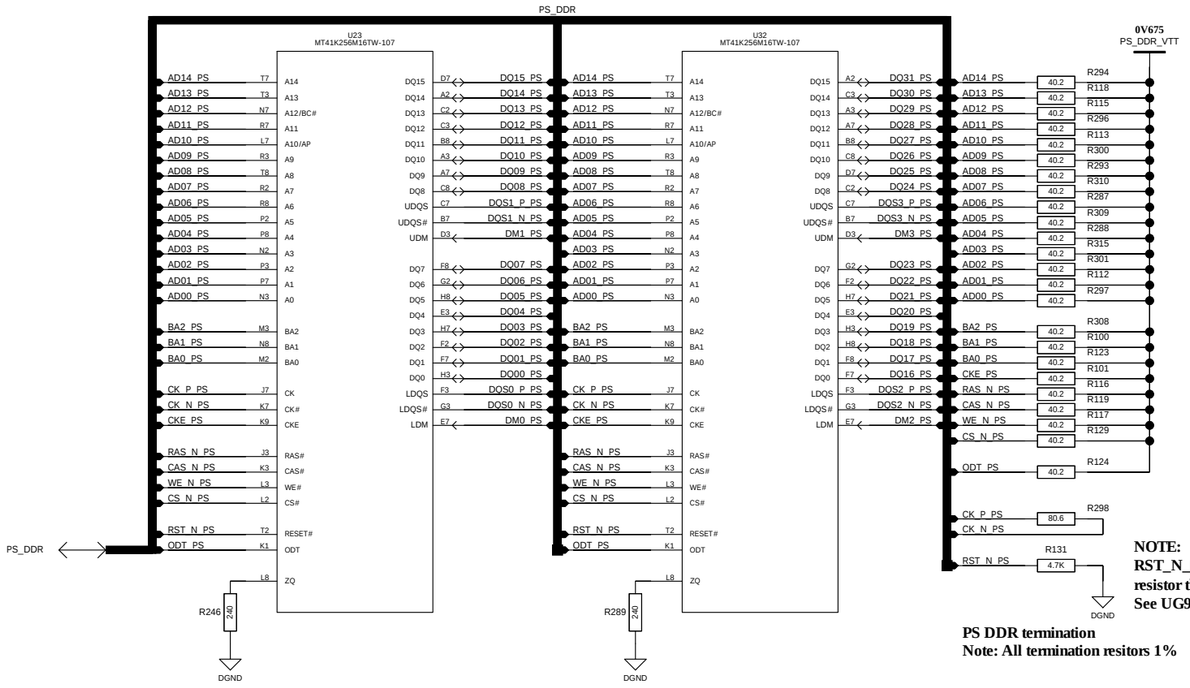
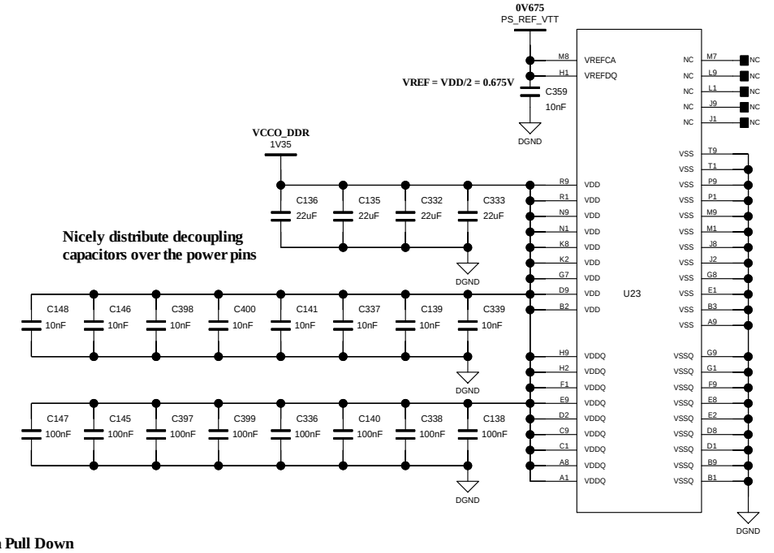
Sheet 11 of 35 A3

Date 2020-01-31



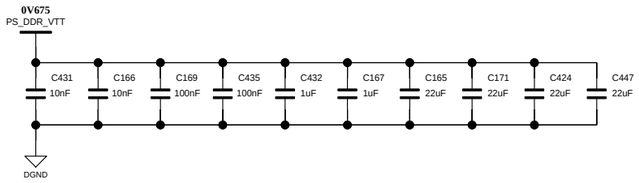
PS DDR termination
Note: All termination resitors 1%

NOTE:
RST_N_PL requires a Pull Down resistor through FPGA Configuration.
See UG93 Chapter 5 "DDR Termination"

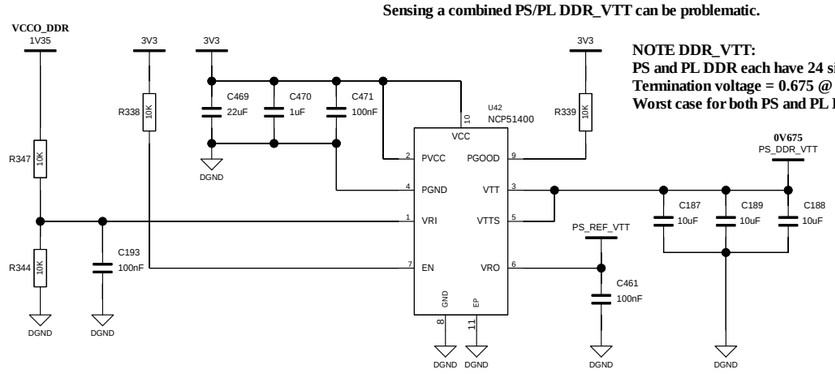


Worst Case IDD per DDR device = 274 mA
(datasheet Tabe 20, Idd7)

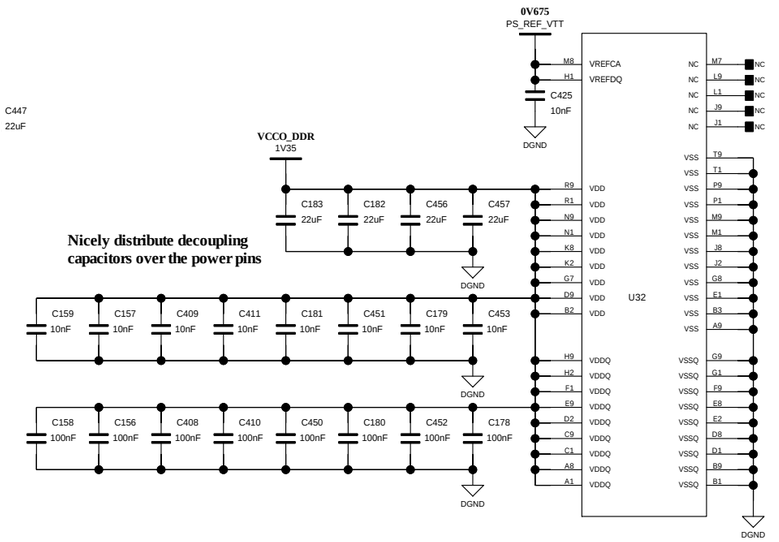
DDR PCB layout
See also UG933 Chapter 5.



Separate DDR_VTT for PS
Note: Sense input VTTS needs to be connected to remote DDR termination bypass capacitors (see datasheet NCP51400).
Sensing a combined PS/PL DDR_VTT can be problematic.



NOTE DDR_VTT:
PS and PL DDR each have 24 signals to terminate.
Termination voltage = 0.675 @ 40.2 ohm = 16.8 mA per signal
Worst case for both PS and PL DDR: 2*24*16.8 mA = 806 mA



rev.	by	notes

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Project	:	WRITE
Sheetname	:	PS_DDR

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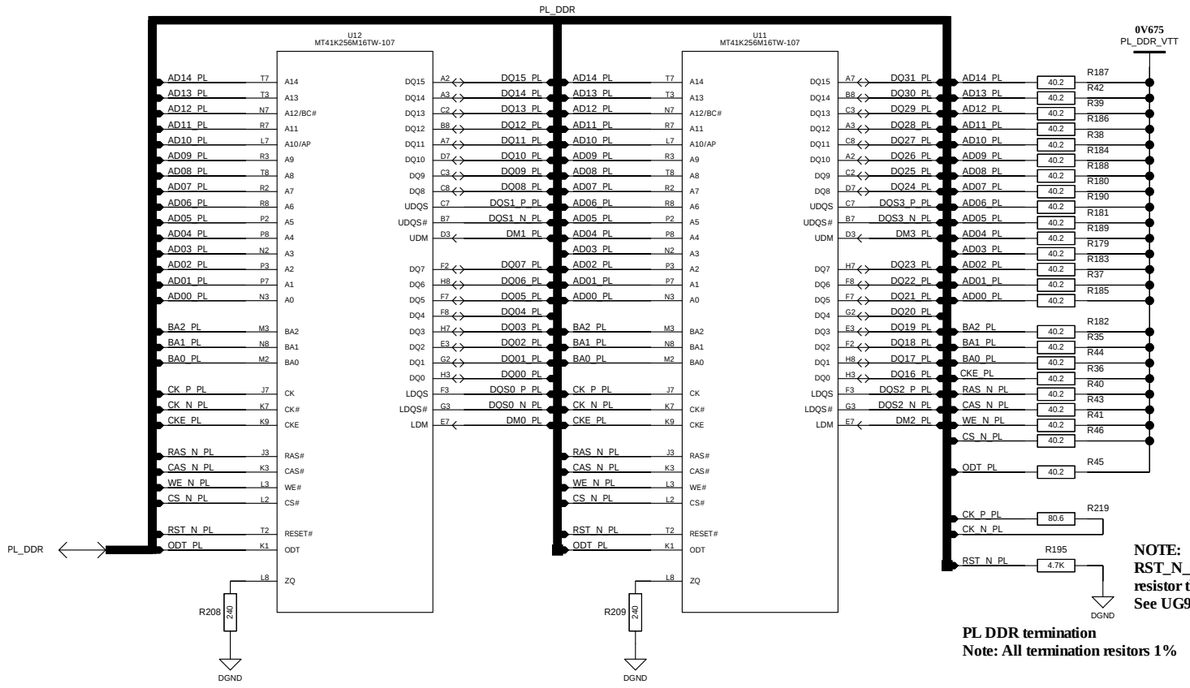
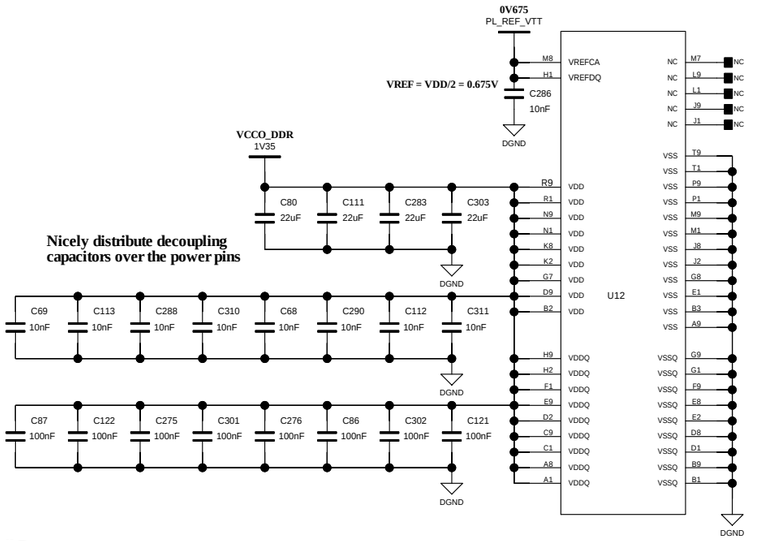


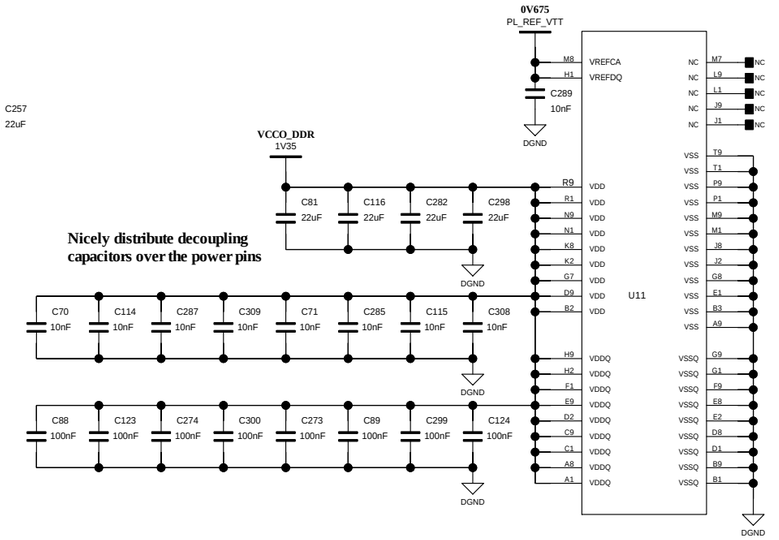
PL DDR termination
Note: All termination resitors 1%

NOTE:
RST_N_PL requires a Pull Down resistor through FPGA Configuration.
See UG93 Chapter 5 "DDR Termination"

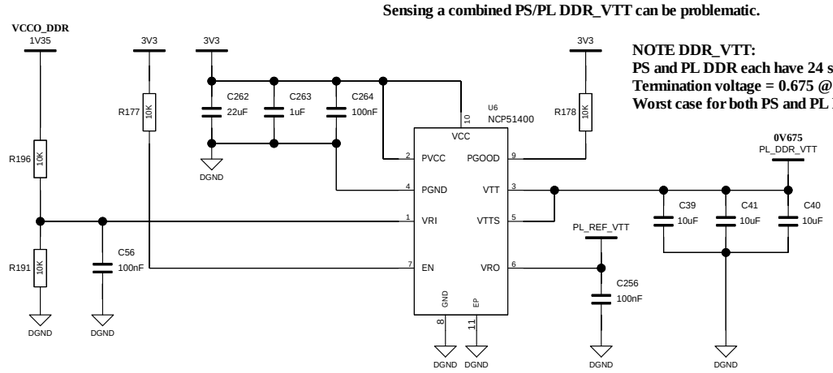


Worst Case IDD per DDR device = 274 mA
(datasheet Tabe 20, Idd7)

DDR PCB layout
See also UG933 Chapter 5.



Separate DDR_VTT for PL
Note: Sense input VTTS needs to be connected to remote DDR termination bypass capacitors (see datasheet NCP51400).
Sensing a combined PS/PL DDR_VTT can be problematic.



NOTE DDR_VTT:
PS and PL DDR each have 24 signals to terminate.
Termination voltage = 0.675 @ 40.2 ohm = 16.8 mA per signal
Worst case for both PS and PL DDR: 2*24*16.8 mA = 806 mA

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Project	:	WRITE
Sheetname	:	PL_DDR

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Notes

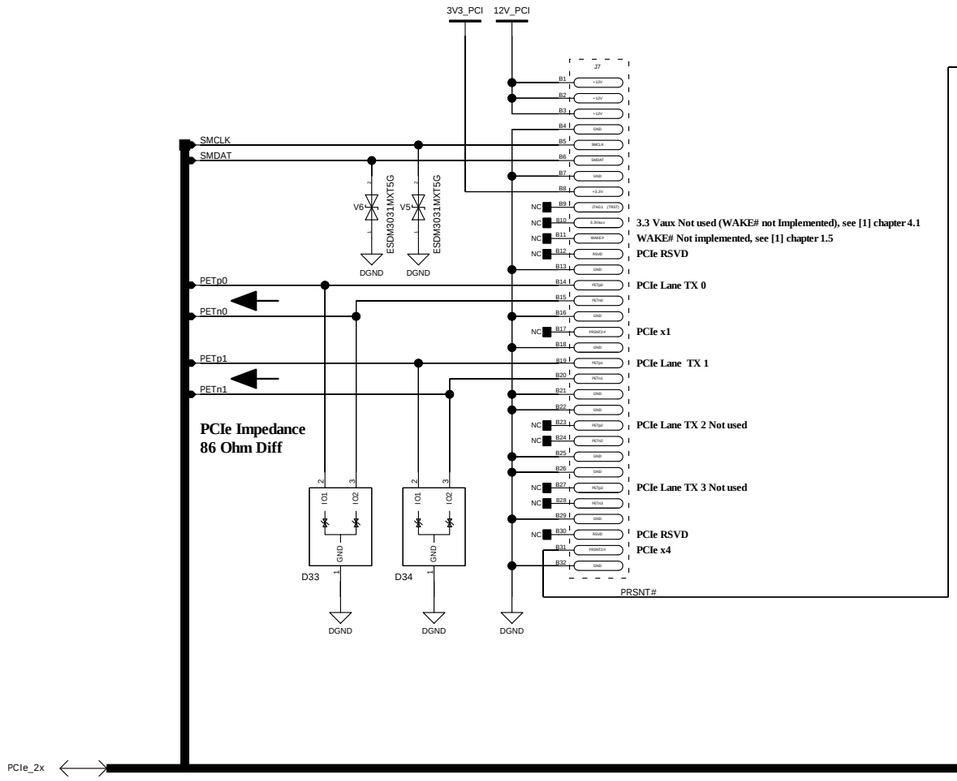
PCI_REFCLK PCIe 100MHz or 250 Mhz
PERpX/PERnX PCIe RX Datalane (Card 2 Motherboard, see 5.1 notes of referencce [1])
PETpX/PETnX PCIe TX Datalane (Motherboard 2 Card, see 5.1 notes of referencce [1])
12V_PCI: 25W Slot (2.1A max, [1] Table 4-1)
3V3_PCI: 25W Slot (3A max, [1] Table 4-1)

Precense detect, see [1] chapter 3.2
"PRSNT1# signal to the farthest-apart PRSNT2# signal with a single trace".
=> i.e. PCIe x4
PCIe x2 is possible see [1] chapter 6.3 "All PCI Express add-in cards must be able to negotiate and operate in all smaller Link widths from the full Link width down to x1. The x2 and x12 Link widths are optional."

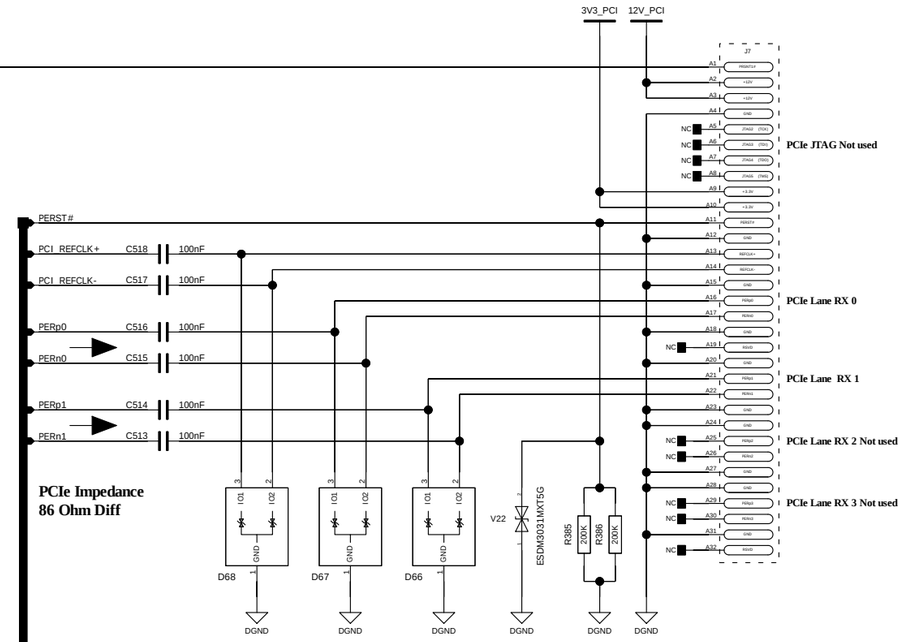
AC Coupling Capacitors (See 4.6.1 of reference [1])
Differential Data Trace Impedance 68-105 ohm (See 4.6.8. of reference [1])
Differential Data Trace Propagation Delay must not exceed 750 ps (See 4.6.9. of reference [1])
PCI connector mechanical dimensions see figure 5.3 of reference [1]
i.e. PCB thickness @ connector 1.57 [0.062]
PCI connector 30 u-inches Gold plating over 50 u-inches of nickel
(see 5.4.1 Environmental Requirements of reference [1])

[1] PCI Express Card Electromechanical Specification Revision 2.0

B Side edge connector



A Side edge connector



PERST# 100 K Pull Down, see also:
https://ohwr.org/project/spec/issues/17

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Project : WRITE
Sheetname : PL_PCIe_2x_Edge_Con

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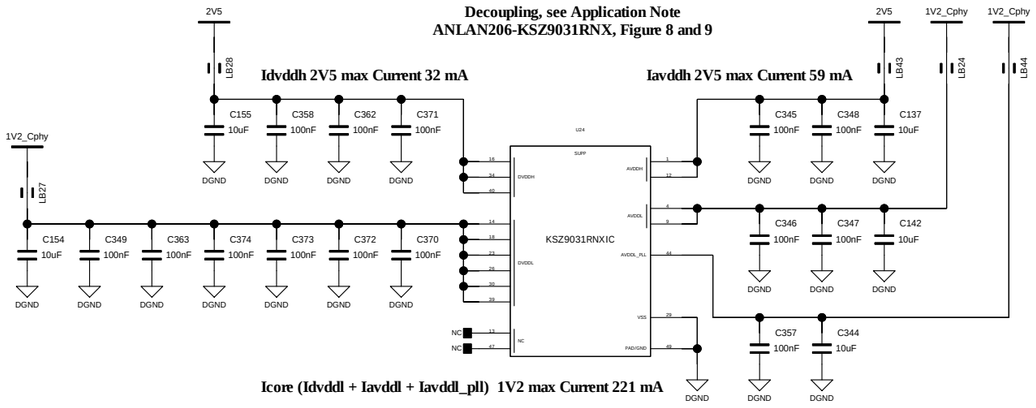
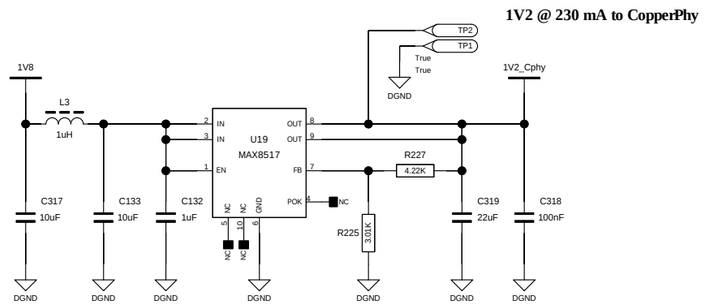
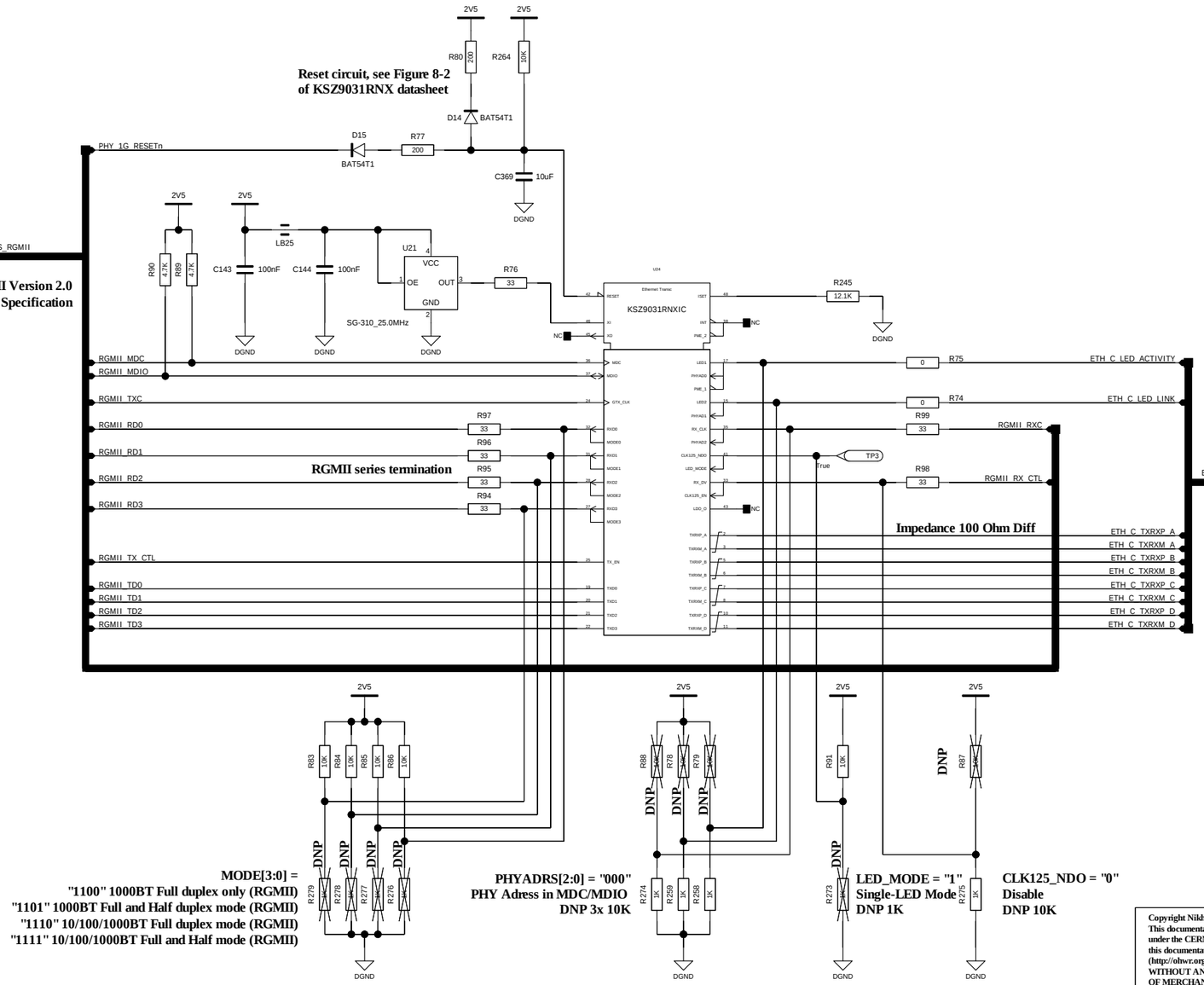
Sheet: 14 of 35 A3
Date: 2020-01-31







rev.	by	notes

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Project	:	WRITE
Sheetname	:	PS_Phy_CopperEthernet

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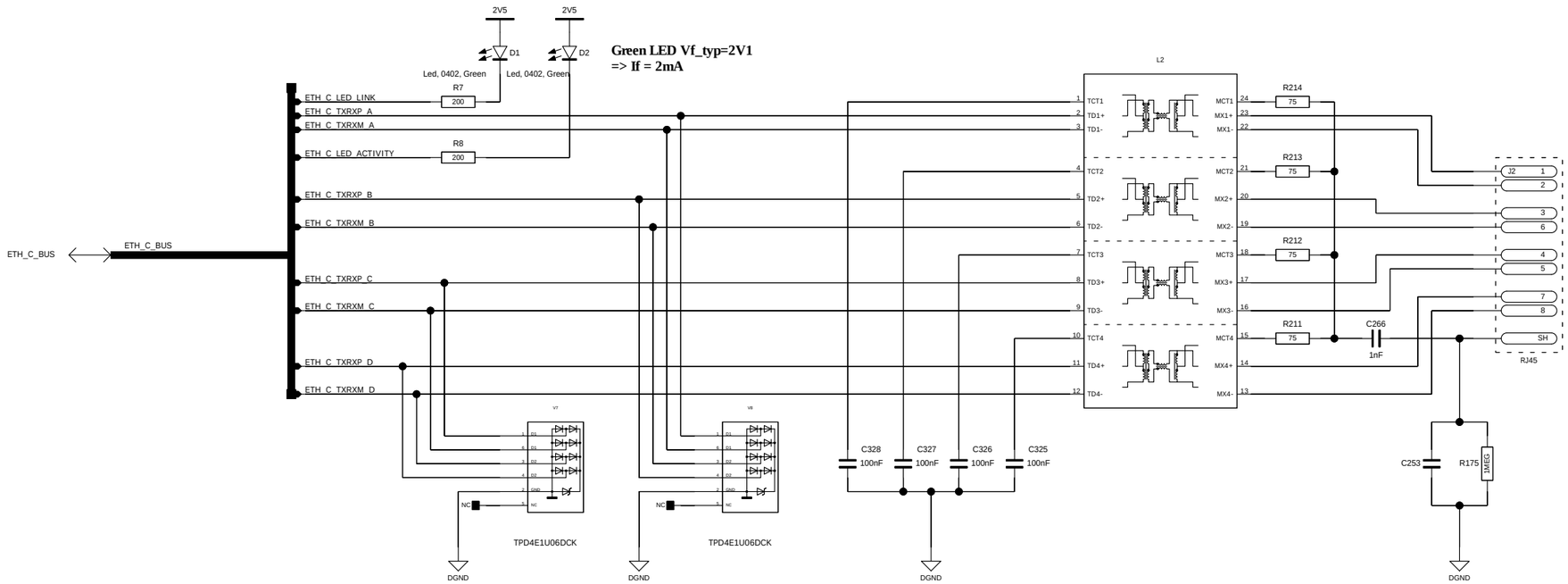

rev.	by	notes

SPEC7 v2 crystek Powered

Project	:	WRITE
Sheetname	:	PS_Phy_CopperEthernet_Jack_8p8c

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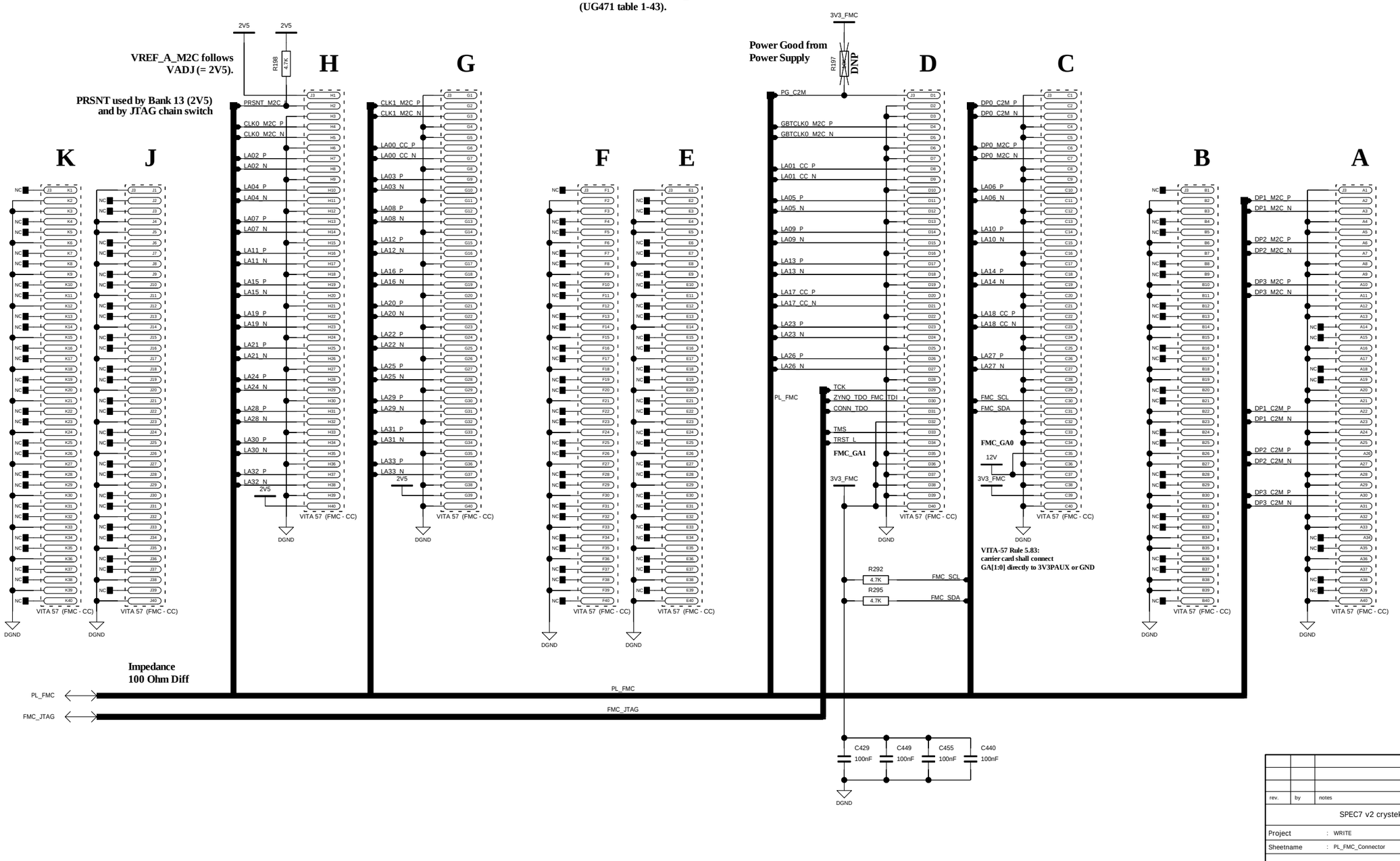
LPC FMC

Note that only LPC FMC signals are implemented!
In addition, partial HPC multi-gigabit transceiver data pairs and all HPC grounds implemented.

Vadj fixed 2V5

The HR bank of the ZYNQ only allows LVDS_25 at VCCO 2V5
(UG471 table 1-43).



rev.	by	notes

SPEC7 v2 crystek Powered

Project : WRITE
Sheetname : PL_FMC_Connector

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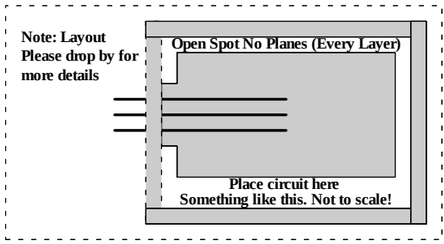
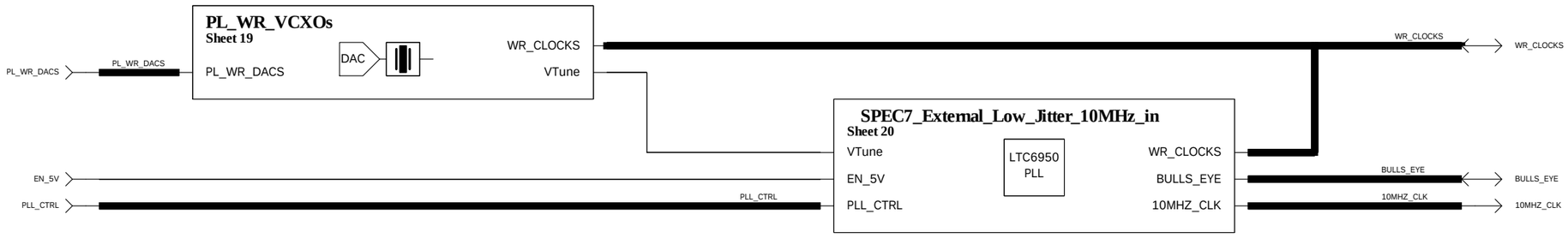
Sheet: 17 of 35 A3
Date: 2020-01-31





rev.	by	notes

SPEC7 v2 crystek Powered

Project	:	WRITE
Sheetname	:	PL_WR_Oscilators

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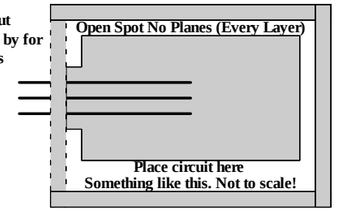
Date	2020-01-31

Note: Layout Please drop by for more details



5V
LB2
L13
1uH
C267 1uF
C270 1uF
C269 100nF
D5
V1PM10
U7
ADR4533ARZ
VRef 3V3
VREF_3V3
C278 1uF
C277 100nF
U3
TPS7A47
3V3_OSC
C32 100nF
C48 47uF
3V3 Clean
C4 47uF
C250 1uF
DGND

See Datasheet Section 7.5.1 Table 2
SBVS204F - June 2012 - Revised September 2017

1V8
U9
NLSV4T244
C63 1uF
C75 100nF
C65 1uF
C76 100nF
C77 1uF
LB10
C66 1uF
C117 100nF
C118 1uF
C125 22uF
LB17
U15
AD5662
LB14
C129 1uF
C78 22uF
C93 1uF
C92 100nF
LB11
PL_WR_DACS
Bank 35 (1V8)
DAC_DMTD_DIN
DAC_DMTD_SCLK
DAC_DMTD_SYNC_N
R58 470
C105 100nF
C106 1uF
C91 100nF
C85 1uF
U16
osc 124.992MHz
A=402
C=0
R64 0
R66 0
C119 100nF
C107 100nF
R59 10K
R68 10K
R62 200
R65 200
R63 3.92K
R67 3.92K
CLK_DMTD_P
CLK_DMTD_N
WR_CLOCKS
Impedance
100 Ohm Diff

U1
NLSV4T244
C7 1uF
C8 100nF
C9 1uF
C10 100nF
C14 1uF
LB3
C64 1uF
C35 100nF
C55 1uF
C59 22uF
LB8
U4
AD5662
LB7
DAC_REF_DIN
DAC_REF_SCLK
DAC_REF_SYNC_N
R23 470
C30 100nF
C36 1uF
C19 100nF
C18 1uF
VTune

Note:
Abracon ABLANO-V124.992MHZ = LVCMOS (0 - 3V)
Crystek CVPD-922-124.992 = LVPECL (1V4 - 2V5)
Place "A" components in case of Abracon
Place "C" components in case of Crystek
Signals connect to Bank 35 (1V8) and will have 0V9 DC offset and proper AC swing.
In ABLNO case, CLK_DMTD_N is not used.

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Project : WRITE
Sheetname : PL_WR_VCXOs

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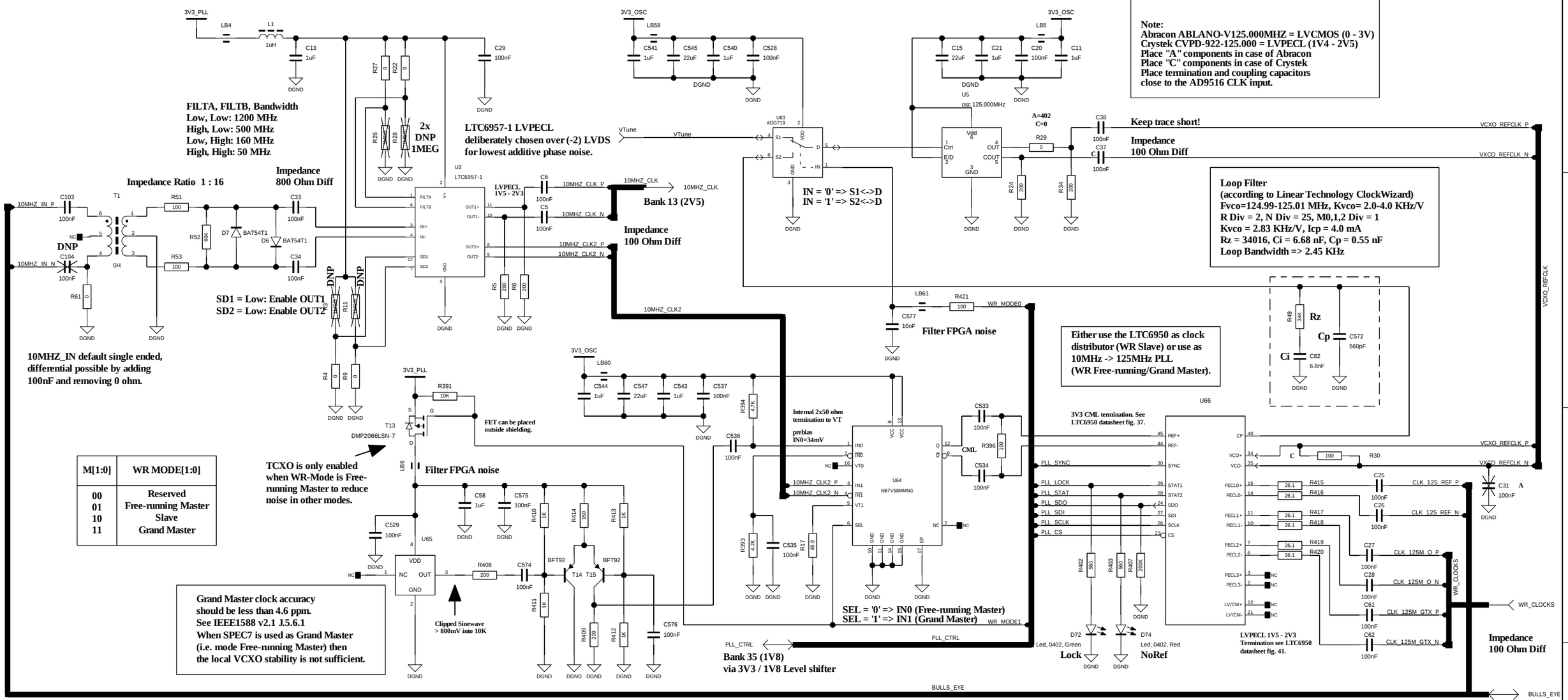

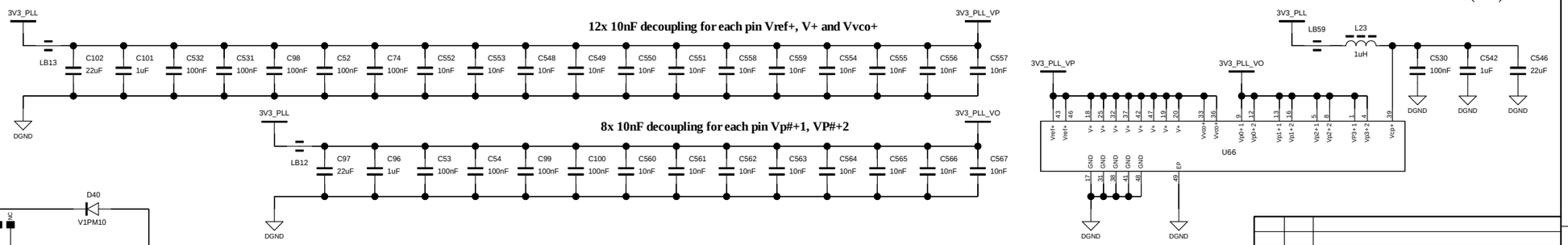

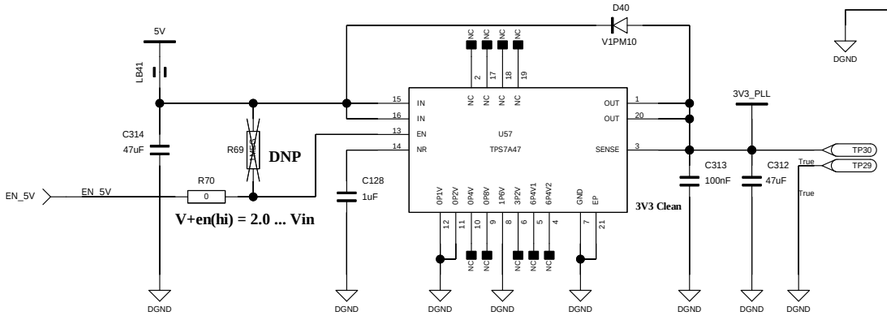

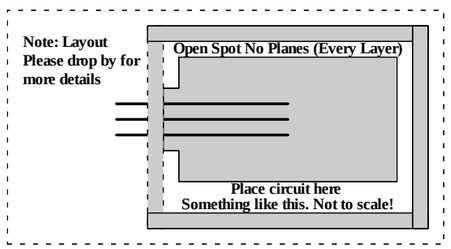

rev.	by	notes

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Project : WRITE

Sheetname : SPEC7_External_Low_Jitter_10MHz_in

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Size: 420 x 297mm

Sheet: 20 of 35 A3

Date: 2020-01-31

Bulles-Eye land pattern must be FILLED VIA-IN-PAD plated with 30 u-inches Gold plating over 50 u-inches of nickel, same as defined for the PCIe connector (see 5.4.1 Environmental Requirements (PCI Express Card Electromechanical Specification Revision 2.0)

BULLS_EYE

TIMING_SIGNALS

LVDS => Bank 35 (HP, 1V8)

ABSCAL_TXTS_P_O
ABSCAL_TXTS_N_O
SPARE_O_P
SPARE_O_N

Impedance 100 Ohm Diff

R282 100
R280 100

U28 CDCLVD2102

NC Vac_ref
INP0
INN0
INP1
INN1
EN
VCC
GND PAD

OUTP0 OUTN0 OUTP1 OUTN1 OUTP2 OUTN2 OUTP3 OUTN3

LVDS

ABSCAL_TXTS_P
ABSCAL_TXTS_N
SPARE_P
SPARE_N

Impedance 100 Ohm Diff

EN = '1' => two buffers enabled
See CDCLVD2102 datasheet Table 1

2V5 LB29 C162 1uF DGND
C163 22uF C395 1uF C394 100nF DGND

AC coupled LVDS = Bank 35 (HP)

PPS_OUT_P
PPS_OUT_N
10MHZ_OUT_P
10MHZ_OUT_N
CLK_125_REF_P
CLK_125_REF_N
BE_TXP C331 100nF
BE_TXN C330 100nF
ABSCAL_TXTS_P
ABSCAL_TXTS_N
SPARE_P
SPARE_N
PPS_IN_P
PPS_IN_N
10MHZ_IN_P C385 100nF
10MHZ_IN_N C384 100nF
BE_REFCLK_P
BE_REFCLK_N
BE_RXP C381 100nF
BE_RXN C380 100nF
BE_DMTD_P C519 100nF
BE_DMTD_N C520 100nF

J4 BDR-J-24

P	PPS_OUT
N	
P	10MHZ_OUT
N	
P	125MHz Reference Clock OUT
N	
P	TX Spare GTX OUT
N	
P	ABSCAL_TXTS OUT
N	
P	General Purpose Spare OUT
N	
P	PPS_IN (used in Grand Master mode)
N	
P	10MHZ_IN (used in Grand Master mode)
N	
P	Reference Clock IN, Spare GTX
N	
P	RX Spare GTX IN
N	
P	DMTD Spare IN
N	
	PPS_IN Single Ended

General Purpose Spare OUT (Non-re-clocked PPS when external high performance Oscillator is used and re-clocking is done there).
Reference Clock IN, Spare GTX (Also 125 MHz Reference Clock Input used for external high performance oscillator)

D46 D45 D44 D47 D43 D42 D51 D50 D49 D48 D69

Drawing on the board for pinname overview of the BullsEye
A-side are OUT
B-side are IN

FILTA, FILTB, Bandwidth
Low, High: 160 MHz

3V3 LB56 1uH L22
C538 1uF C521 100nF

U60 LTC6957-1

FILTA FILTB IN+ IN- SD1 SD2 GND OUT1+ OUT1- OUT2+ OUT2-

Impedance 100 Ohm Diff

10MHZ_P_O C524 100nF R395 100 C525 100nF 10MHZ_N_O

LVDS => Bank 35 (HP, 1V8)

C522 100nF 10MHZ_OUT_P
C523 100nF 10MHZ_OUT_N

LVPECL 1V5 - 2V3

TP34 TP35 True True

R389 200 R390 200 R387 200 R388 200

SD1 = Low: Enable OUT1
SD2 = Low: Enable OUT2

5V 3V3 LB57
C526 100nF C539 1uF

D71 CMYD4448
R397 470
U61 NC7SZ125
D71 CMYD4448
D70 VBUS05L1-DD1
R401 100 R400 100

PPS_I

Bank 13 (HR, 2V5)

2V5 LB26
C153 1uF C152 22uF C151 1uF C407 100nF

U30 CDCLVD2102

VCC
Vac_ref
INP0 INN0 INP1 INN1 EN
OUTP0 OUTN0 OUTP1 OUTN1 OUTP2 OUTN2 OUTP3 OUTN3
GND PAD

DMTD_P_I
DMTD_N_I
PPS_P_I
PPS_N_I

LVDS => Bank 35 (HP, 1V8)

BE_DMTD_P
BE_DMTD_N
PPS_IN_P
PPS_IN_N

EN = Open => two buffers enabled
See Table 1

49.9 R82 49.9 R81 49.9 R107 49.9 R106
C150 1uF C161 100nF

2V5 LB47
C415 1uF R102 10K
C396 22uF C149 1uF C160 100nF

U29 MAX9381

VCC D D Q Q CLK CLK VEE

PPS_P_O
PPS_N_O
R92 100

LVPECL

PPS_OUT_P
PPS_OUT_N

CLK_125M_O_P
CLK_125M_O_N

Impedance 100 Ohm Diff

R104 100 **no internal termination**
R103 10K

Bias and Termination must be put at the end of the line.

R105 91 R93 91

WR_CLOCKS

Reclock PPS with clean Reference Clock

Note:
10 MHz can not be re-clocked with 125 MHz.
For 50% duty Cycle a 500 MHz re-clock is needed.
SPEC7 forwards the 10MHz ouput clock from the FPGA to the Bulls-Eye.
For low jitter this 10 MHz ouput needs to be re-clocked with the external high performance oscillator.

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Project : WRITE
Sheetname : PL_BullsEye

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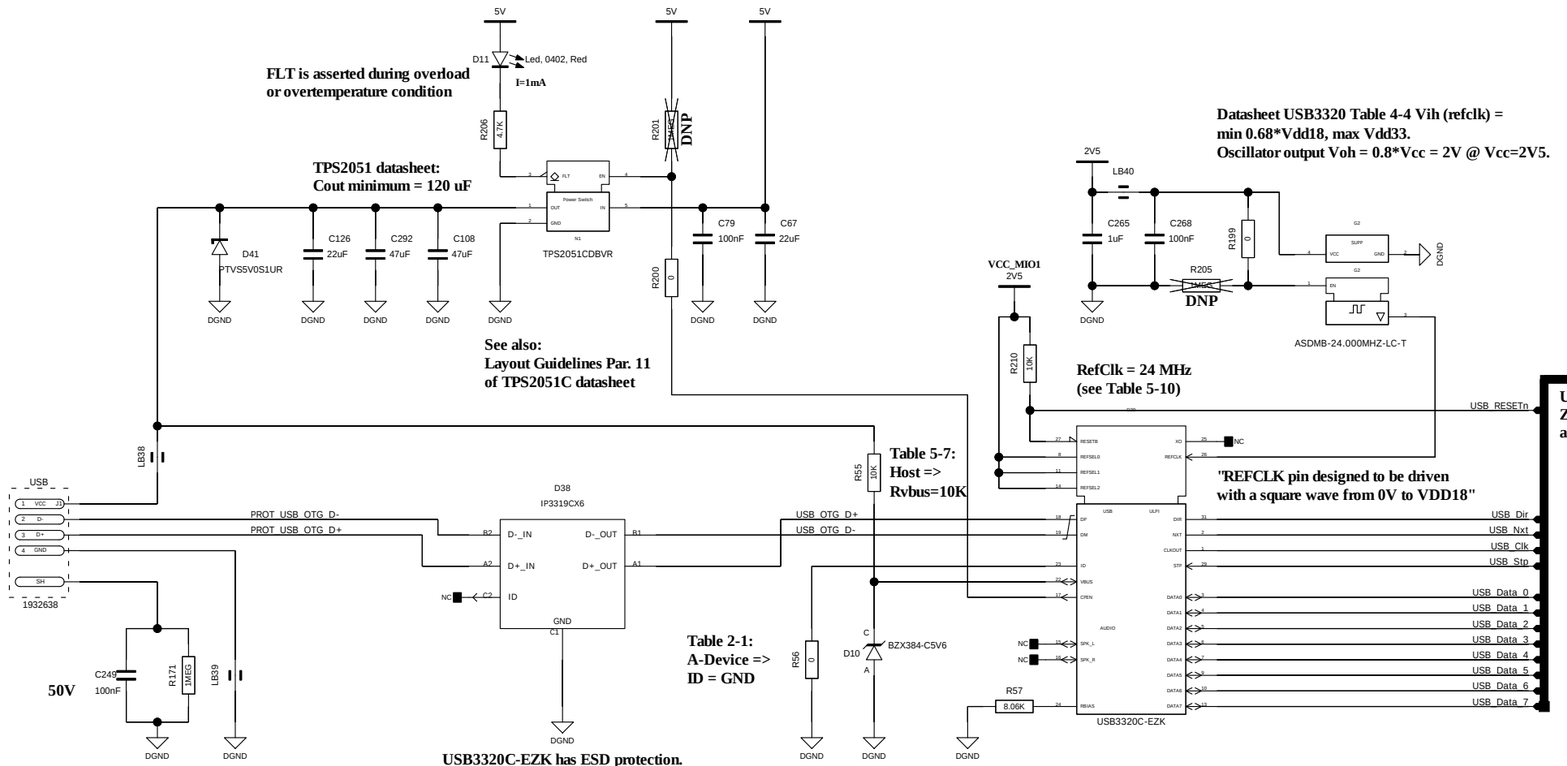
Date 2020-01-31

USB 2.0 A-Device (i.e. host)



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Project : WRITE

Sheetname : PS_USB_OTG

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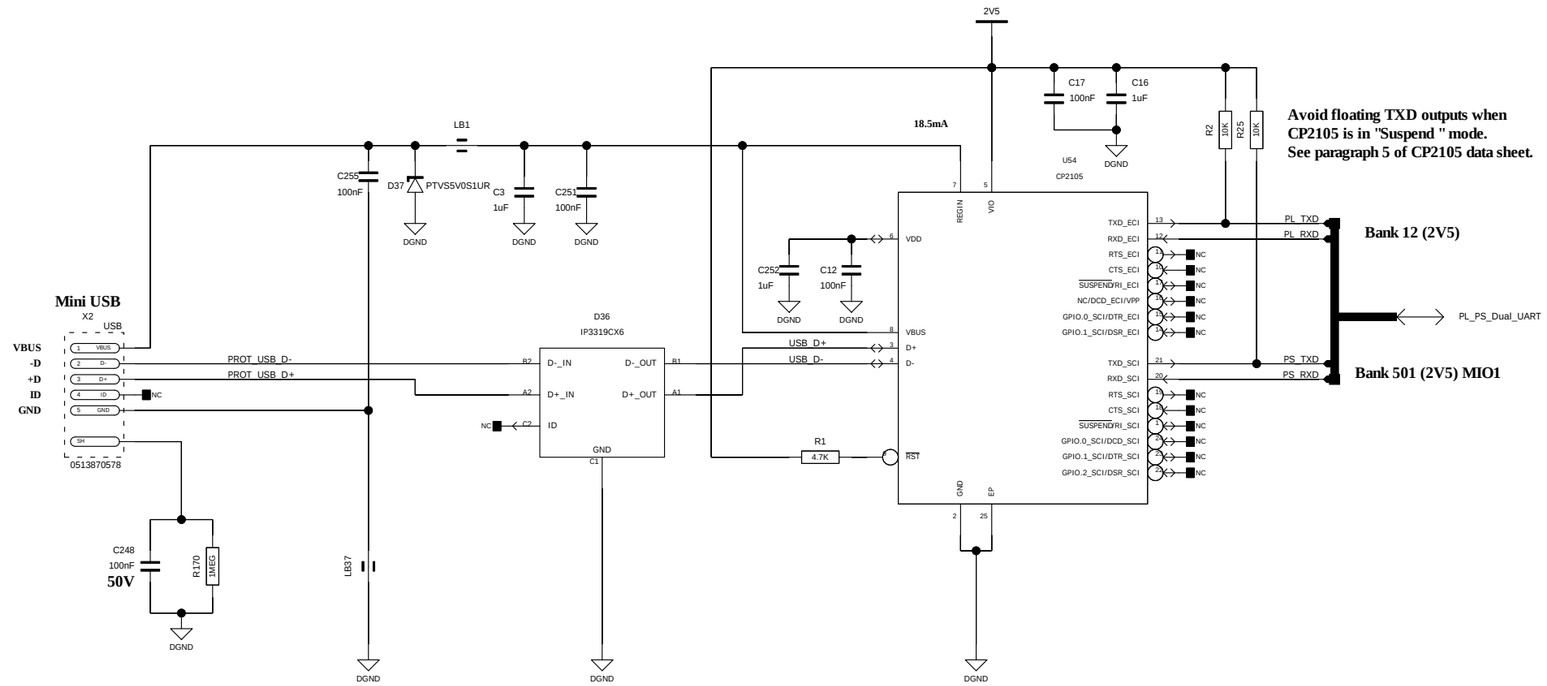
PL_USB
PS_USB



Diffrential impedance must 90 Ohm,See Universal Serial Bus Specification Revision 2.0 chapter 7.1

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Sheetname : PL_PS_Uart

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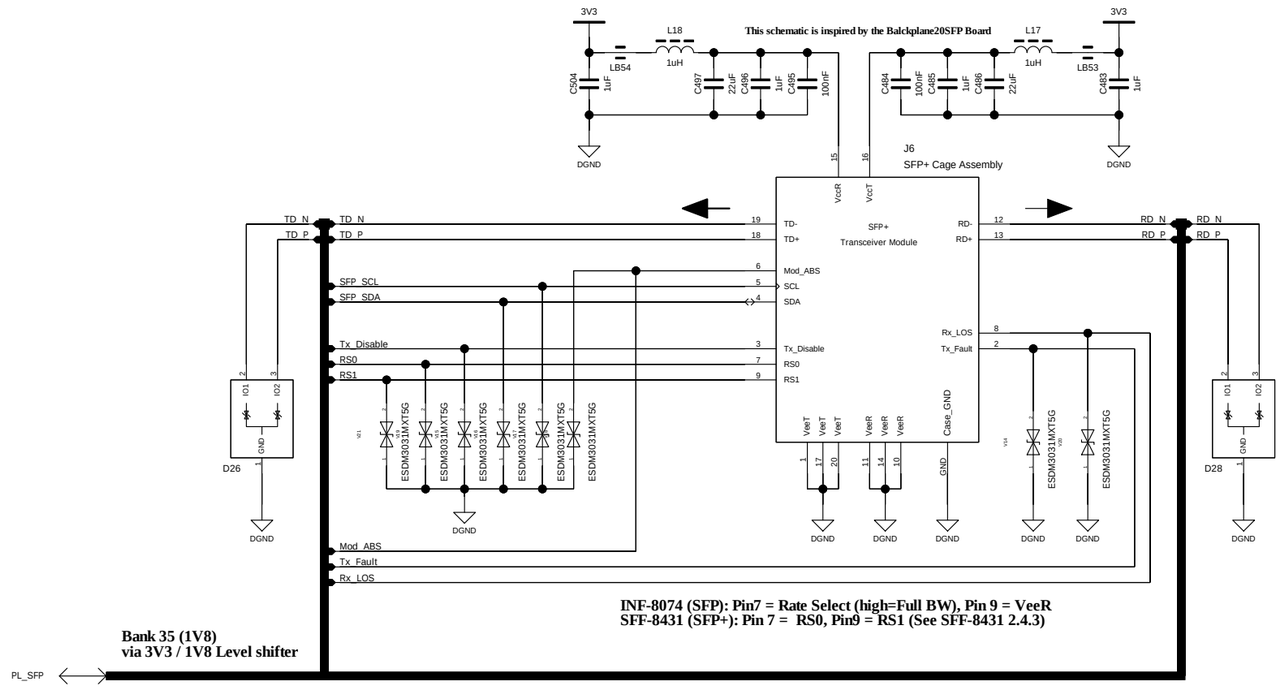

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Project : WRITE

Sheetname : PL_SFP_Connector

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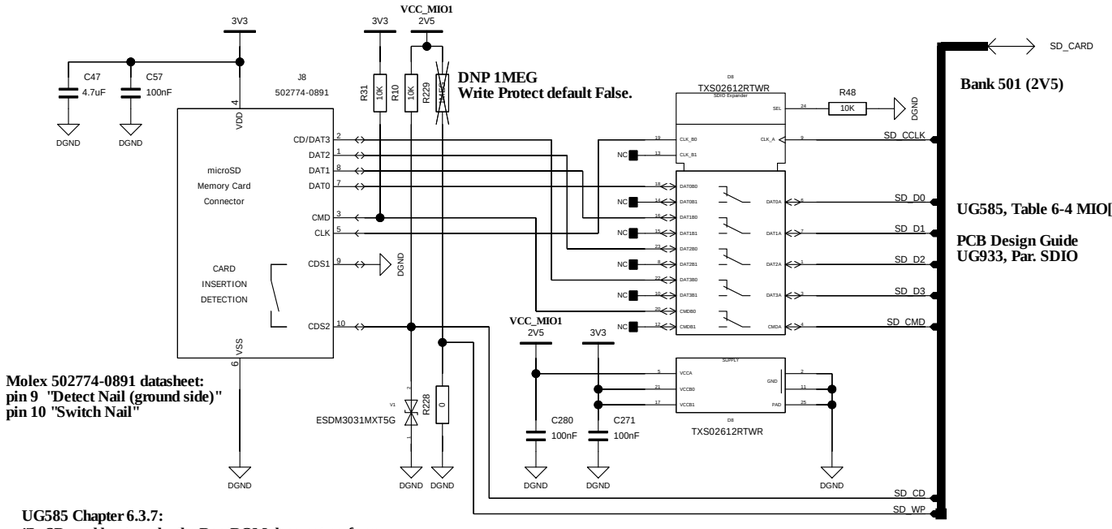

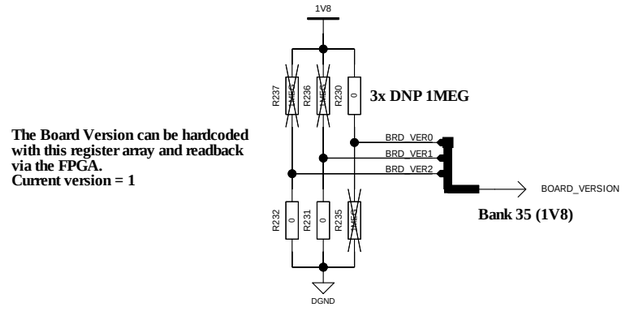

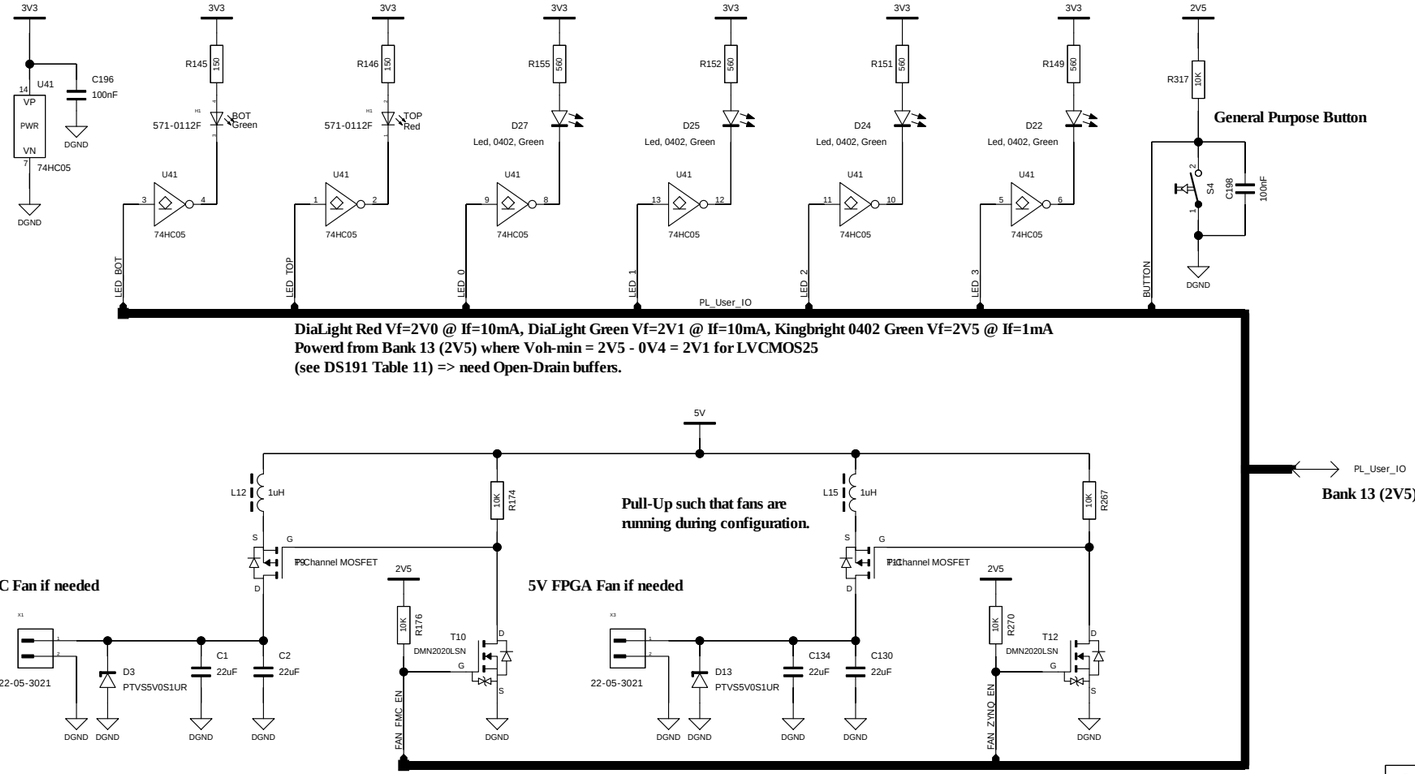

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Project	:	WRITE
Sheetname	:	PL_User_IO

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Pull-down:
IEEE-1149.1 Par. 4.2.2

'0' when JTAG cable is plugged
ELSE
'1' => JTAG control from FPGA PL

Pull-up:
IEEE-1149.1 Par. 4.3.2

TRST_L Default
Pull-up

Optional TRST_L control using the HALT signal (see DS593).

Pull-up:
IEEE-1149.1 Par. 4.4.2

ZYNQ always in JTAG chain

PRSTNT_M2C_L Pullup to 2V5
on FMC schematic (also used by BANK 13, 2V5)
Note 2V5 > Vih_min (0.7*3V3) on JTAG chain switch

DNP

Possibility to put 0 ohm for FMC mezzanines that do not connect TDI-TDO

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Project : WRITE
Sheetname : SPEC7_JTAG_Chain

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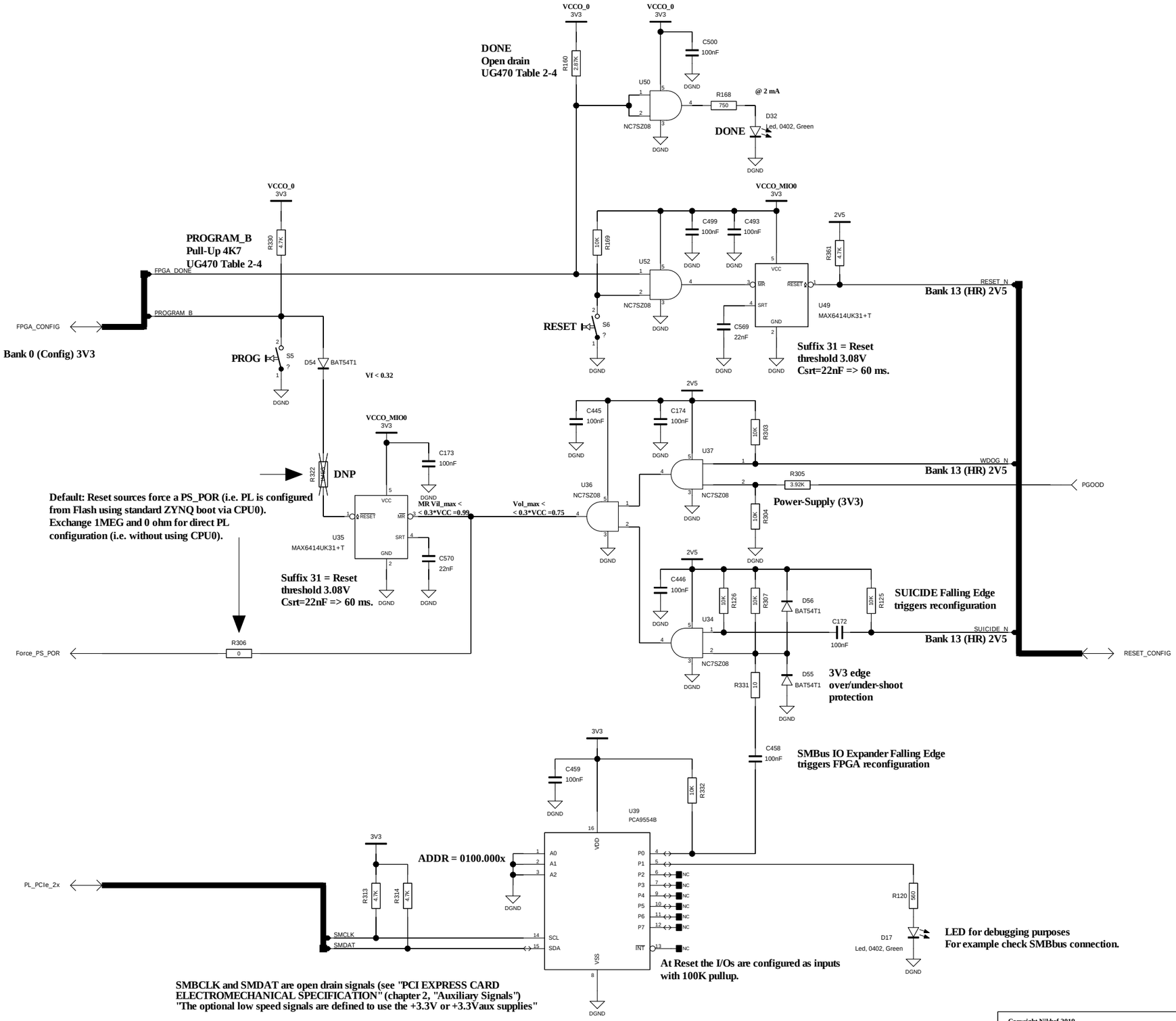

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Project	:	WRITE
Sheetname	:	SPEC7_Reset_Config

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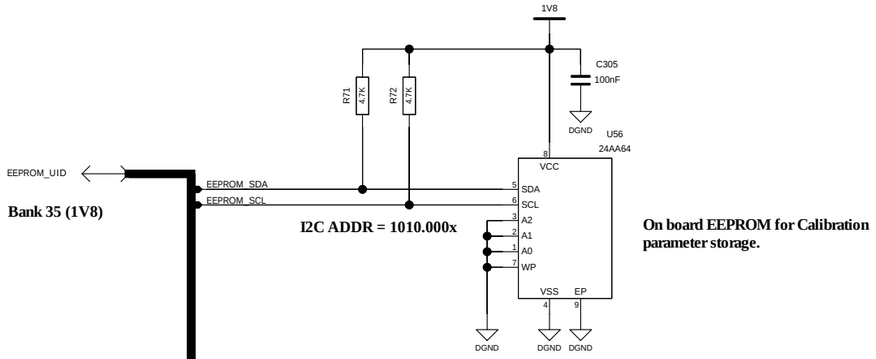
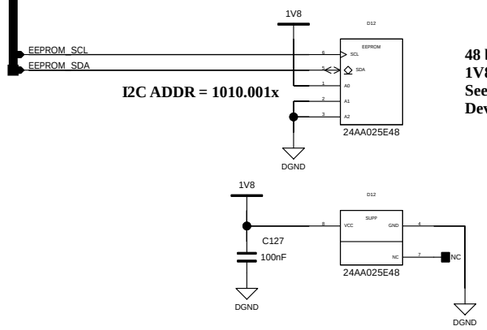


Bank 35 (1V8)

I2C ADDR = 1010.000x

On board EEPROM for Calibration parameter storage.



I2C ADDR = 1010.001x

48 bit Unique ID (WR MAC Address)
1V8 capable but fmax = 100 KHz for VCC < 2v5
See datasheet 24AA025E48
Device Selection Table Note 1

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Project : WRITE

Sheetname : PL_EEPROM_Unique_ID

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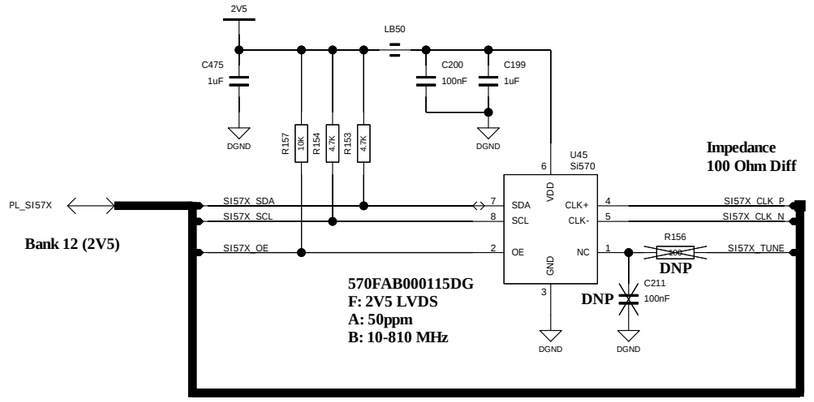

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Project : WRITE

Sheetname : PL_SI570

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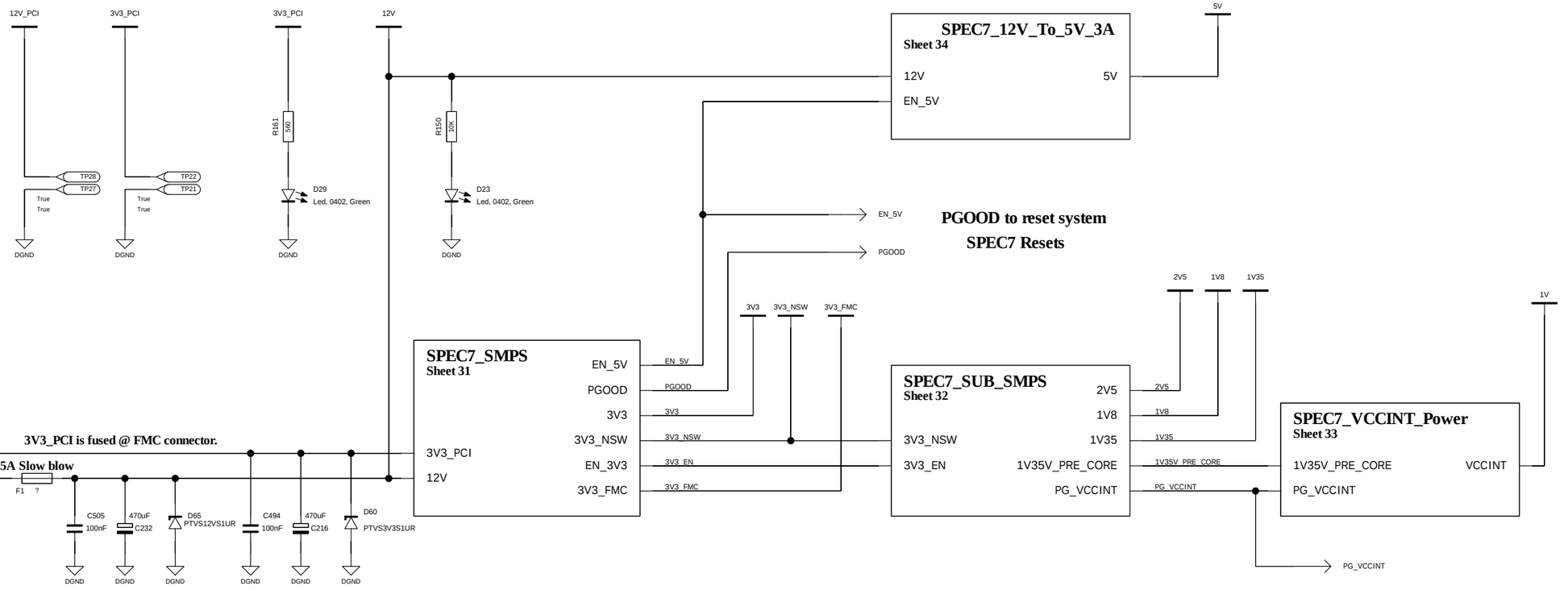

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Project : WRITE

Sheetname : SPEC7_Power_System

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3V3 @ 10A

Ven max = 3.6 V
Enabled when Ven > 1V2

Make the current loop so small as possible
47uF cap should be a 1210 package see datasheet

Place close as possible to switcher

Compesation network Type III
See EN29A0Q1 datasheet
Figure 7 and Table 9

Over Voltage Protection set to 3V45.

feedback network

Feedback network is referenced to GNDSNS (Ground Ref point)

Note :

POK = Power is oke when Vout is +/- 10%
POK = Open Drain, High is oke.
POK = POK_3V3,Controls. 1V35 SMPS

Switch Freq set to 2 MHz.
Softstart 200 ms.
Output Overvoltage set to 3.45V.

Slowly turn on FET V3 to reduce inrush current.

Vgs protection.

Vgs protection

Note:

SPEC7 Resets PGOOD to reset system

Dual MOSFETs eliminate current flow from V3_FMC_F to 3V3_NSW or 3V3_PCI or vice versa via MOSFET body diode.

PIN 1 - 19 (NC) may be connected to Vout
See EN29A0QI Table 2

PIN 87 (NC) May be connected to PVIN,VOUT,GDNG Planes
See EN29A0QI Table2
See also figure 9 Typical Appliction Circuit

When EN_3V3 And PCI_3V3 then route 3V3_PCI to 3V3_FMC
When EN_3V3 And NOT PCI_3V3 then route 3V3_NSW to 3V3_FMC

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Project : WRITE
Sheetname : SPEC7_SMPS

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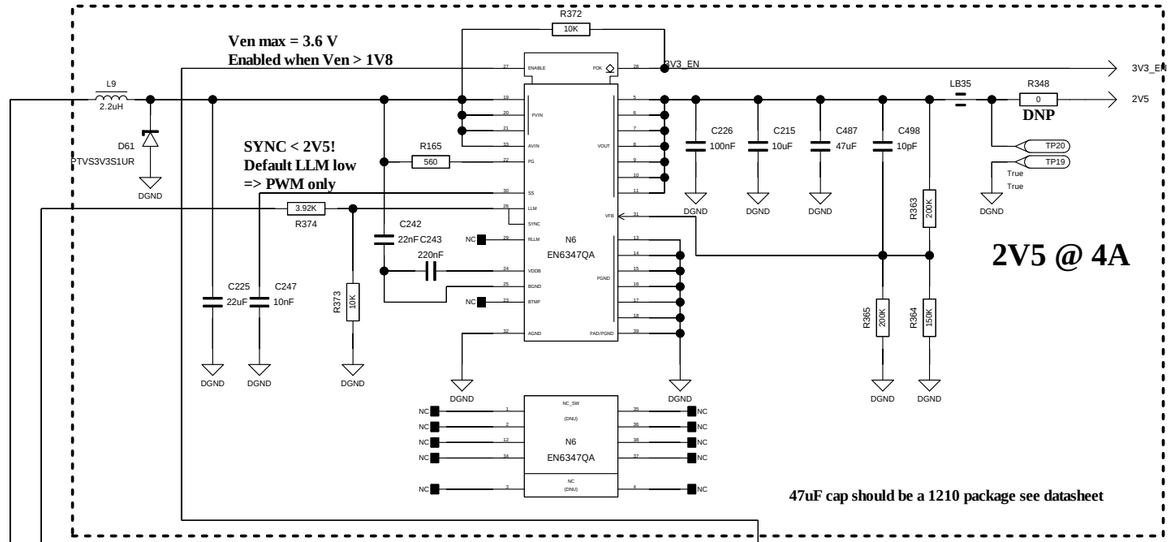

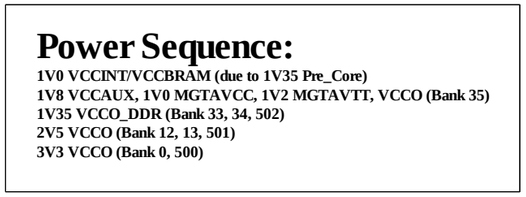

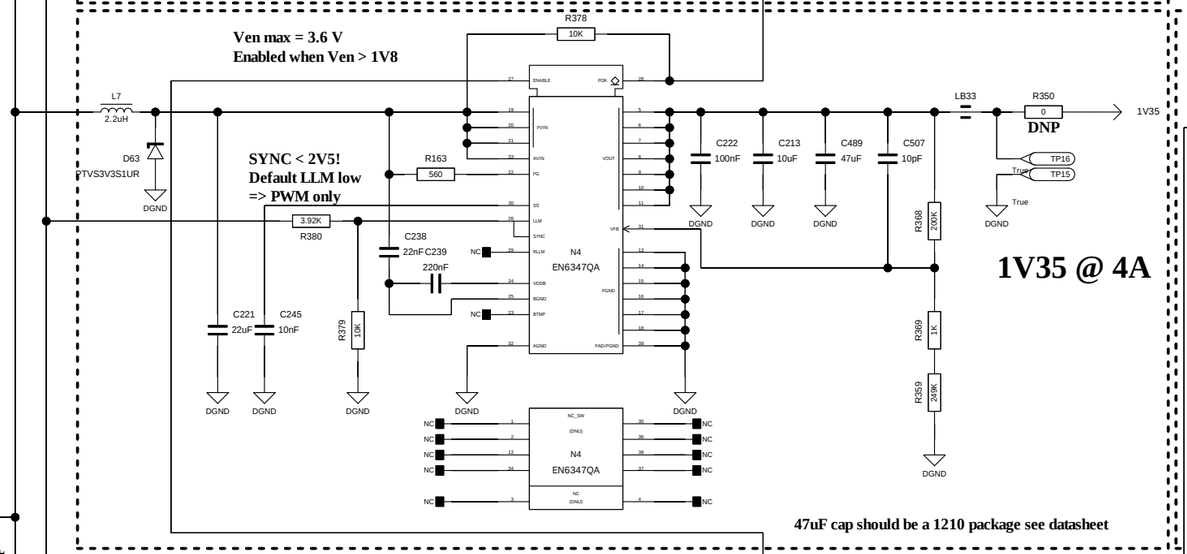

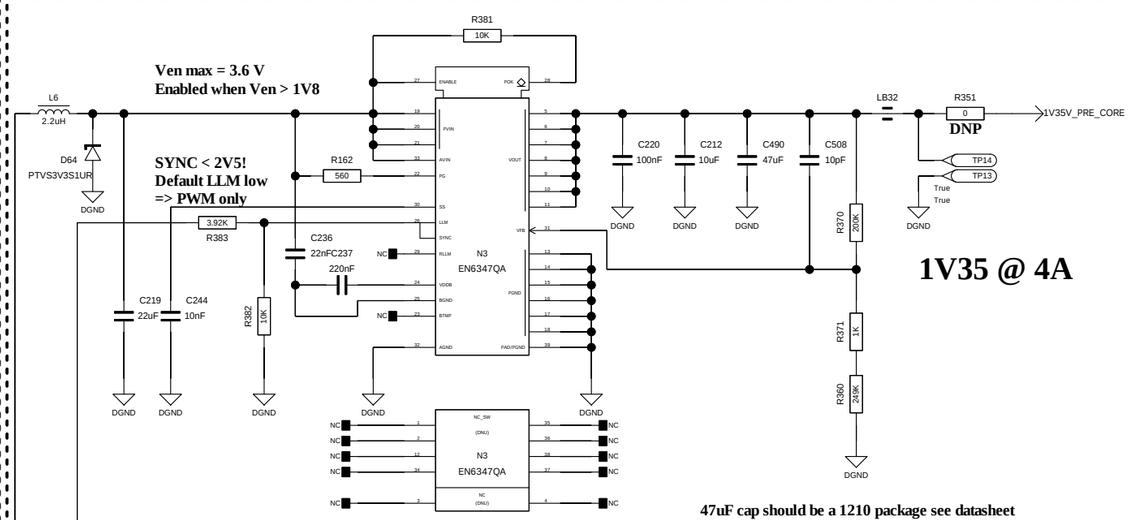

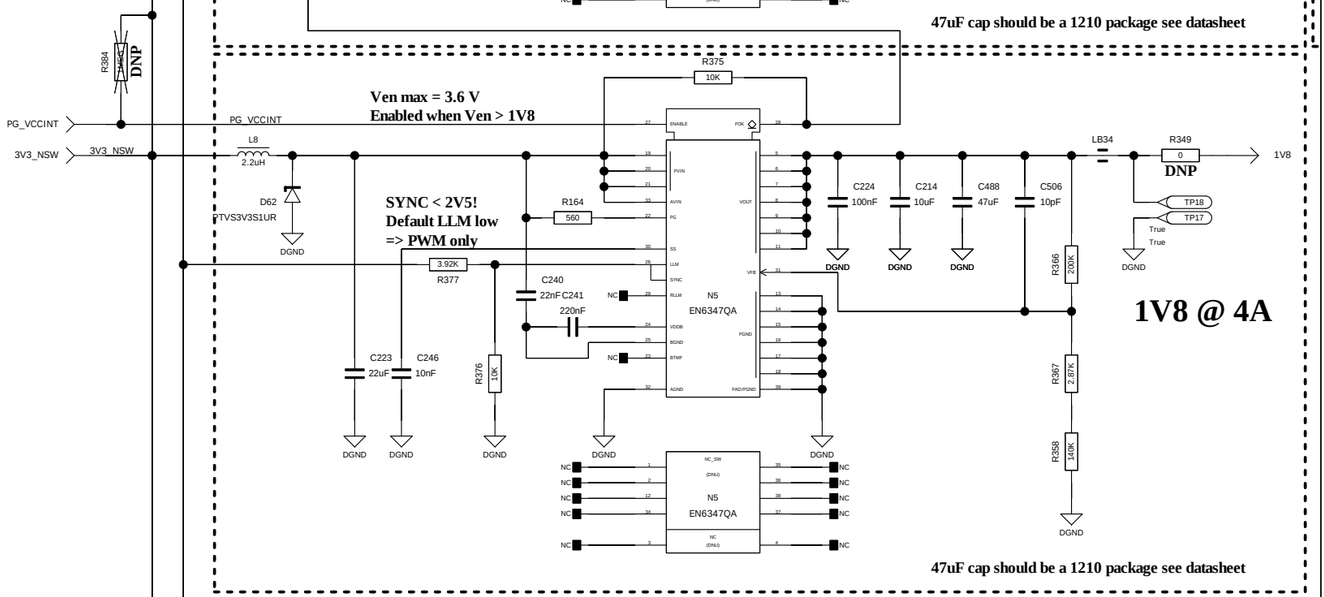

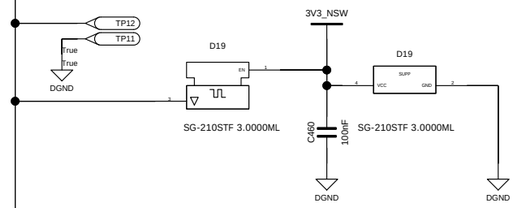

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Project	:	WRITE
Sheetname	:	SPEC7_SUB_SMPS

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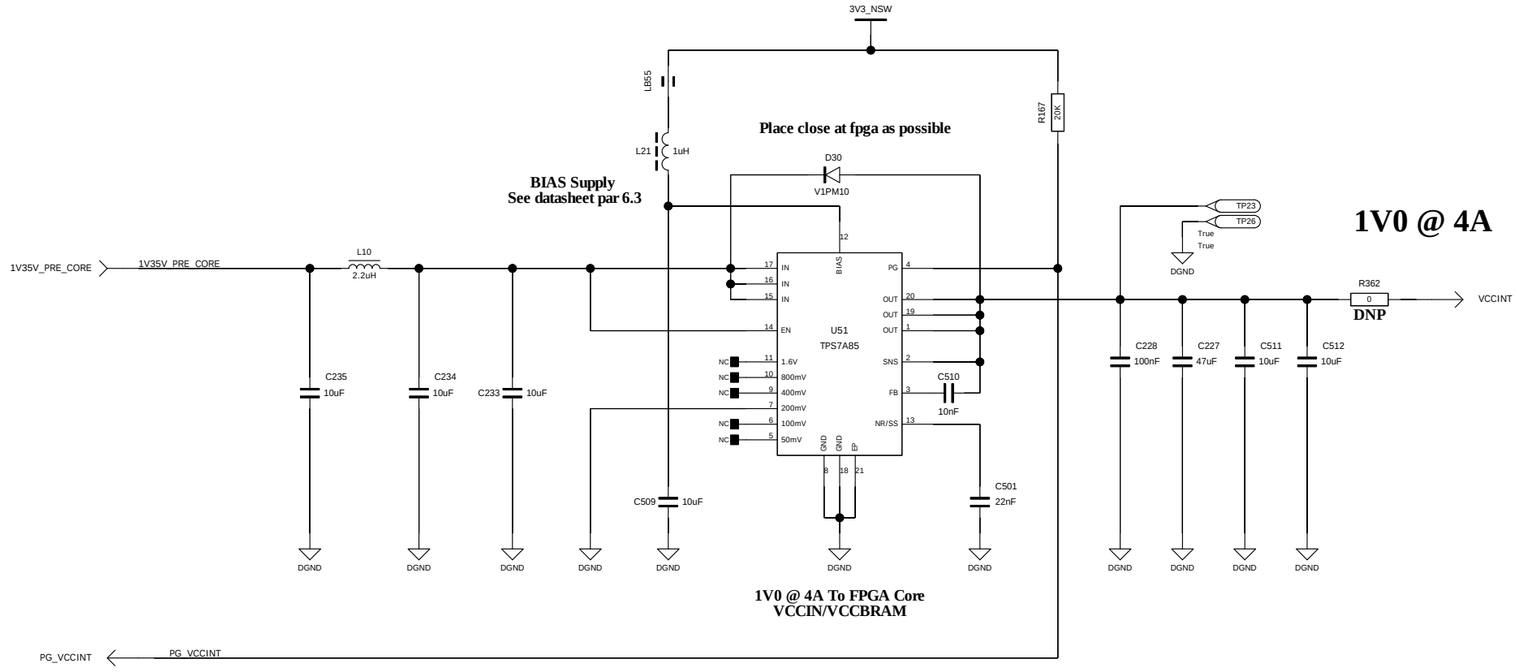

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SPEC7 v2 crystek Powered

Project : WRITE

Sheetname : SPEC7_VCCINT_POWER

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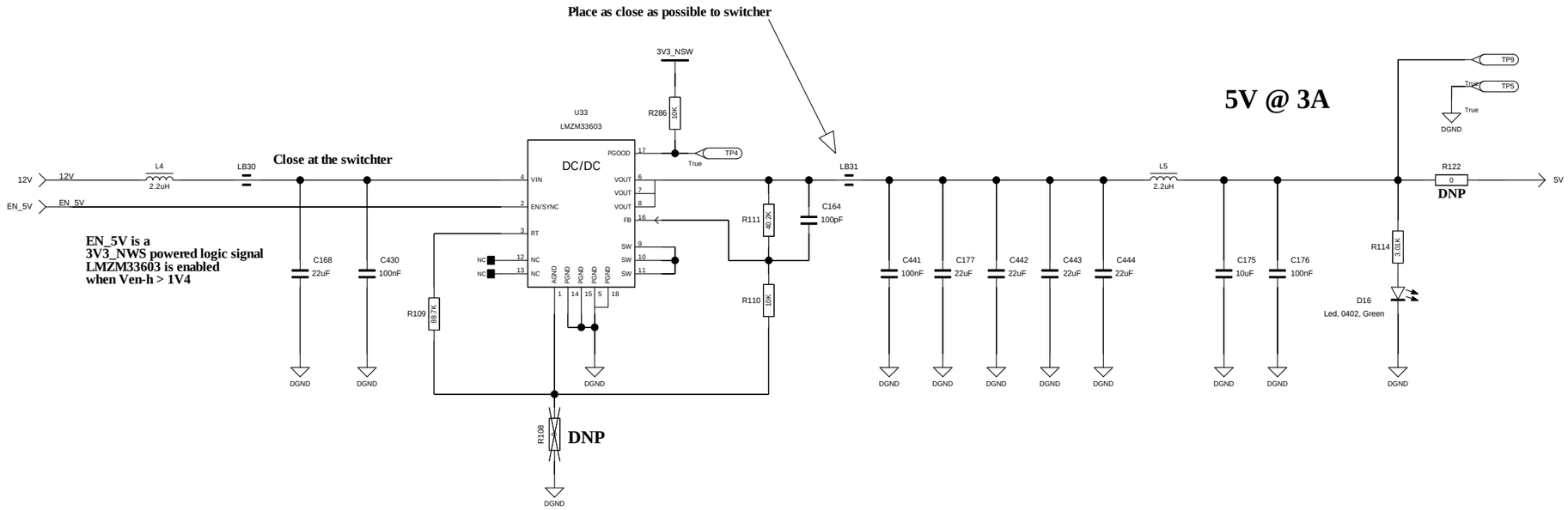

LMZM33603 datasheet Table 1:
Vin = 12V, Vout = 5V
RT = 88.7 K (fsw=450 Khz)
Rfbt = 40.2 K
Cff = 100 pF
66 uF < Cout <200 uF

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Project : WRITE

Sheetname : SPEC7_12V_To_5V_3A

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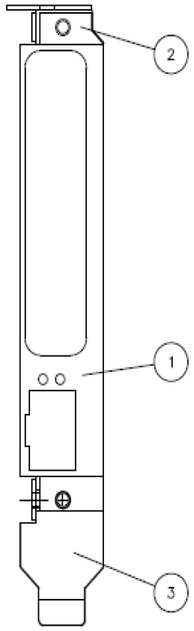
Mechanical Parts



1	NC	MP13 3200-0478	**Frontpanel for SPEC Card**
2	NC	MP14 3200-0476LC	**Steel Bracket for SPEC Card, Up**
3	NC	MP15 3200-0477LC	**Steel Bracket for SPEC Card, Down**
	NC	MP16 BN-330-1123238	**M2.5-6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated**
	NC	MP17 BN-330-1123238	**M2.5-6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated**
	NC	MP18 BN-330-1123238	**M2.5-6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated**
	NC	MP19 BN-330-1123238	**M2.5-6 Screw, Slotted Cheese Head, Zinc Coated Steel, Passivated**
	NC	MP20 11300.01.01.2	**SPEC7 v2 PCB, PCIe, 14Layers**
	NC	MP11 AAVID 342943	**FPGA Heatsink**

Shielding for PL WR VCXO's

MP5	S1711-46R	RFI Shield Clip, Midi
MP8	S1711-46R	RFI Shield Clip, Midi
MP1	S1711-46R	RFI Shield Clip, Midi
MP4	S1711-46R	RFI Shield Clip, Midi
MP9	S1711-46R	RFI Shield Clip, Midi
MP12	S1711-46R	RFI Shield Clip, Midi
MP3	S1711-46R	RFI Shield Clip, Midi
MP2	S1711-46R	RFI Shield Clip, Midi
MP7	S1711-46R	RFI Shield Clip, Midi
MP10	S1711-46R	RFI Shield Clip, Midi
MP6	1500-35-50-10-TS0.20	Clip-On EMI Shielding Can, 35x50mm, Height=10mm

DGND

NC	MP21	UB5U3-700 DC Fan, 30x30x3mm, 5V/0.35A, 9500RPM
NC	MP22	M1.7x? Pan Head Screw
NC	MP23	M1.7x? Pan Head Screw
NC	MP24	M1.7x? Pan Head Screw
NC	MP25	M1.7 Washer
NC	MP26	M1.7 Washer
NC	MP27	M1.7 Washer
NC	MP28	M1.7 Nut
NC	MP29	M1.7 Nut
NC	MP30	M1.7 Nut

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Project : WRITE

Sheetname : SPEC7_Mechanical_Parts

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