The supported COM Express Type 6 modules are limited to only Revision 2.0 and up. Since Revision 2.0 of the COM Express specification two serial ports are available on the Type 6 COM Express Modules which are pins on the module that have been excluded from the +5V VCC_12V pin. As such, it is possible that a Type 6 R0 Module is deployed on the +5V VCC_12V pin that may bridge 12V on the serial pins SIR1 TX, SIR1 RX, SIR1 RX, and SIR1 tx. These signals are not protected against 12V. It is highly recommended that any signals connected to +12V are pulled to 12V on the module and not connected to R2+0 branches as they are not used for external detection.
Layout note.
Place ESD protection devices close to the connector.
Place ESD protection devices close to the connector.
Layout note: Place ESD protection device close to the connector.
Layout note.
Place ESD protection device close to the connector.
Standard logic devices powered by 3V3.

Layout note: Place ESD protection devices close to the connector.
Standard logic device powered by P3V3.

Layout note. Place ESD protection devices close to the connector.
The connector pin layout should be changed for better routing.

'Trigger and Serial circuits should be placed on a mezzanine PCB.'

This mezzanine PCB should be connected to the main PCB using the mounting holes.

05.60.125 mounting brackets mounted on the two plated 2.7mm can for example be done using two Ettinger 05.60.422 or similar holders.

The Trigger and RS232 circuits should be placed on a mezzanine PCB.

Layout note:
Place ESD protection devices close to the connector.

The Trigger and RS232 circuits should be placed on a mezzanine PCB electrically connected to the circuits of the front panel.

This can be realized by using the ETTL connection DB-122 or ETTL connection DB-123. The 2.7mm can is used with two 2.3mm mounting holes.
Zero delay PCI Express GEN-3 clock buffer.
The outputs are all identical and so for easier routing the output ports (DIF[0 to 3]) may be swapped for a better connection to the 4 differential RefClk+/- signals.

PLL mode selection (HIBW_BYPM_LOBW):
- 3.3V (1): PLL high Bandwidth.
- 1.65V (M): PLL bypass.
- 0V (0): PLL low bandwidth.

Preferably use High Bandwidth by setting the configuration resistors.

Configuration resistors are available to put the clock buffer into "Bypass Mode", which experience has shown is needed in some Carrier situations.

SMBus interface is not connected to prevent potential conflicts with COM Express Module or PXIe MMIO devices otherwise. So SMAR_x is not connected (it has an internal pull-down).

1. Route power from bead through bulk capacitor pad then through 100nF capacitor pad then to clock chip Vdd pad.
2. Do not share ground vias. One ground pin one ground via.
3. Exposed pad must be grounded properly.
4. SMBus interface is not connected to prevent potential conflicts with COM Express Module or PXIe MMIO devices otherwise. So SMAR_x is not connected (it has an internal pull-down).

See COM Express design Guide Rev 2.0 section 6.5.1 for the routing guidelines. A 85 Ohm +/- 15% differential impedance is recommended.
The PCI Express transmit coupling capacitors are already part of the COM Express module. See COM Express design guide Rev. 2.0 section 2.5.6.

The PCI Express receive signals run on the COM Express (PCI Express 3.0 x1/3.0 x4) lane and are terminated either at the destination board or at the card edge connector. The receiver output may be driven in or out of low-power state in order to simplify the design for low-power operation or low-power state.

The PCI Express receive coupling capacitors are already part of the COM Express module. See COM Express design guide Rev. 2.0 section 2.3.6.1 and 2.4.4.

The PCI Express lanes are grouped in four links of four lanes. This is the 4-lane configuration of CompactPCI Express and PXI Express (see also the PXI Express Electronic Specification Rev. 3.1 section 5.5.1). The four lanes of each link (3.3 V to 3.3 V) can be interconnected as long as the individual lanes (link 0 to link 3 and link 1 to link 2) within the links are connected one-to-one. Lane swapping is not permitted.

See COM Express design guide Rev. 2.0 section 6.5.1 for the routing guidelines. A 100 Ω termination is recommended.
mSATA SSD memory card

Project/Equipment: PXIe controller COM Express based carrier

INCAA Computers

Sketch by:

07/11/2019

INCAA Computers

Last Mod.

01-May-20

Copyright CERN 2020. This source describes Open Hardware and is licensed under the CERN-OHL-S v2.
The I/O ports are not yet connected to the FPGA because this fully depends on the placement and routing of the PCB.

These I/O ports are not yet connected to the FPGA because this fully depends on the placement and routing of the PCB.

PXI_STAR should be attached to a FPGA I/O pads which is also a MRCC capable input.

PXI_CLK[0-3] should be attached to 4 FPGA I/O pads which is also a MRCC capable input.

As an PXI_TRIG0 input only one of these four (the MRCC capable input) is needed.

PXI_CLK[0-3] are capable of incident wave switching on rising edges, preventing jitter degradation due to transmission line effects.

Forcing voltage high V(oh)(AC) = 2.5 V (max)

High source current I(o)h(AC) = 75 mA (min)
Standard logic devices powered by PIV3

LED for during config

LED for during config error

These IO ports are not yet connected to the FPGA because this fully depends on the placement and routing of the PCB.
PCB Decoupling Capacitors according to 7 series FPGAs PCB Design Guide UG483 (v1.13) August 18, 2017, Table 2-2.

VCCINT
C35 100uF  C36 100uF  C37 4.7uF  C38 4.7uF  C39 4.7uF  C40 330uF  C41 330uF  C42 330uF  C43 330uF  C44 330uF

VCCBRAM
C45 100uF  C46 100uF  C47 4.7uF  C48 4.7uF  C49 4.7uF

VCCAUX
C50 100uF  C51 100uF  C52 100uF  C53 330uF  C54 330uF  C55 330uF  C56 330uF  C57 330uF  C58 330uF  C59 330uF  C60 330uF

VCCO_34
C61 4.7uF  C62 4.7uF  C63 4.7uF  C64 4.7uF  C65 4.7uF  C66 4.7uF

VCCO_35
C67 4.7uF  C68 4.7uF  C69 4.7uF  C70 4.7uF  C71 4.7uF  C72 4.7uF  C73 4.7uF  C74 4.7uF  C75 4.7uF  C76 4.7uF  C77 4.7uF  C78 4.7uF

†PCB Decoupling Capacitors according to 7 series FPGAs PCB Design Guide UG483 (11.13) August 18, 2017, Table 2-2.
**LAYOUT NOTES:**

- Place the input capacitor close to the top switching FET. The output capacitance for the bottom FET should also be kept as small as possible.
- Make sure all component leads are soldered solidly to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin (FBx) of the device.

- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.

**DC/DC calculations**

- No. 2700 µA
- Rtrip is calculated

1.8 V and 1.0 V

**Switching Regulator**

- V1: 100 µF
- V2: 100 µF
- C1: 10 µF
- C2: 10 µF
- R1: 10 kΩ
- R2: 10 kΩ
- L1: 2.2 µH
- L2: 2.2 µH

**Ground**

- GND

**Feedback pin (FBx)**

- Make a single point connection from the signal ground to power ground.

**Switching Regulator**

- V1: 100 µF
- V2: 100 µF
- C1: 10 µF
- C2: 10 µF
- R1: 10 kΩ
- R2: 10 kΩ
- L1: 2.2 µH
- L2: 2.2 µH

**Ground**

- GND

**Feedback pin (FBx)**

- Make a single point connection from the signal ground to power ground.

**Switching Regulator**

- V1: 100 µF
- V2: 100 µF
- C1: 10 µF
- C2: 10 µF
- R1: 10 kΩ
- R2: 10 kΩ
- L1: 2.2 µH
- L2: 2.2 µH

**Ground**

- GND

**Feedback pin (FBx)**

- Make a single point connection from the signal ground to power ground.

**Switching Regulator**

- V1: 100 µF
- V2: 100 µF
- C1: 10 µF
- C2: 10 µF
- R1: 10 kΩ
- R2: 10 kΩ
- L1: 2.2 µH
- L2: 2.2 µH

**Ground**

- GND

**Feedback pin (FBx)**

- Make a single point connection from the signal ground to power ground.

**Switching Regulator**

- V1: 100 µF
- V2: 100 µF
- C1: 10 µF
- C2: 10 µF
- R1: 10 kΩ
- R2: 10 kΩ
- L1: 2.2 µH
- L2: 2.2 µH

**Ground**

- GND

**Feedback pin (FBx)**

- Make a single point connection from the signal ground to power ground.

**Switching Regulator**

- V1: 100 µF
- V2: 100 µF
- C1: 10 µF
- C2: 10 µF
- R1: 10 kΩ
- R2: 10 kΩ
- L1: 2.2 µH
- L2: 2.2 µH

**Ground**

- GND

**Feedback pin (FBx)**

- Make a single point connection from the signal ground to power ground.

**Switching Regulator**

- V1: 100 µF
- V2: 100 µF
- C1: 10 µF
- C2: 10 µF
- R1: 10 kΩ
- R2: 10 kΩ
- L1: 2.2 µH
- L2: 2.2 µH

**Ground**

- GND

**Feedback pin (FBx)**

- Make a single point connection from the signal ground to power ground.

**Switching Regulator**

- V1: 100 µF
- V2: 100 µF
- C1: 10 µF
- C2: 10 µF
- R1: 10 kΩ
- R2: 10 kΩ
- L1: 2.2 µH
- L2: 2.2 µH

**Ground**

- GND

**Feedback pin (FBx)**

- Make a single point connection from the signal ground to power ground.

**Switching Regulator**

- V1: 100 µF
- V2: 100 µF
- C1: 10 µF
- C2: 10 µF
- R1: 10 kΩ
- R2: 10 kΩ
- L1: 2.2 µH
- L2: 2.2 µH

**Ground**

- GND

**Feedback pin (FBx)**

- Make a single point connection from the signal ground to power ground.

**Switching Regulator**

- V1: 100 µF
- V2: 100 µF
- C1: 10 µF
- C2: 10 µF
- R1: 10 kΩ
- R2: 10 kΩ
- L1: 2.2 µH
- L2: 2.2 µH

**Ground**

- GND

**Feedback pin (FBx)**

- Make a single point connection from the signal ground to power ground.

**Switching Regulator**

- V1: 100 µF
- V2: 100 µF
- C1: 10 µF
- C2: 10 µF
- R1: 10 kΩ
- R2: 10 kΩ
- L1: 2.2 µH
- L2: 2.2 µH

**Ground**

- GND

**Feedback pin (FBx)**

- Make a single point connection from the signal ground to power ground.
Power button input to signal the COM Express Module the power button is pressed. Translate from PWRBTN signal to 3.3Vaux and 5Vaux signals using R86 and R87 when no power up or BIOS problems could occur.

Power OK input to signal the COM Express Module the 12V, 5V and 3.3V power supply are good. Translate from PWR_OK signal to 3.3Vaux and 5Vaux signals by P3V3AUX.

Power supply on. When the COM Express Module is a Type 6 and not in the 8V supplied, then the power supply on Module Type 6 has TYPE2# to GND and TYPE1# and TYPE0# not connected.

Standard Logic devices powered by P3V3AUX.

System reset button

System deep button