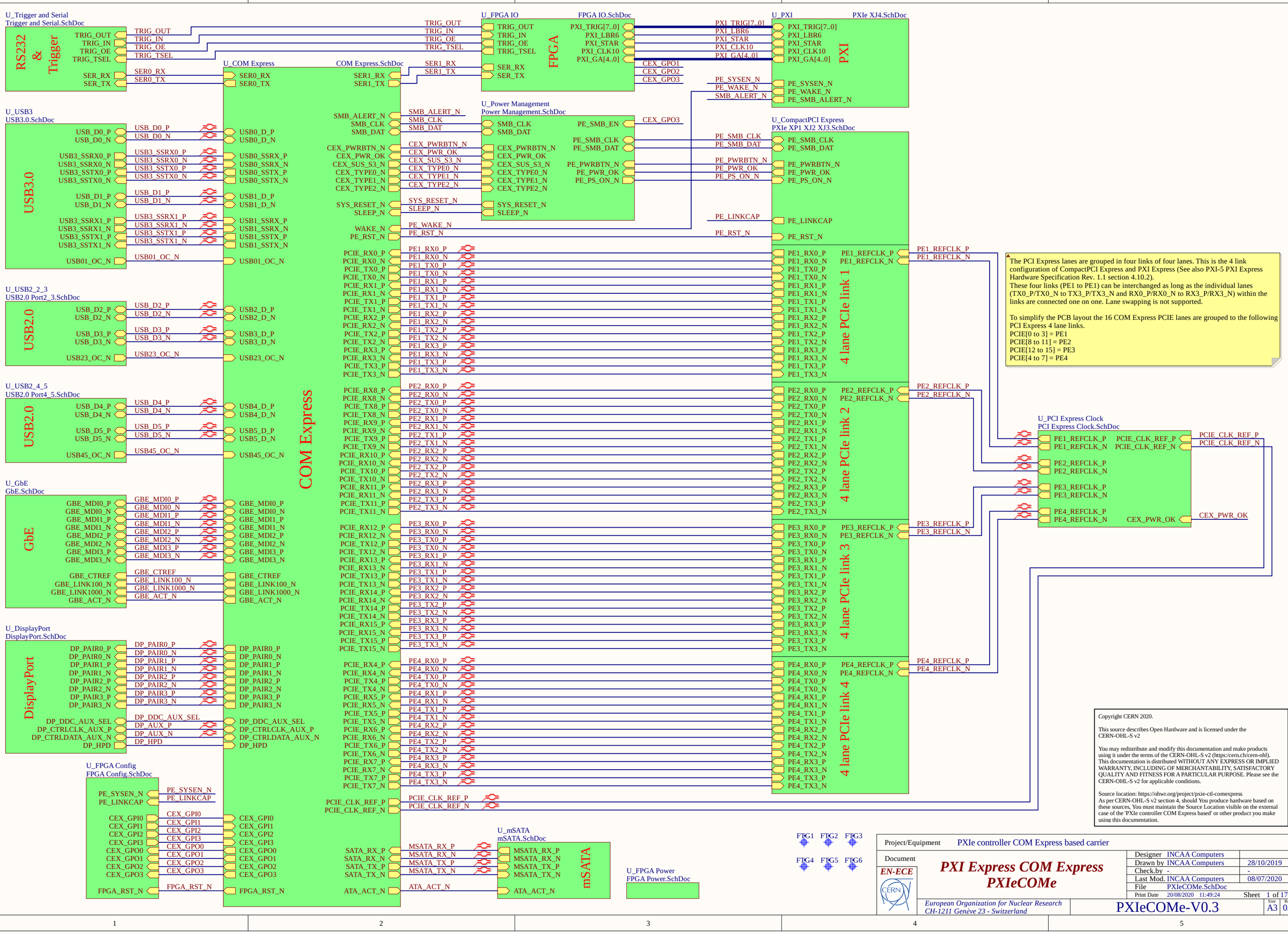
U_Trigger and Serial
Trigger and Serial.SchDoc
RS232 & Trigger
TRIG_OUT
TRIG_IN
TRIG_OE
TRIG_TSEL
SER_RX
SER_TX
U_COM Express
COM Express.SchDoc
SER0_RX
SER0_TX
SER1_RX
SER1_TX
U_FPGA IO
FPGA IO.SchDoc
FPGA
PXI_TRIG[7..0]
PXI_LBR6
PXI_STAR
PXI_CLK10
PXI_GA[4..0]
CEX_GPO1
CEX_GPO2
CEX_GPO3
U_PXI
PXIe XJ4.SchDoc
PXI
PE_SYSEN_N
PE_WAKE_N
SMB_ALERT_N
U_USB3
USB3.0.SchDoc
USB3.0
USB_D0_P
USB_D0_N
USB3_SSRX0_P
USB3_SSRX0_N
USB3_SSTX0_P
USB3_SSTX0_N
USB_D1_P
USB_D1_N
USB3_SSRX1_P
USB3_SSRX1_N
USB3_SSTX1_P
USB3_SSTX1_N
USB01_OC_N
U_Power Management
Power Management.SchDoc
SMB_CLK
SMB_DAT
PE_SMB_EN
CEX_PWRBTN_N
CEX_PWR_OK
CEX_SUS_S3_N
CEX_TYPE0_N
CEX_TYPE1_N
CEX_TYPE2_N
PE_PWRBTN_N
PE_PWR_OK
PE_PS_ON_N
SYS_RESET_N
SLEEP_N
U_CompactPCI Express
PXIe XP1 XJ2 XJ3.SchDoc
PE_SMB_CLK
PE_SMB_DAT
PE_LINKCAP
PE_RST_N
WAKE_N
PE_WAKE_N
U_USB2_2_3
USB2.0 Port2_3.SchDoc
USB2.0
USB_D2_P
USB_D2_N
USB_D3_P
USB_D3_N
USB23_OC_N
U_USB2_4_5
USB2.0 Port4_5.SchDoc
USB_D4_P
USB_D4_N
USB_D5_P
USB_D5_N
USB45_OC_N
U_GbE
GbE.SchDoc
GbE
GBE_MDI0_P
GBE_MDI0_N
GBE_MDI1_P
GBE_MDI1_N
GBE_MDI2_P
GBE_MDI2_N
GBE_MDI3_P
GBE_MDI3_N
GBE_CTREF
GBE_LINK100_N
GBE_LINK1000_N
GBE_ACT_N
U_DisplayPort
DisplayPort.SchDoc
DisplayPort
DP_PAIR0_P
DP_PAIR0_N
DP_PAIR1_P
DP_PAIR1_N
DP_PAIR2_P
DP_PAIR2_N
DP_PAIR3_P
DP_PAIR3_N
DP_DDC_AUX_SEL
DP_AUX_P
DP_AUX_N
DP_HPD
DP_CTRLCLK_AUX_P
DP_CTRLDATA_AUX_N
U_FPGA Config
FPGA Config.SchDoc
FPGA_RST_N
COM Express
PCIE_RX0_P
PCIE_RX0_N
PCIE_TX0_P
PCIE_TX0_N
PCIE_RX1_P
PCIE_RX1_N
PCIE_TX1_P
PCIE_TX1_N
PCIE_RX2_P
PCIE_RX2_N
PCIE_TX2_P
PCIE_TX2_N
PCIE_RX3_P
PCIE_RX3_N
PCIE_TX3_P
PCIE_TX3_N
PCIE_RX8_P
PCIE_RX8_N
PCIE_TX8_P
PCIE_TX8_N
PCIE_RX9_P
PCIE_RX9_N
PCIE_TX9_P
PCIE_TX9_N
PCIE_RX10_P
PCIE_RX10_N
PCIE_TX10_P
PCIE_TX10_N
PCIE_RX11_P
PCIE_RX11_N
PCIE_TX11_P
PCIE_TX11_N
PCIE_RX12_P
PCIE_RX12_N
PCIE_TX12_P
PCIE_TX12_N
PCIE_RX13_P
PCIE_RX13_N
PCIE_TX13_P
PCIE_TX13_N
PCIE_RX14_P
PCIE_RX14_N
PCIE_TX14_P
PCIE_TX14_N
PCIE_RX15_P
PCIE_RX15_N
PCIE_TX15_P
PCIE_TX15_N
PCIE_RX4_P
PCIE_RX4_N
PCIE_TX4_P
PCIE_TX4_N
PCIE_RX5_P
PCIE_RX5_N
PCIE_TX5_P
PCIE_TX5_N
PCIE_RX6_P
PCIE_RX6_N
PCIE_TX6_P
PCIE_TX6_N
PCIE_RX7_P
PCIE_RX7_N
PCIE_TX7_P
PCIE_TX7_N
PCIE_CLK_REF_P
PCIE_CLK_REF_N
4 lane PCIe link 1
4 lane PCIe link 2
4 lane PCIe link 3
4 lane PCIe link 4
PE1_RX0_P
PE1_RX0_N
PE1_TX0_P
PE1_TX0_N
PE1_RX1_P
PE1_RX1_N
PE1_TX1_P
PE1_TX1_N
PE1_RX2_P
PE1_RX2_N
PE1_TX2_P
PE1_TX2_N
PE1_RX3_P
PE1_RX3_N
PE1_TX3_P
PE1_TX3_N
PE1_REFCLK_P
PE1_REFCLK_N
PE2_RX0_P
PE2_RX0_N
PE2_TX0_P
PE2_TX0_N
PE2_RX1_P
PE2_RX1_N
PE2_TX1_P
PE2_TX1_N
PE2_RX2_P
PE2_RX2_N
PE2_TX2_P
PE2_TX2_N
PE2_RX3_P
PE2_RX3_N
PE2_TX3_P
PE2_TX3_N
PE2_REFCLK_P
PE2_REFCLK_N
PE3_RX0_P
PE3_RX0_N
PE3_TX0_P
PE3_TX0_N
PE3_RX1_P
PE3_RX1_N
PE3_TX1_P
PE3_TX1_N
PE3_RX2_P
PE3_RX2_N
PE3_TX2_P
PE3_TX2_N
PE3_RX3_P
PE3_RX3_N
PE3_TX3_P
PE3_TX3_N
PE3_REFCLK_P
PE3_REFCLK_N
PE4_RX0_P
PE4_RX0_N
PE4_TX0_P
PE4_TX0_N
PE4_RX1_P
PE4_RX1_N
PE4_TX1_P
PE4_TX1_N
PE4_RX2_P
PE4_RX2_N
PE4_TX2_P
PE4_TX2_N
PE4_RX3_P
PE4_RX3_N
PE4_TX3_P
PE4_TX3_N
PE4_REFCLK_P
PE4_REFCLK_N
U_PCI Express Clock
PCI Express Clock.SchDoc
PCIE_CLK_REF_P
PCIE_CLK_REF_N
CEX_PWR_OK
U_mSATA
mSATA.SchDoc
mSATA
SATA_RX_P
SATA_RX_N
SATA_TX_P
SATA_TX_N
MSATA_RX_P
MSATA_RX_N
MSATA_TX_P
MSATA_TX_N
ATA_ACT_N
U_FPGA Power
FPGA Power.SchDoc
FTG1
FTG2
FTG3
FTG4
FTG5
FTG6
The PCI Express lanes are grouped in four links of four lanes. This is the 4 link configuration of CompactPCI Express and PXI Express (See also PXI-5 PXI Express Hardware Specification Rev. 1.1 section 4.10.2).
These four links (PE1 to PE1) can be interchanged as long as the individual lanes (TX0_P/TX0_N to TX3_P/TX3_N and RX0_P/RX0_N to RX3_P/RX3_N) within the links are connected one on one. Lane swapping is not supported.
To simplify the PCB layout the 16 COM Express PCIE lanes are grouped to the following PCI Express 4 lane links.
PCIE[0 to 3] = PE1
PCIE[8 to 11] = PE2
PCIE[12 to 15] = PE3
PCIE[4 to 7] = PE4
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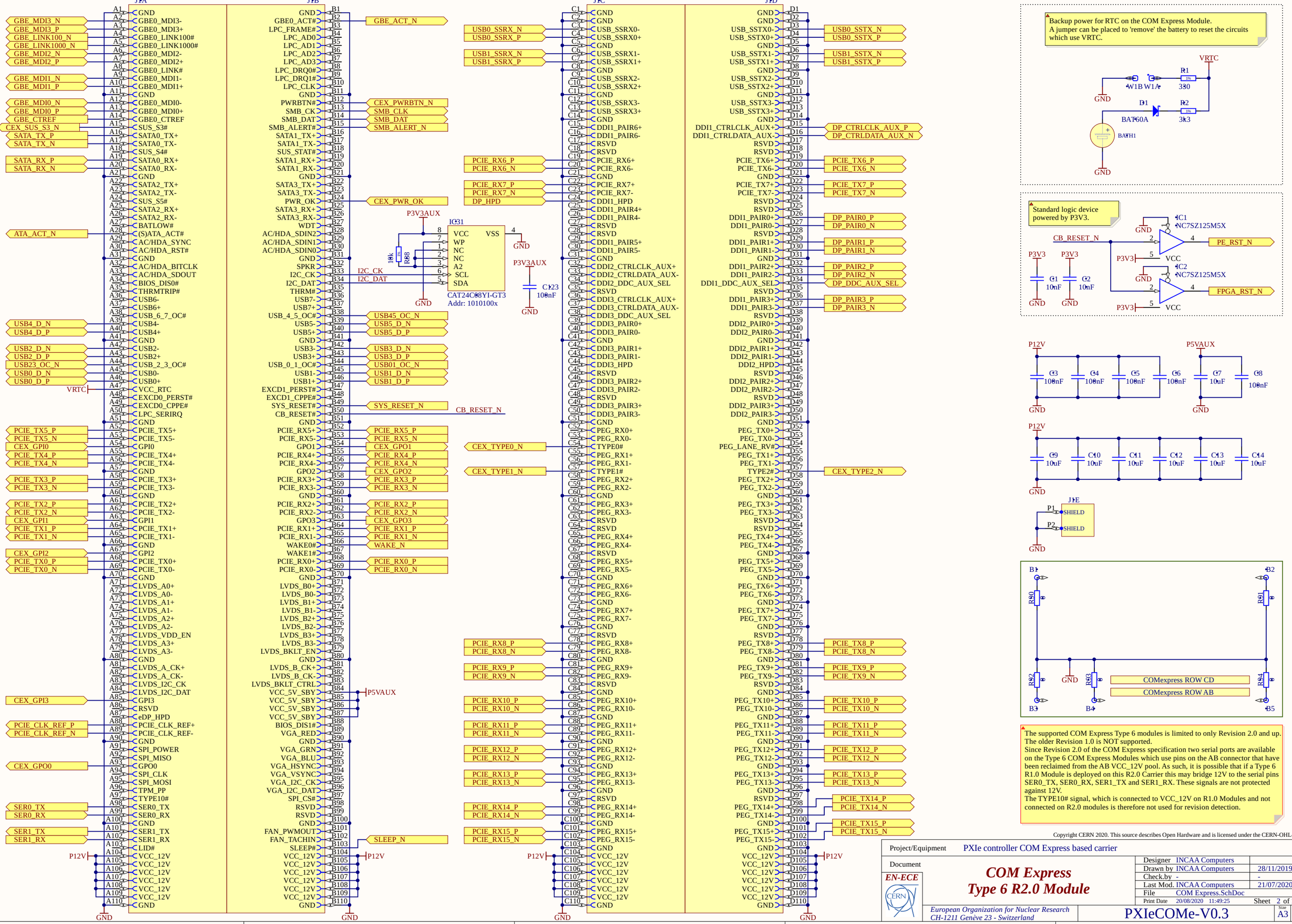
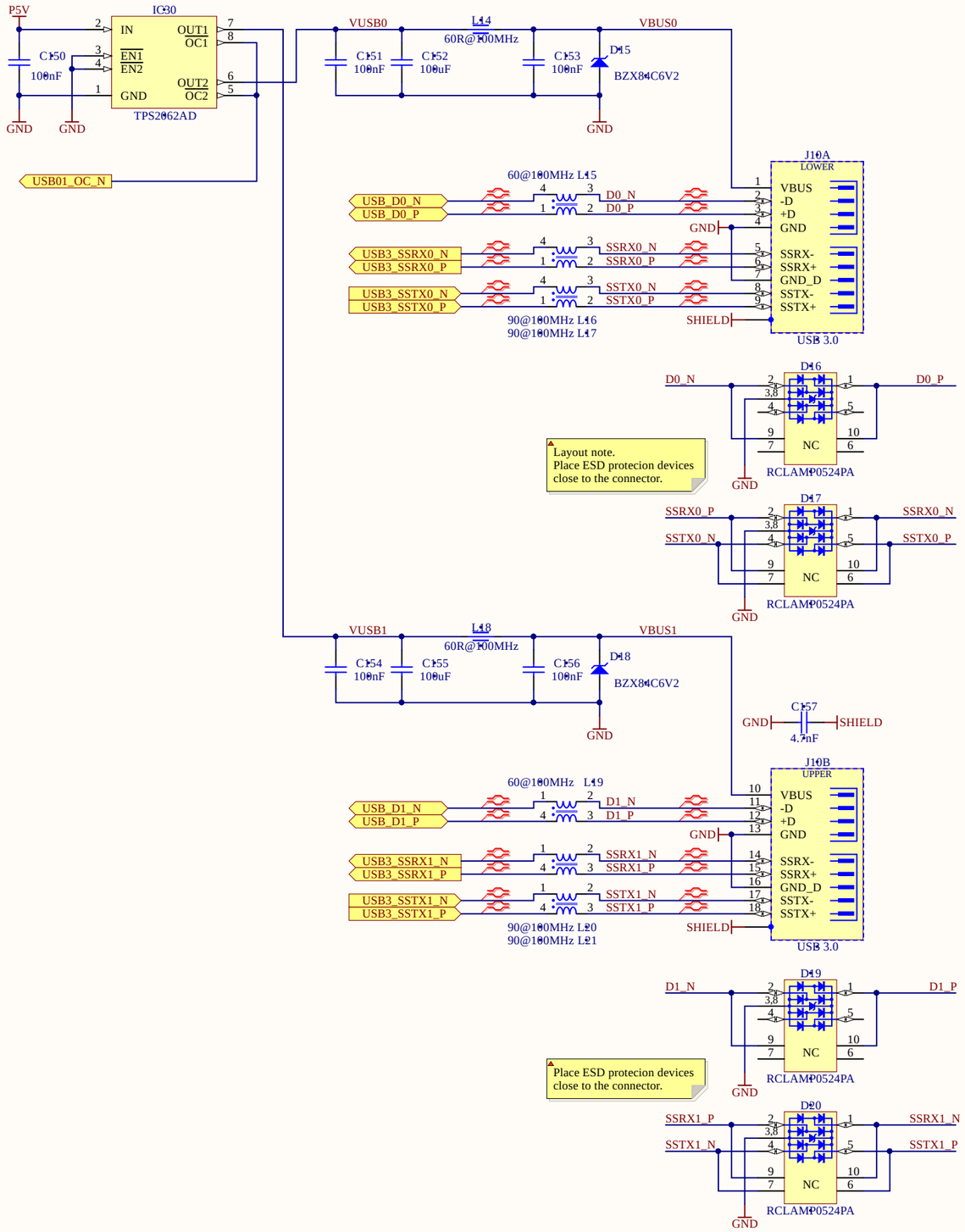
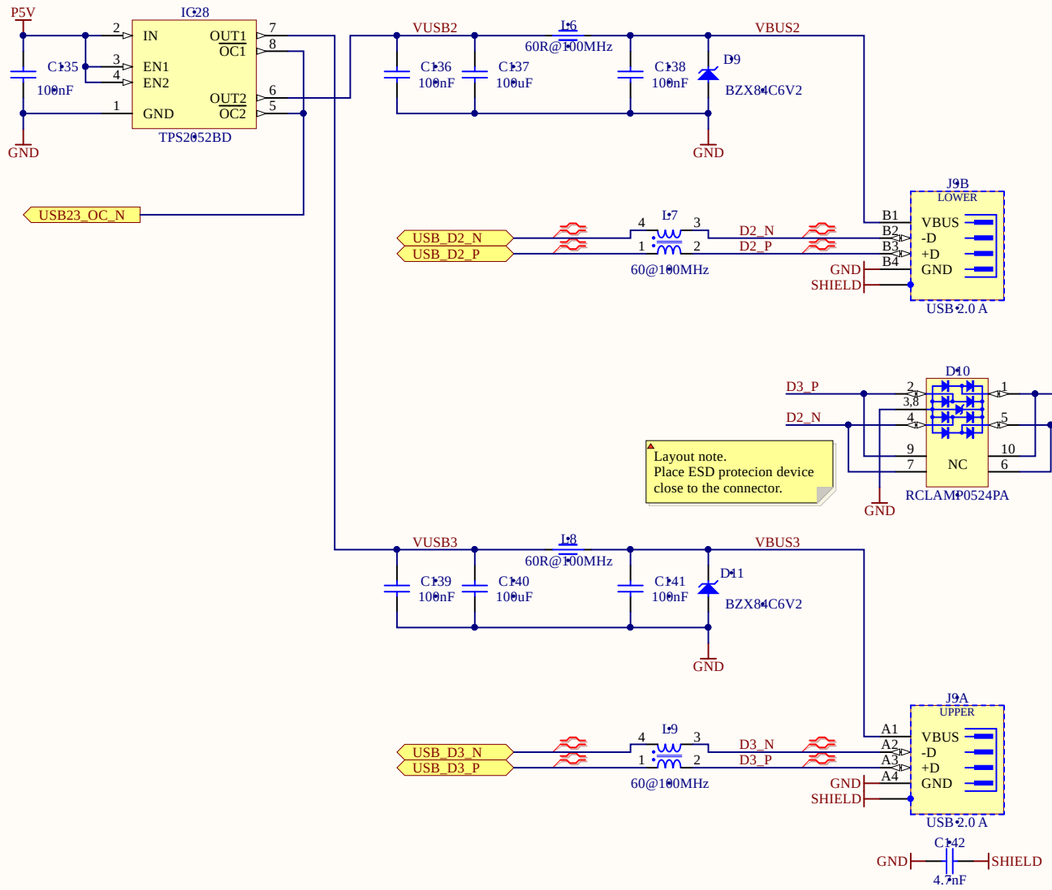
Source location: https://ohwr.org/project/pxie-ctl-comexpress
As per CERN-OHL-S v2 section 4, should You produce hardware based on these sources, You must maintain the Source Location visible on the external case of the 'PXIe controller COM Express based' or other product you make using this documentation.
Project/Equipment
PXIe controller COM Express based carrier
Document
EN-ECE
PXI Express COM Express
PXIeCOMe
Designer INCAA Computers
Drawn by INCAA Computers 28/10/2019
Check.by -
Last Mod. INCAA Computers 08/07/2020
File PXIeCOMe.SchDoc
Print Date 20/08/2020 11:49:24
Sheet 1 of 17
European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland
PXIeCOMe-V0.3
Size A3
Rev 0.3



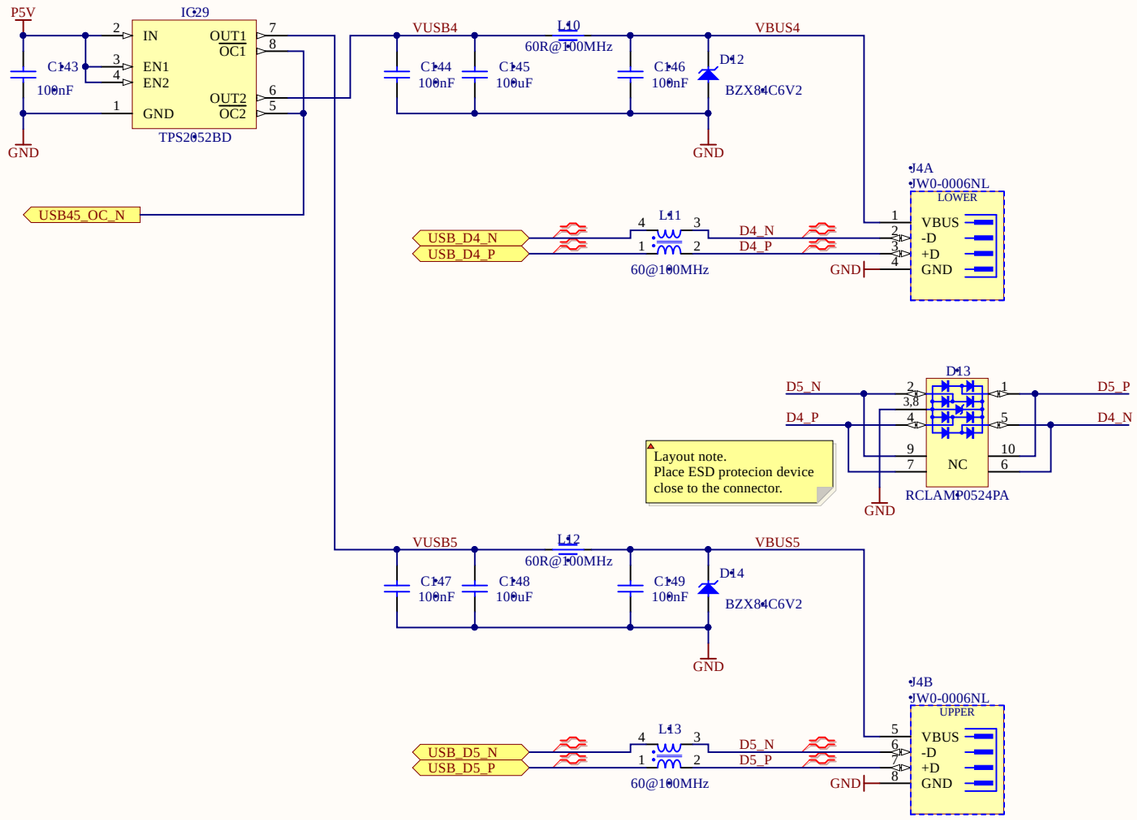
Project/Equipment	PXIe controller COM Express based carrier		
Document	**COM Express Type 6 R2.0 Module**	Designer	INCAA Computers
EN-ECE		Drawn by	INCAA Computers 28/11/2019
		Check.by	- -
		Last Mod.	INCAA Computers 21/07/2020
		File	COM Express.SchDoc
		Print Date	20/08/2020 11:49:25 Sheet 2 of 17
European Organization for Nuclear Research *CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size	A3 Rev 0.3



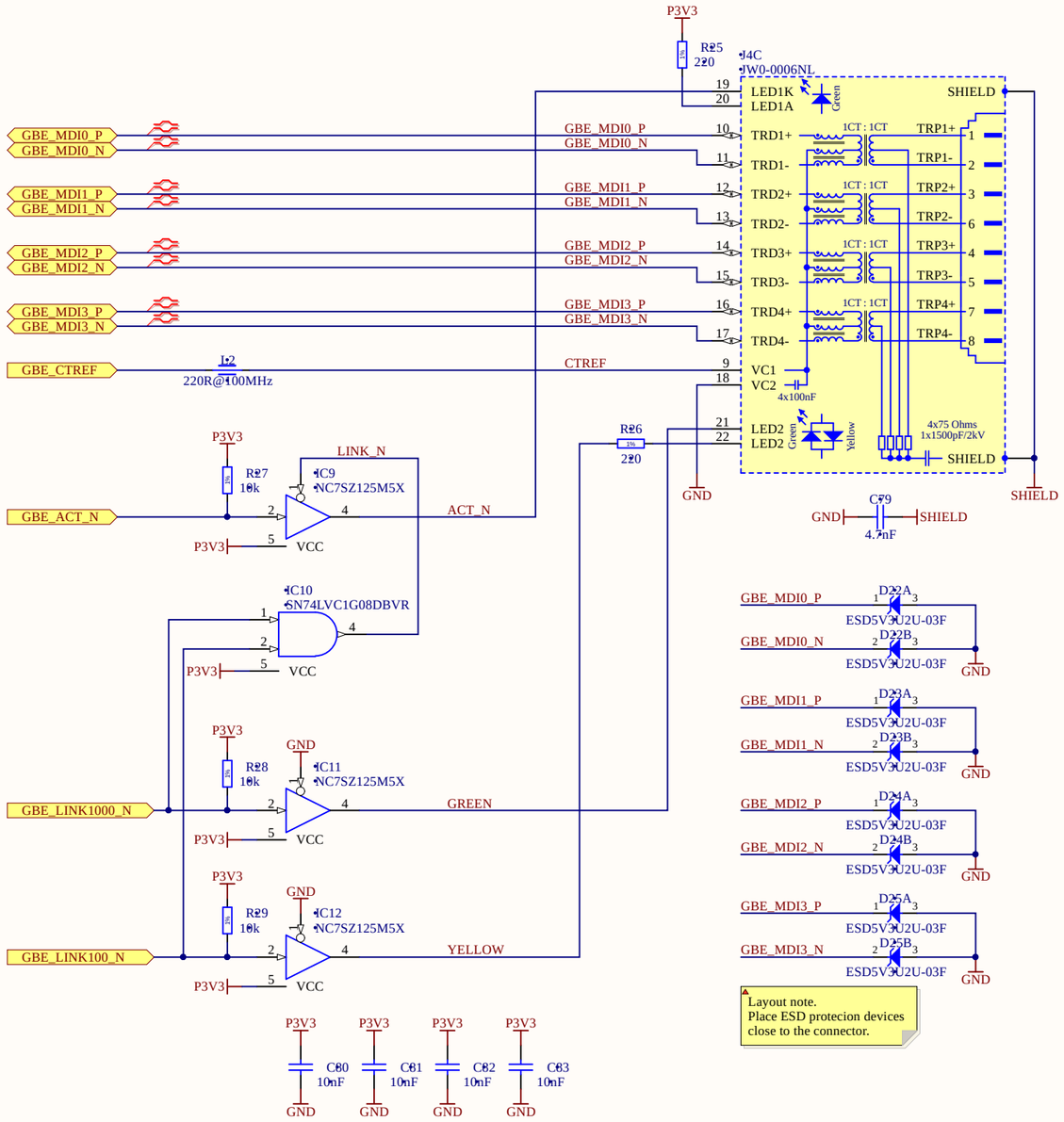
Project/Equipment	PXIe controller COM Express based carrier		
Document	***USB 3.0 Port 0 and 1***	Designer	INCAA Computers
		Drawn by	INCAA Computers 29/10/2019
		Check.by	- -
		Last Mod.	INCAA Computers 15/07/2020
		File	USB3.0.SchDoc
		Print Date	20/08/2020 11:49:26 Sheet 3 of 17
EN-ECE	*European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3



Project/Equipment	PXIe controller COM Express based carrier		
Document	***USB 2.0 Port 2 and 3***	Designer	INCAA Computers
		Drawn by	INCAA Computers 29/10/2019
		Check.by	- -
		Last Mod.	INCAA Computers 15/07/2020
		File	USB2.0 Port2_3.SchDoc
		Print Date	20/08/2020 11:49:26 Sheet 4 of 17
EN-ECE	*European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3



Project/Equipment	PXIe controller COM Express based carrier		
Document	***USB 2.0 Port 4 and 5***	Designer	INCAA Computers
		Drawn by	INCAA Computers 29/10/2019
		Check.by	- -
		Last Mod.	INCAA Computers 15/07/2020
		File	USB2.0 Port4_5.SchDoc
		Print Date	20/08/2020 11:49:26 Sheet 5 of 17
EN-ECE	*European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3



Project/Equipment	PXIe controller COM Express based carrier		
Document	**Gigabit Ethernet**	Designer	INCAA Computers
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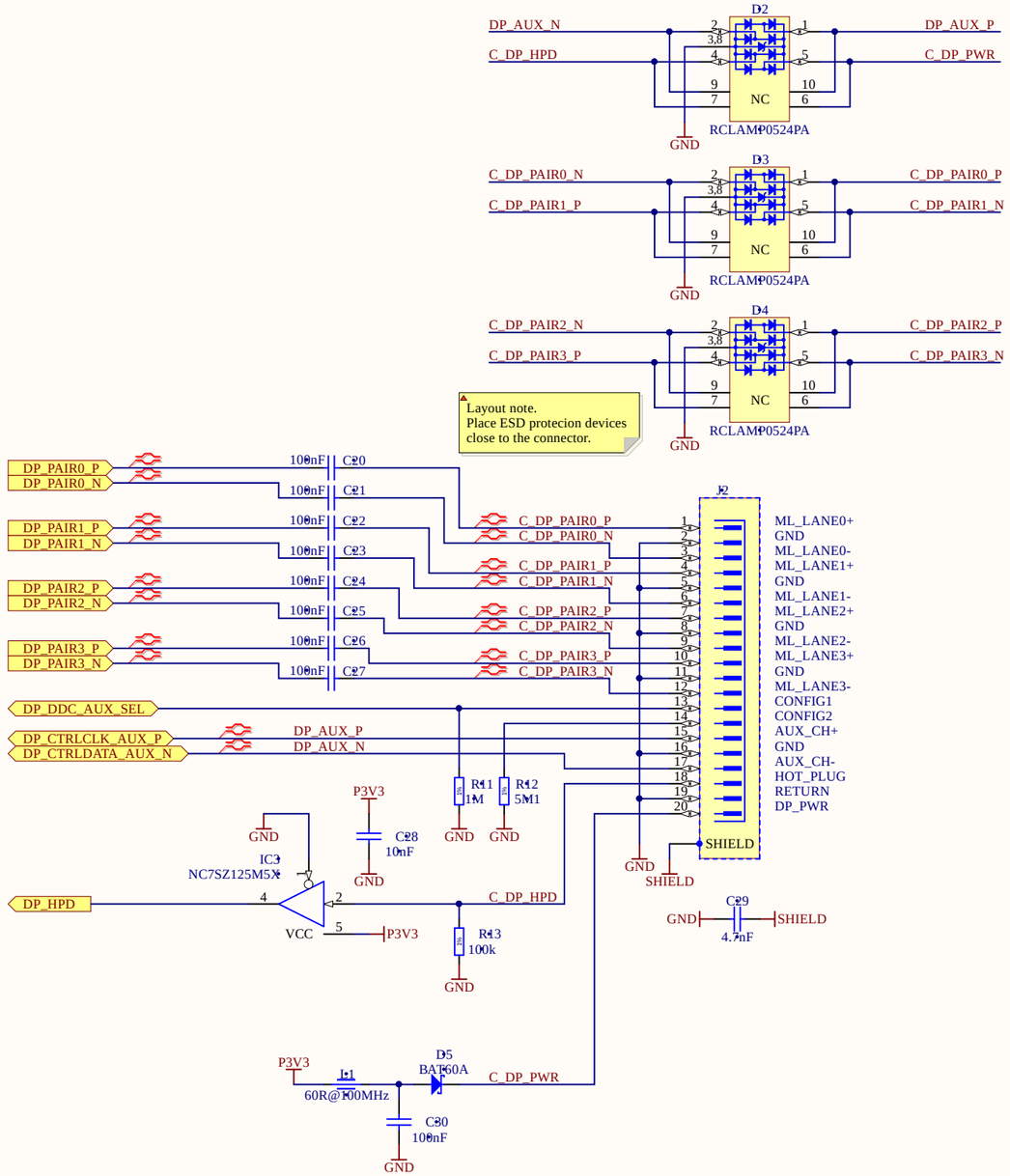
		Check.by	- -
		Last Mod.	INCAA Computers 14/07/2020
		File	GbE.SchDoc
		Print Date	20/08/2020 11:49:26 Sheet 6 of 17
EN-ECE	*European Organization for Nuclear Research* *CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3



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Document	**DisplayPort**	Designer	INCAA Computers
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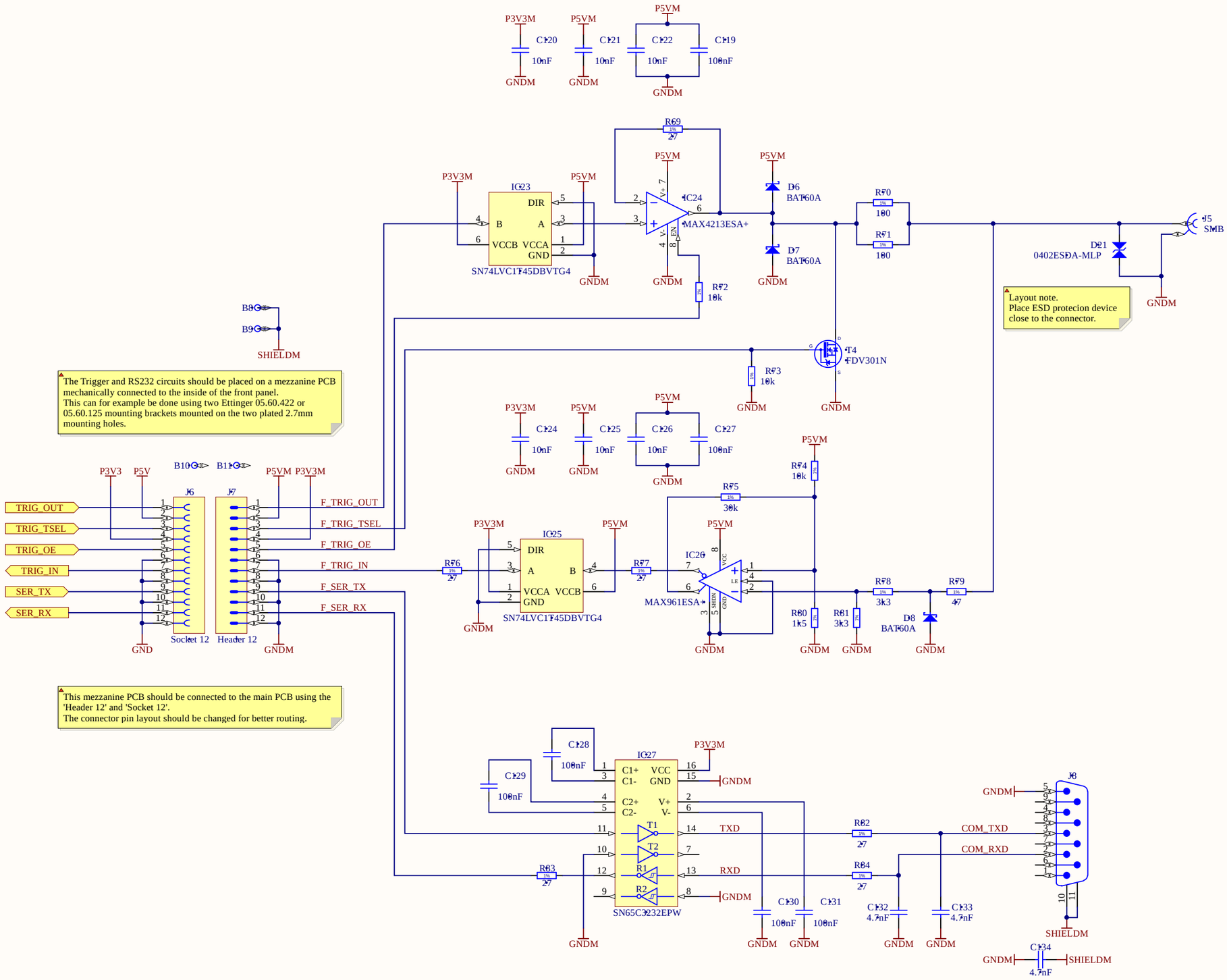
EN-ECE		Check.by	- -
		Last Mod.	INCAA Computers 15/07/2020
		File	DisplayPort.SchDoc
		Print Date	20/08/2020 11:49:26 Sheet 7 of 17
European Organization for Nuclear Research *CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size	A3
		Rev	0.3



Project/Equipment	PXIe controller COM Express based carrier		
Document	**Trigger and Serial Mezzanine board**	Designer	INCAA Computers
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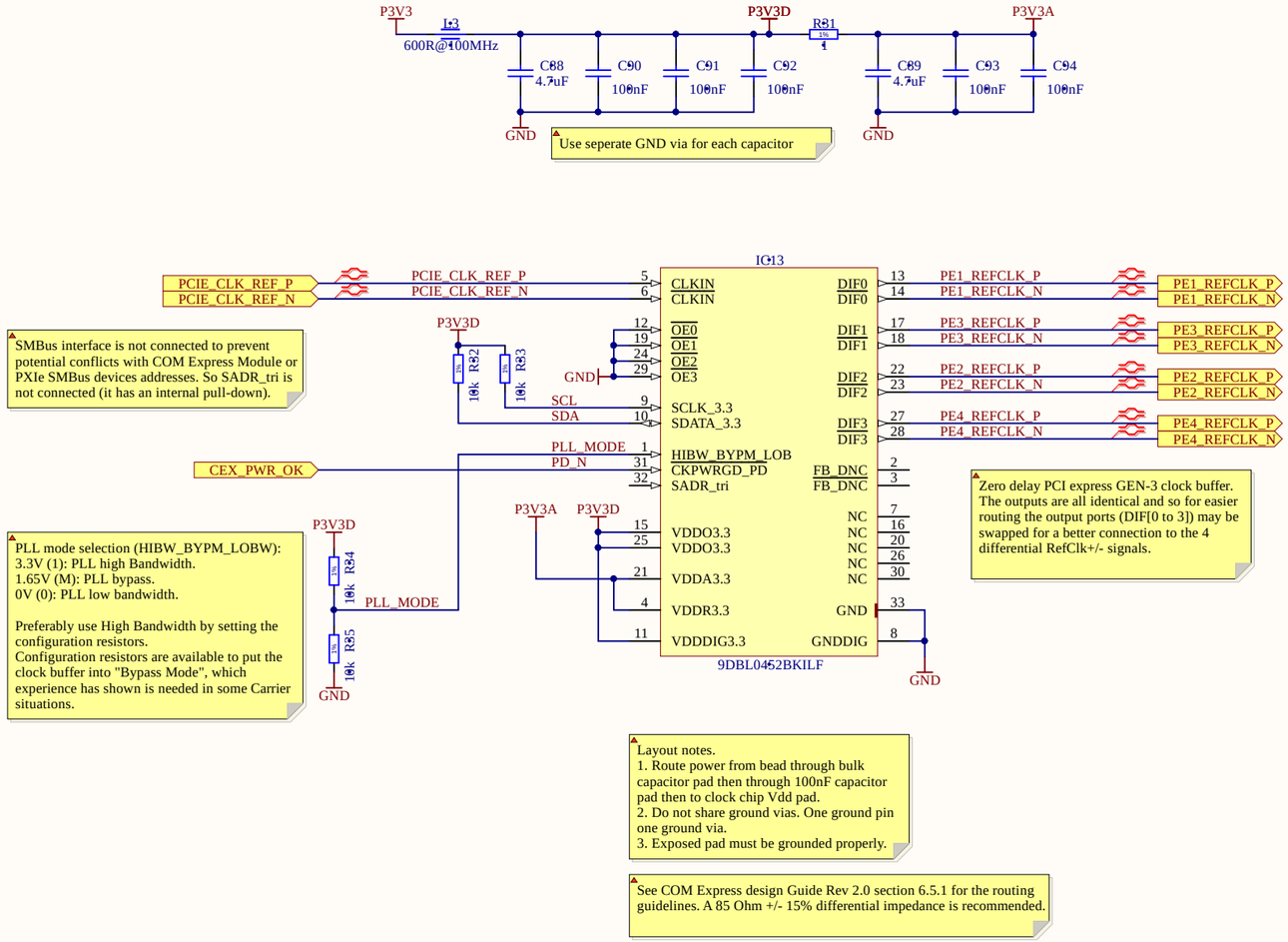
		Check.by	- -
		Last Mod.	INCAA Computers 24/06/2020
		File	Trigger and Serial.SchDoc
		Print Date	20/08/2020 11:49:27 Sheet 8 of 17
EN-ECE	*European Organization for Nuclear Research* *CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3



Project/Equipment	PXIe controller COM Express based carrier		
Document	**PCI Express Clock Zero Delay Buffer**	Designer	INCAA Computers
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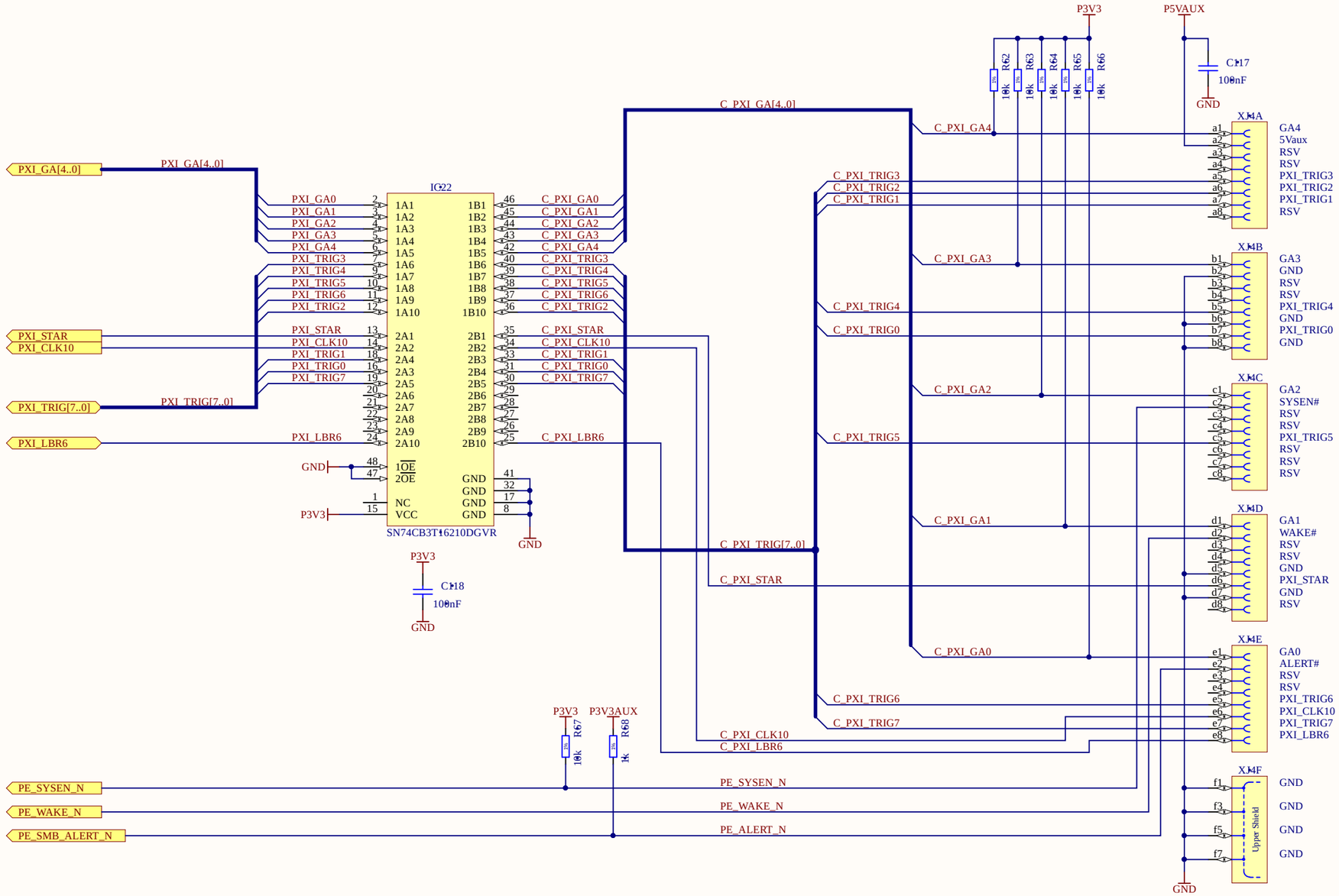
		Check.by	- -
		Last Mod.	INCAA Computers 02/07/2020
		File	PCI Express Clock.SchDoc
		Print Date	20/08/2020 11:49:27 Sheet 9 of 17
EN-ECE	*European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3



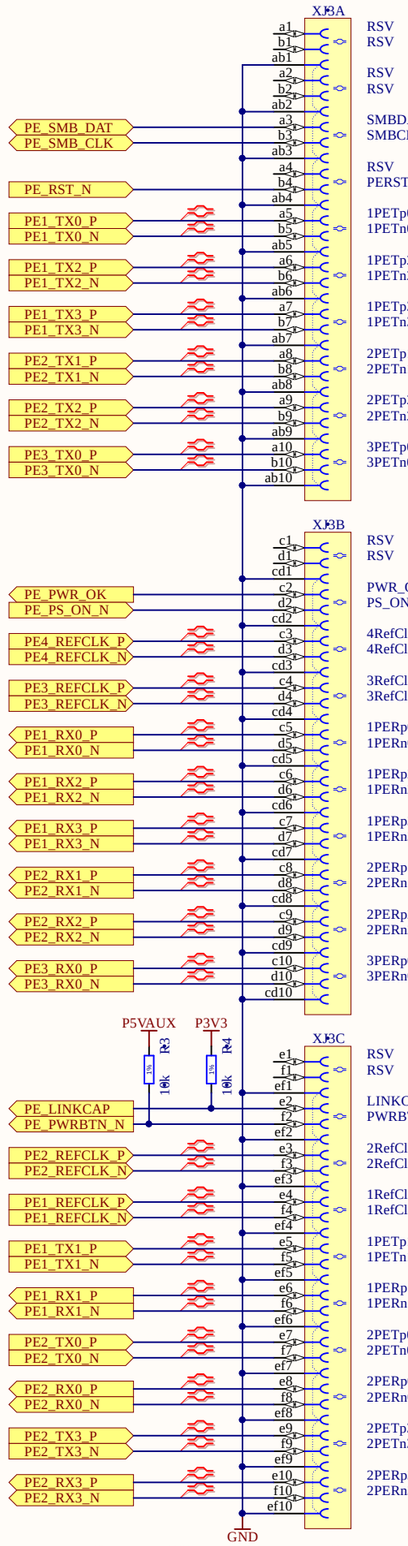
Project/Equipment	PXIe controller COM Express based carrier		
Document	**PXI Express XJ4 PXI**	Designer	INCAA Computers
		Drawn by	INCAA Computers 30/10/2019
		Check.by	- -
		Last Mod.	INCAA Computers 15/06/2020
		File	PXIe XJ4.SchDoc
		Print Date	20/08/2020 11:49:27 Sheet 10 of 17
EN-ECE	*European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3

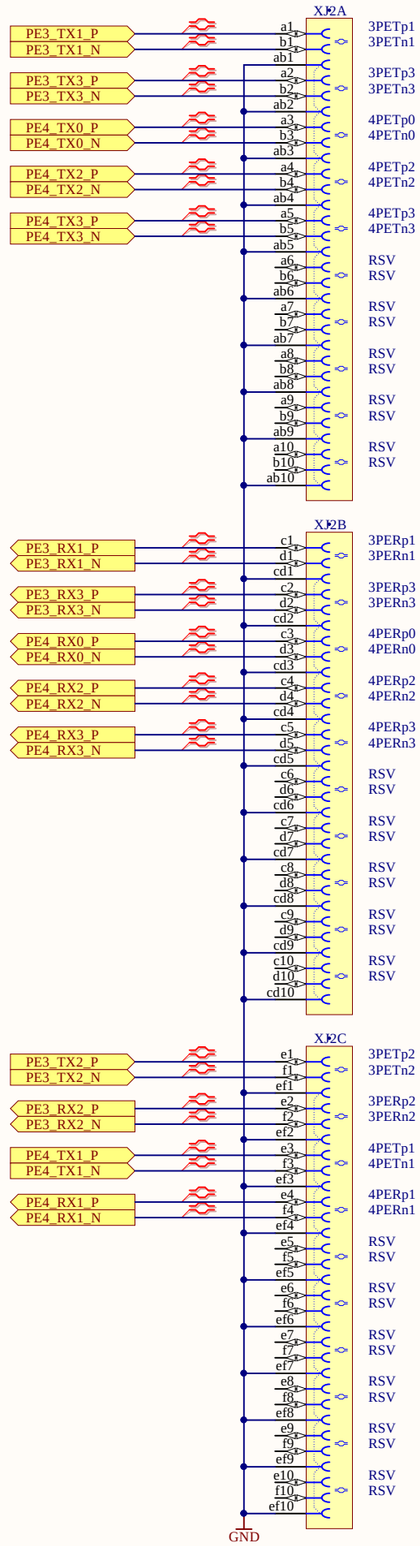
The PCI Express transmit coupling capacitors are already part of the COM Express module.
See COM Express design Guide Rev 2.0 section 2.3.4

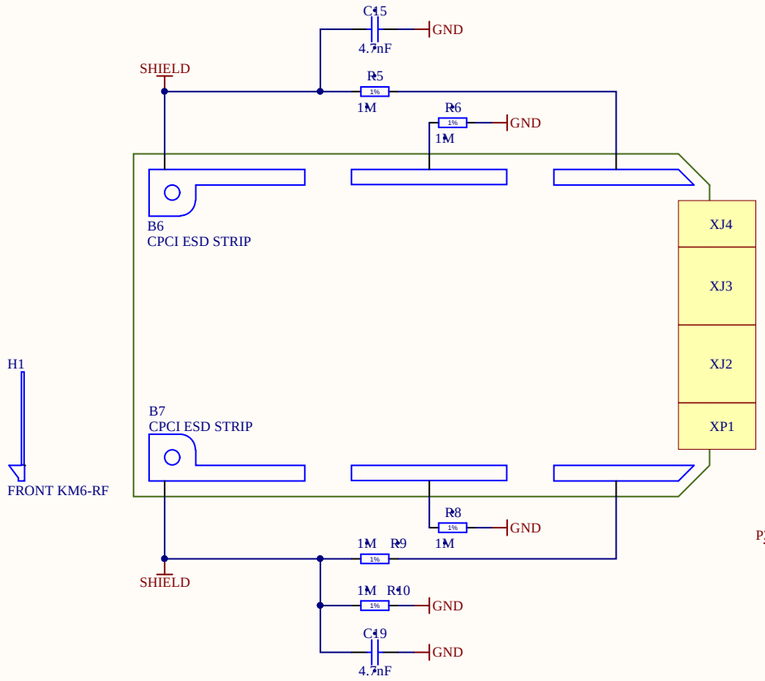
The PCI Express receive inputs on the COM Express (xPERp[3:0]/xPERn[3:0]) can be connected using either the advertised polarity, or an inverted polarity. Inverted polarity may be chosen in order to simplify the PCB layout by avoiding signal crossover and additional vias.
See COM Express design Guide Rev 2.0 sections 2.3.6.1 and 2.4.4.1

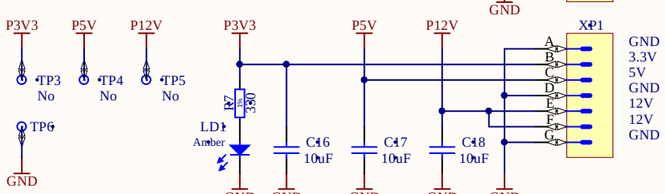
The PCI Express lanes are grouped in four links of four lanes. This is the 4 link configuration of CompactPCI Express and PXI Express (See also PXI-5 PXI Express Hardware Specification Rev. 1.1 section 4.10.2).
These four links (1PE to 4PE) can be interchanged as long as the individual lanes (Tp0/Tn0 to Tp3/Tn3 and Rp0/Rn0 to Rp3/Rn3) within the links are connected one on one. Lane swapping is not supported.

See COM Express design Guide Rev 2.0 section 6.5.1 for the routing guidelines. A 85 Ohm +/- 15% differential impedance is recommended.

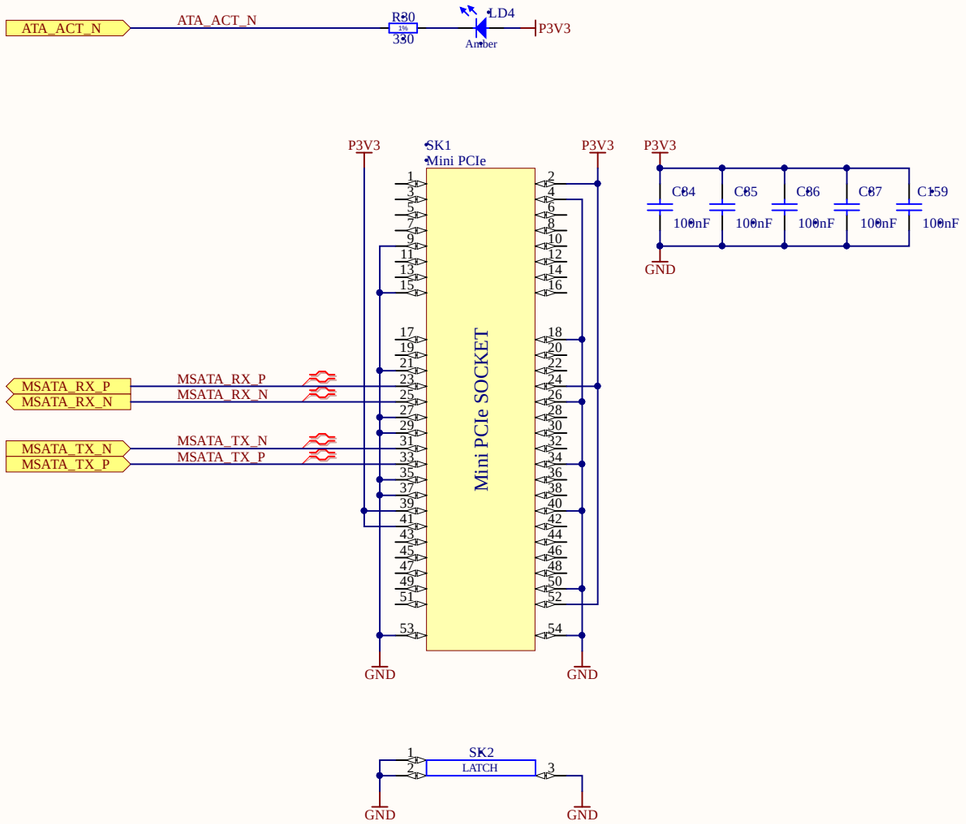








Project/Equipment	PXIe controller COM Express based carrier
Document	**PXI Express XP1, XJ2, XJ3 CompactPCI Express**
EN-ECE	
Designer	INCAA Computers
Drawn by	INCAA Computers 07/11/2019
Check.by	- -
Last Mod.	INCAA Computers 30/06/2020
File	PXIe XP1 XJ2 XJ3.SchDoc
Print Date	20/08/2020 11:49:27 Sheet 11 of 17
European Organization for Nuclear Research, CH-1211 Genève 23 - Switzerland	PXIeCOMe-V0.3 Size A3 Rev 0.3



Project/Equipment	PXIe controller COM Express based carrier		
Document	***mSATA SSD memory card***	Designer	INCAA Computers
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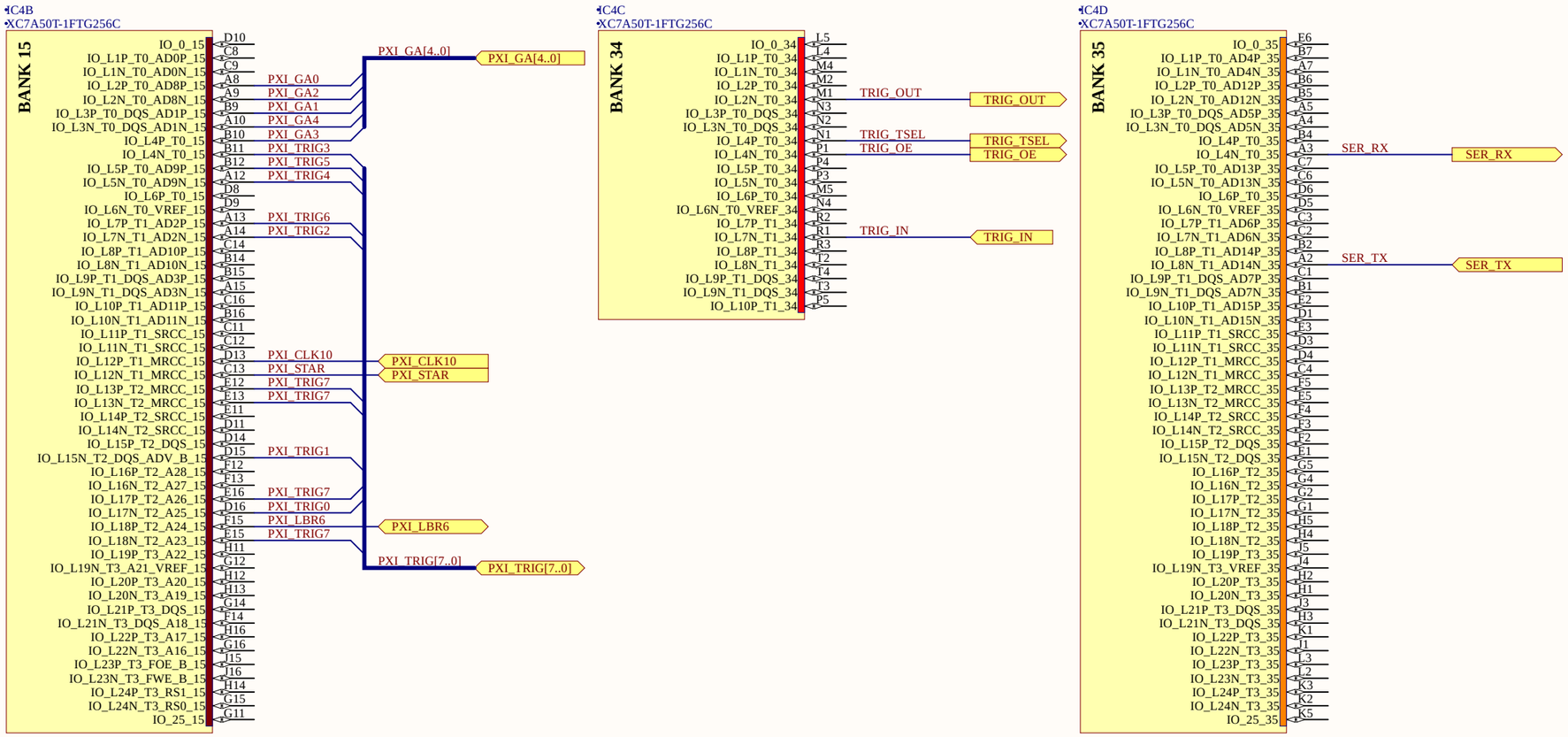
		Last Mod.	INCAA Computers 15/06/2020
		File	mSATA.SchDoc
		Print Date	20/08/2020 11:49:28 Sheet 12 of 17
EN-ECE	*European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3



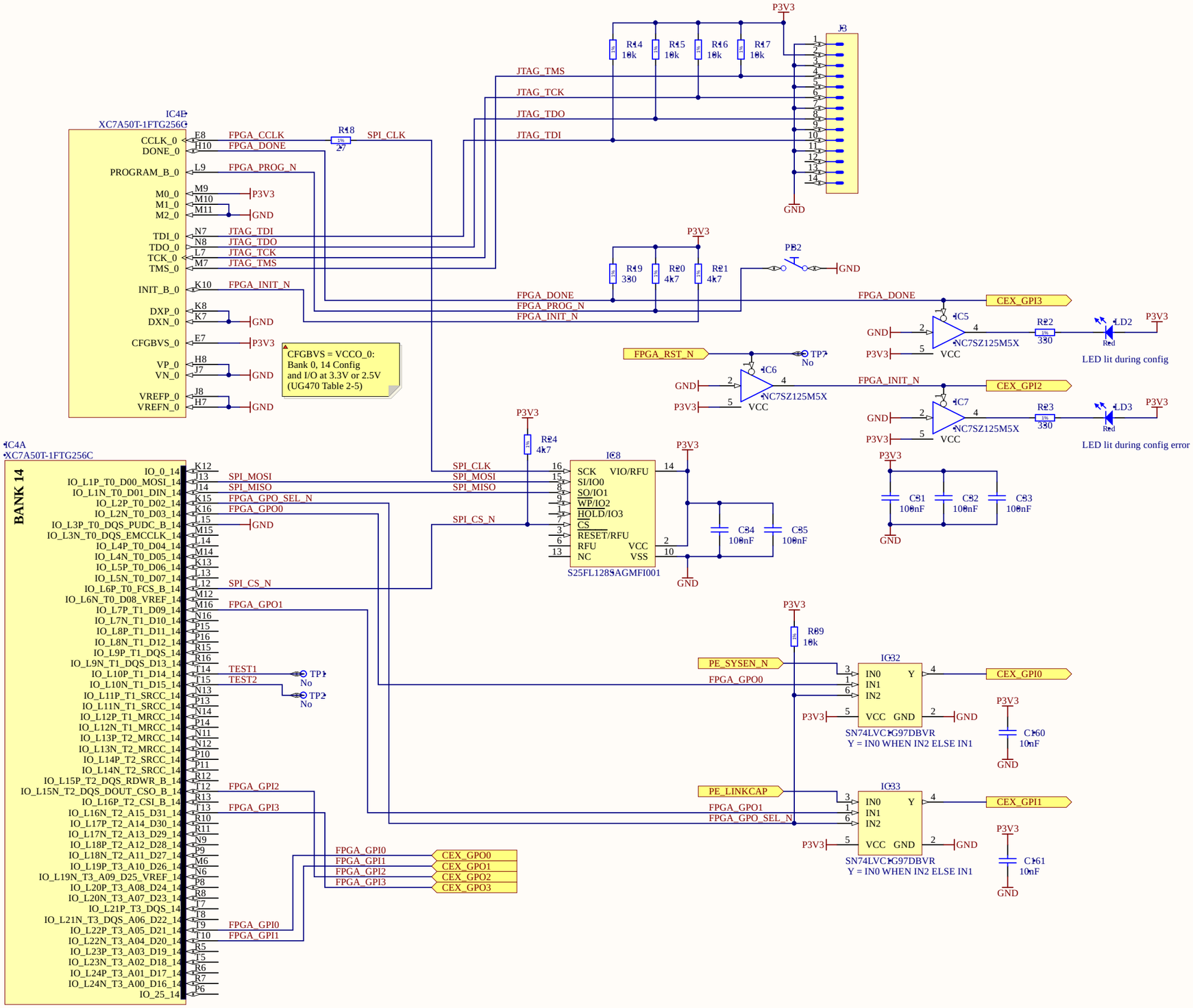
PXI_STAR should be attached to a FPGA I/O pads which is also a MRCC capable input.

PXI_CLK10 should be attached to a FPGA I/O pads which is also a MRCC capable input.

PXI_TRIG7 should be attached to four FPGA I/O pads of which one is also a MRCC capable input.
As an PXI_TRIG7 input only one of these four (the MRCC capable input) is needed.
As an PXI_TRIG7 output all four have to switch simultaniously to be able to source a minimum of 75mA.
This can be achieved by selecting LVCMOS33 outputs with two outputs driving 24mA and two 16mA.

PXI Hardware Specification Revision 2.2:
RECOMMENDATION: Type A drivers SHOULD be used for clock transmission over the PXI trigger bus. Type A drivers are capable of incident wave switching on rising edges, preventing jitter degradation due to transmission line effects.
Switching voltage high Vsoh(AC) = 2.3 V (min)
High source current Ioh(AC) = 75mA (min) @Vsoh(AC)

Project/Equipment	PXIe controller COM Express based carrier		
Document	**PXI Trigger Controller I/O**	Designer	INCAA Computers
		Drawn by	INCAA Computers 11/11/2019
		Check.by	- -
		Last Mod.	INCAA Computers 09/07/2020
		File	FPGA IO.SchDoc
		Print Date	20/08/2020 11:49:28 Sheet 13 of 17
EN-ECE	*European Organization for Nuclear Research* *CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3



Project/Equipment	PXIe controller COM Express based carrier		
Document	**PXI Trigger Controller Configuration**	Designer	INCAA Computers
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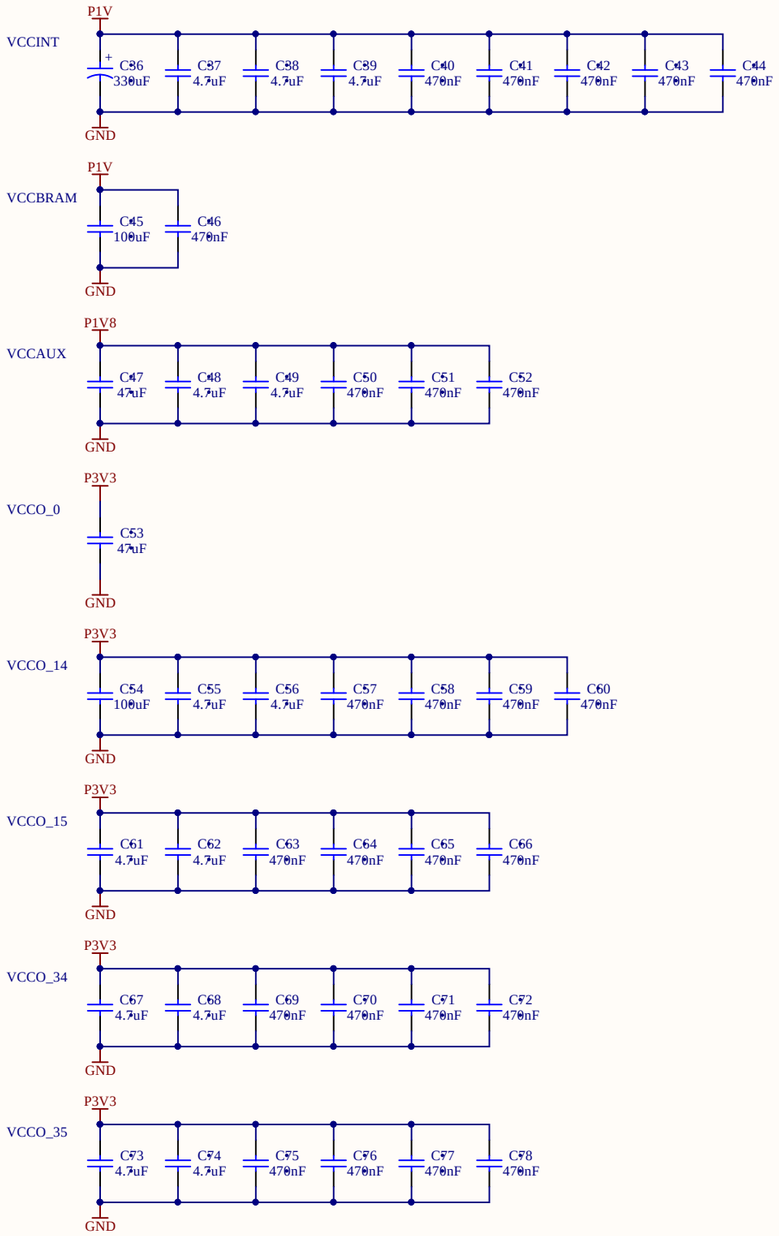
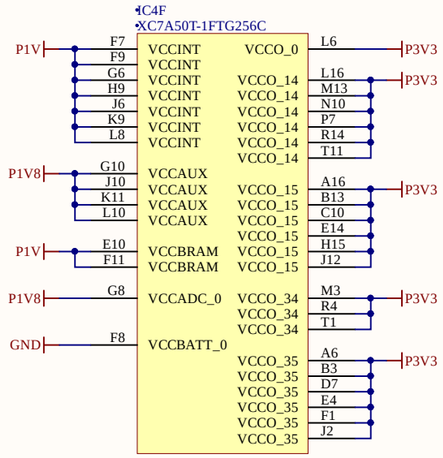
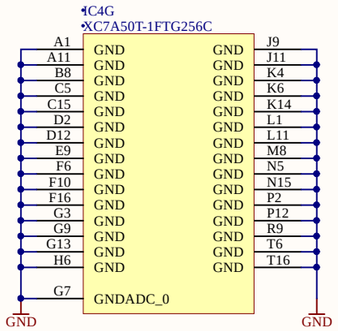
		Check.by	- -
		Last Mod.	INCAA Computers 09/07/2020
		File	FPGA Config.SchDoc
		Print Date	20/08/2020 11:49:28 Sheet 14 of 17
EN-ECE	*European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3



PCB Decoupling Capacitors according to 7 series FPGAs PCB Design Guide UG483 (v1.13) August 18, 2017, Table 2-2.





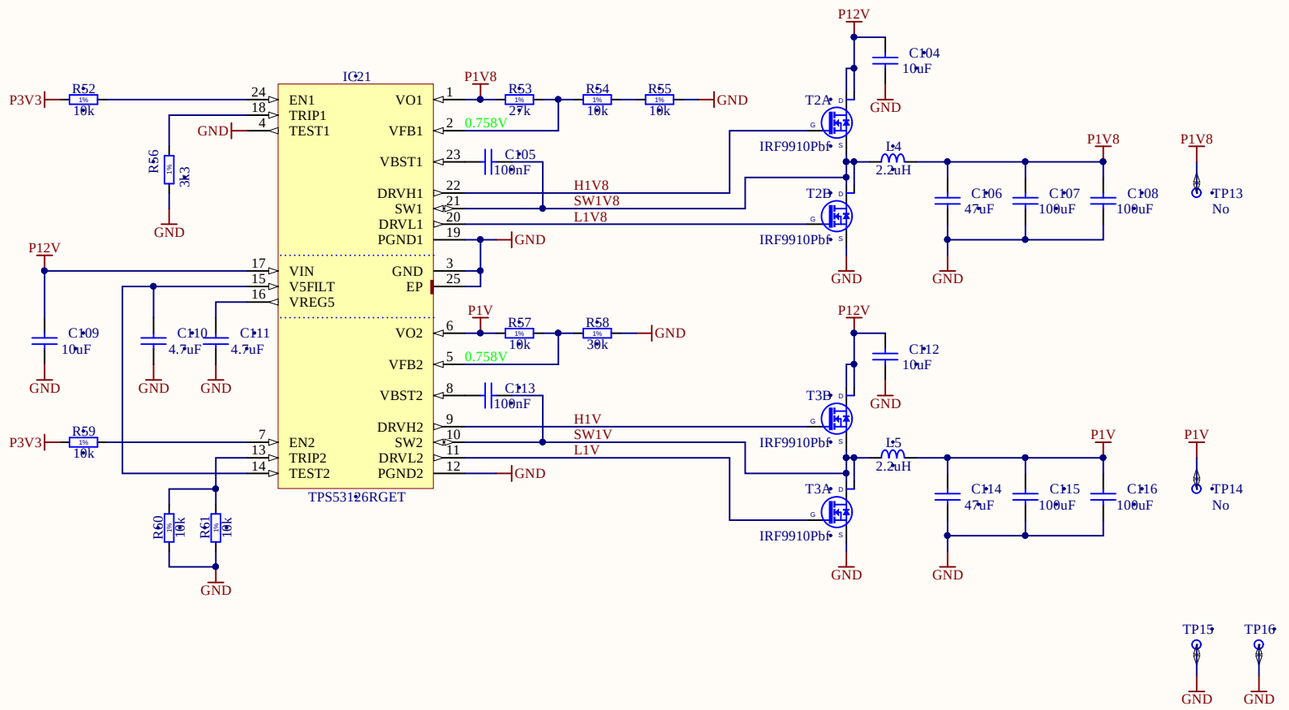
U_Power Supply
Power Supply.SchDoc

Project/Equipment	PXIe controller COM Express based carrier		
Document	***PXI Trigger Controller Power***	Designer	INCAA Computers
		Drawn by	INCAA Computers 11/11/2019
		Check.by	- -
		Last Mod.	INCAA Computers 15/06/2020
		File	FPGA Power.SchDoc
		Print Date	20/08/2020 11:49:29 Sheet 15 of 17
EN-ECE	*European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3

DC/DC calculations,Voripple=10mV
The over current protection for the inductor L is set to about 3A .

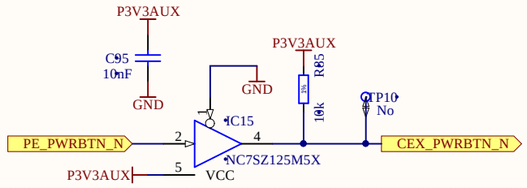
Fsw=700kHz
Rds(on)= typ value at Tj=25°C (because of the ambient temperature and the operational dissipation the Tj will not be expected to be lower)
Itrip=11.5uA(max)
Rtrip is calculated
1.0V, Imax=3A, L=1.5uH, Rtrip=5017 -> 10k//10k, C=15.6uF, ILpeak=4.31A
1.8V, Imax=3A, L=1.5uH, Rtrip=3393 -> 3300, C=26.0uF, ILpeak=5.19A

LAYOUT NOTES:
· Place the input capacitor close to the top switching FET. The output current loop should also be kept as small as possible.
· Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions Kelvin connections should be brought from the output to the feedback pin (FBx) of the device.
· Make a single point connection from the signal ground to power ground
· Do not allow switching current to flow under the device

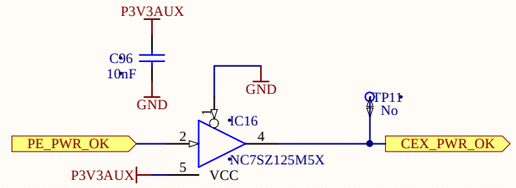


Project/Equipment	PXIe controller COM Express based carrier		
Document	**Switching Regulator 1.8V and 1.0V**	Designer INCAA Computers	
EN-ECE		Drawn by INCAA Computers	08/11/2019
		Check.by -	-
		Last Mod. INCAA Computers	15/06/2020
		File Power Supply.SchDoc	
		Print Date 20/08/2020 11:49:29	Sheet 16 of 17
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	PXIeCOMe-V0.3	Size A3	Rev 0.3

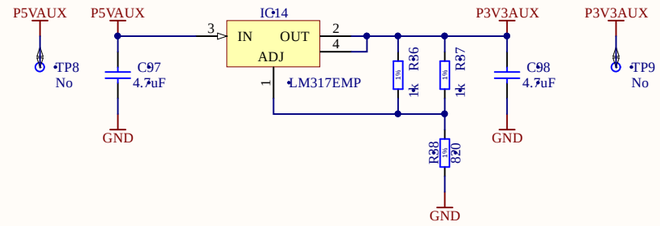
Power button input to signal the COM Express Module the power button in pressed.
Translate from 5Vaux signal to 3.3Vaux.



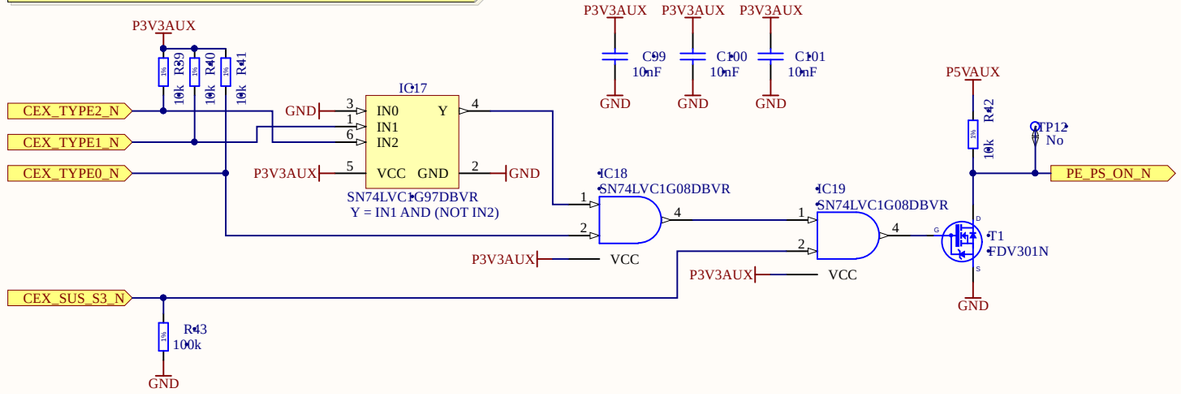
Power OK input to signal the COM Express Module the 12V, 5V and 3.3V power supply are good.
Translate from 5Vaux signal to 3.3Vaux.



LDO for 3.3Vaux standby power supply



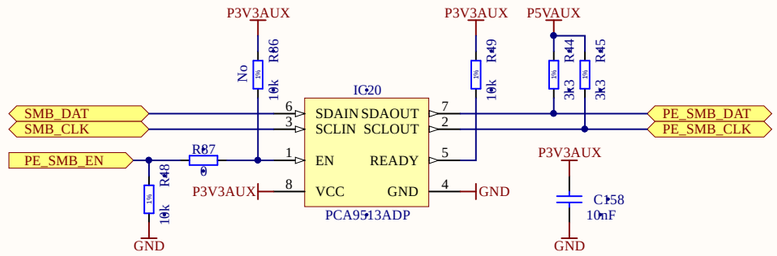
Power supply on. When the COM Express Module is a Type 6 and not in the S3 suspend stated, turn the power supply on.
Module Type 6 has TYPE2# to GND and TYPE1# and TYPE0# not connected



PICMG EXP.O 3.14:
There shall be a SMBus buffer device on the system board that has 2mA rise time accelerator capability.

A 3.3kOhm Pull-up to 5Vaux shall be used on SMBDAT and SMBCLK on the system board.

The 92 uA current source at SCLIN and SDAIN for PICMG applications, is placed at the COM Express side to not intervene with this specification for the system board. PXIe peripheral boards should have the SCLIN and SDAIN connected to the backplane.

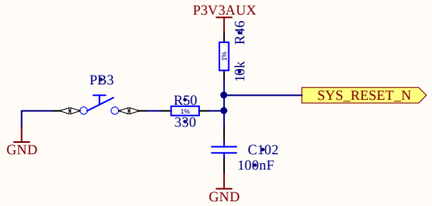


COM Express design Guide Rev 2.0 section 2.19.2.
"The SMBus should be connected to all or none of the PCIe/PCI devices and slots. A general recommendation is to not connect these devices to the SMBus."
Since the SMBus is mainly used by BIOS and power management purposes a potential SMBus address conflict between the SMBus devices on the COM Express module and devices on the external PXIe peripherals, can be seen als the source of this recommendation.

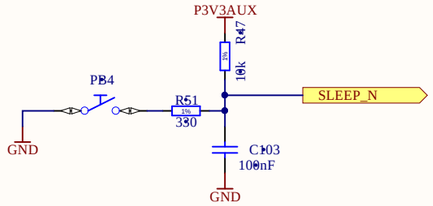
The PICMG EXP.O 3.1.4 however specifies the SMBus is required for System Boards.

To overcome this problem and still be able to use the PXIe SMBus it can be enabled using a COM Express GPO.
Or by placing and removing the resitors R86 and R87 when no power up or BIOS problems could occur.

System reset button



System sleep button



Project/Equipment	PXIe controller COM Express based carrier		
Document	**Power Management On/Off/Standby and SMBus**	Designer	INCAA Computers
		Drawn by	INCAA Computers 27/11/2019
		Check.by	- -
		Last Mod.	INCAA Computers 21/07/2020
		File	Power Management.SchDoc
		Print Date	20/08/2020 11:49:29 Sheet 17 of 17
EN-ECE	*European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland*	PXIeCOMe-V0.3	Size A3 Rev 0.3