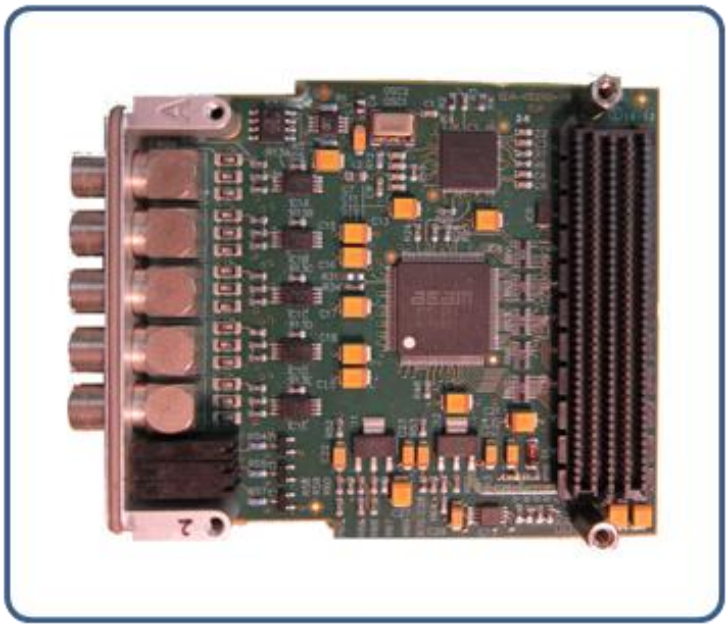
TDC Production Test Suite

User Guide



CERN | March 2013 | Version 1.0 | E.Gousiou

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Introduction 1

Welcome to the Production Test Suite for TDC boards, TDC PTS!

The TDC PTS is the environment designed for the functionality tests of the TDC mezzanine boards (EDA-02290) at the manufacturing site, right after production. It assures that the boards comply with a minimum set of quality rules in terms of soldering, mounting and PCBs fabrication process.

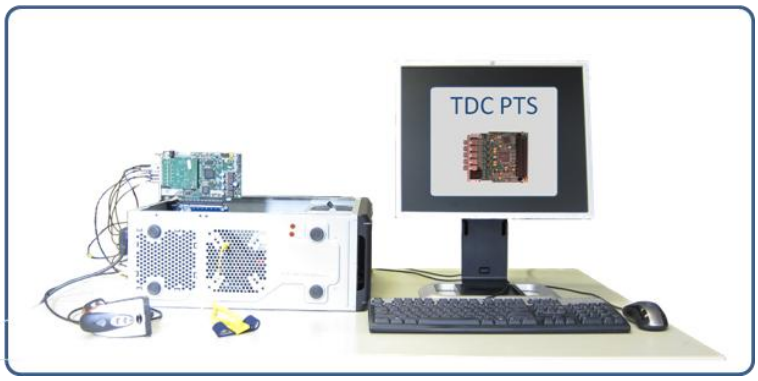


Figure 1: TDC PTS view

The main elements of the TDC PTS are listed in Table 1.

Item	Comments
Computer	power cord provided
Monitor	not provided
Keyboard, Mouse	not provided
Barcode reader	
ESD strap	
PCIe Extender board	screws for mounting in the computer provided
SPEC board	screws for mounting the TDC mezzanine on provided
SPEC-Fine Delay board	
5 LEMO cables	
Documentation	this user guide plus a one-page testing procedure

Table 1: TDC PTS elements

A TDC mezzanine board is tested while mounted on a SPEC carrier board, as figure 2 shows. The SPEC carrier board provides access to the PCIe interface of the computer. The computer hosts the TDC PTS software which provides the automated testing environment.

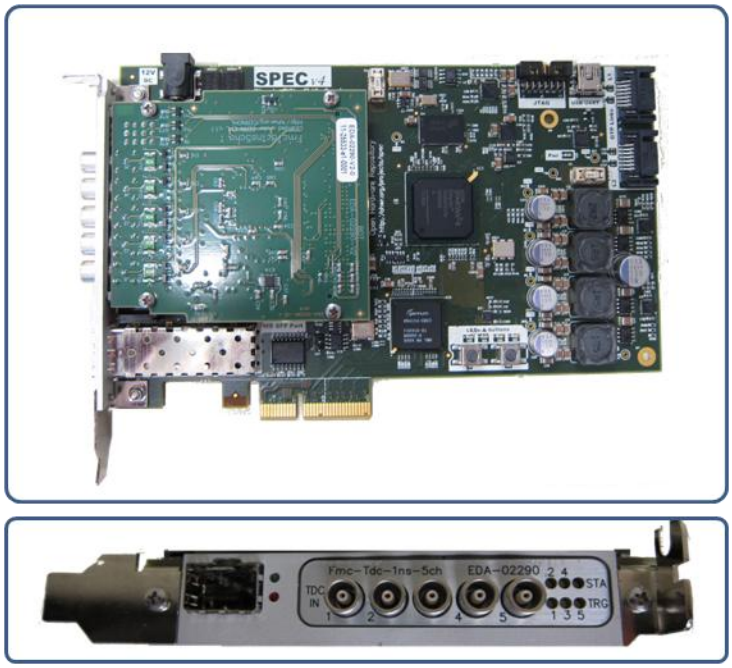


Figure 2: SPEC-TDC combination

To facilitate the testing setup a PCIe extender board is provided. The extender board is mounted and screwed on a PCIe slot of the computer; then the SPEC carrier board is easily mounted on the extender.

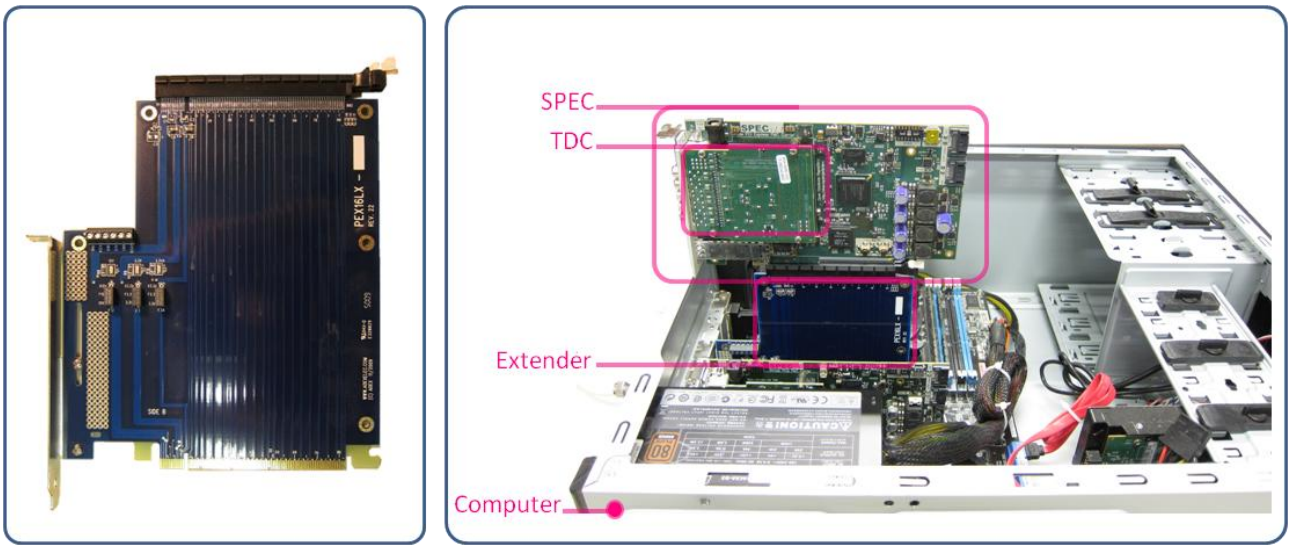


Figure 3: PCIe extender board

A SPEC-Fine Delay combination is used as pulse generator for the testing.

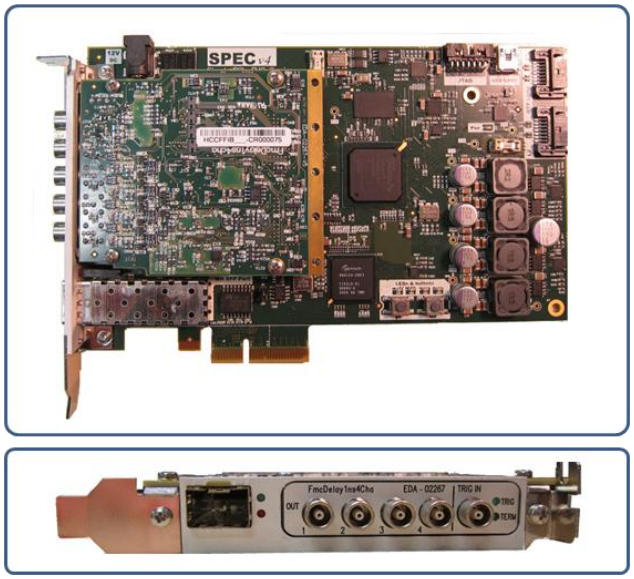


Figure 4: SPEC-Fine Delay combination, used as pulse generator

A set of LEMO cables is provided to connect the five TDC input channels to the four Fine Delay output channels; TDC channels 4 and 5 are connected to the same Fine Delay output.

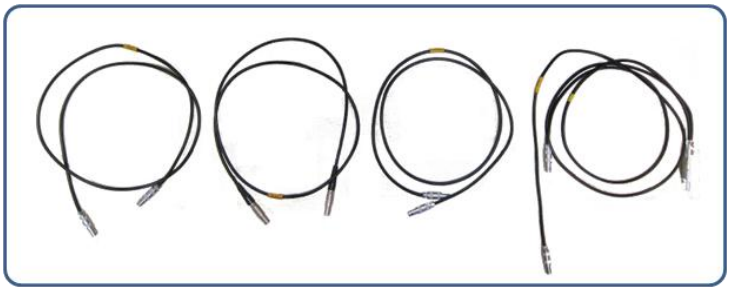


Figure 5: LEMO cables

In terms of software, the computer is equipped with the following:

- Ubuntu Linux, with kernel 2.6.38 or higher
- Python 2.7
- The PTS environment installed
- Driver gnurabbit installed

The user login is the following:

- Username: user
- Password: baraka

The computer should not be connected to the network and no updates should be allowed.

The duration of the test of a TDC board is five minutes.

Briefly, the operator needs to:

- mount the board on the **SPEC carrier**
- plug the SPEC carrier on the **extender**
- connect the provided **cables** between the TDC and the **Fine Delay**
- run the **software**

At the end of the test the operator receives a PASS/FAIL notification. In case of a FAILED board, information is provided on the failing components.

All test results are automatically saved in a folder on the computer.

For a FAILED board, you can repeat the test only one more time! If a board FAILs twice, please report to the CERN responsible.

TDC Board 2

The Time to Digital Converter board, TDC (EDA-02290) is an FMC mezzanine board with five input channels. It houses the Time to Digital Converter chip ACAM and it can calculate time differences between pulses arriving on the different channels.

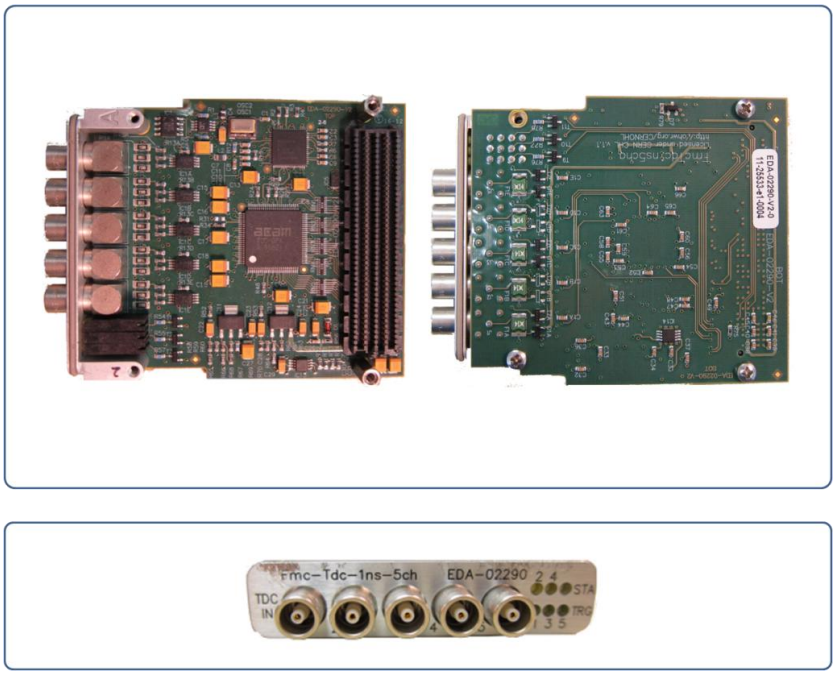


Figure 6: Top, bottom and front views of the TDC board

Figure 7 shows the main parts of the board.

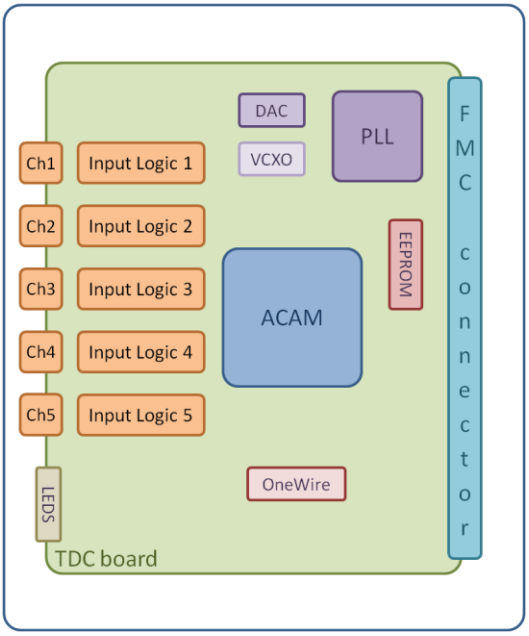


Figure 7: Basic parts of the TDC board

The following picture shows in detail the location of the components of the TDC tested by PTS.

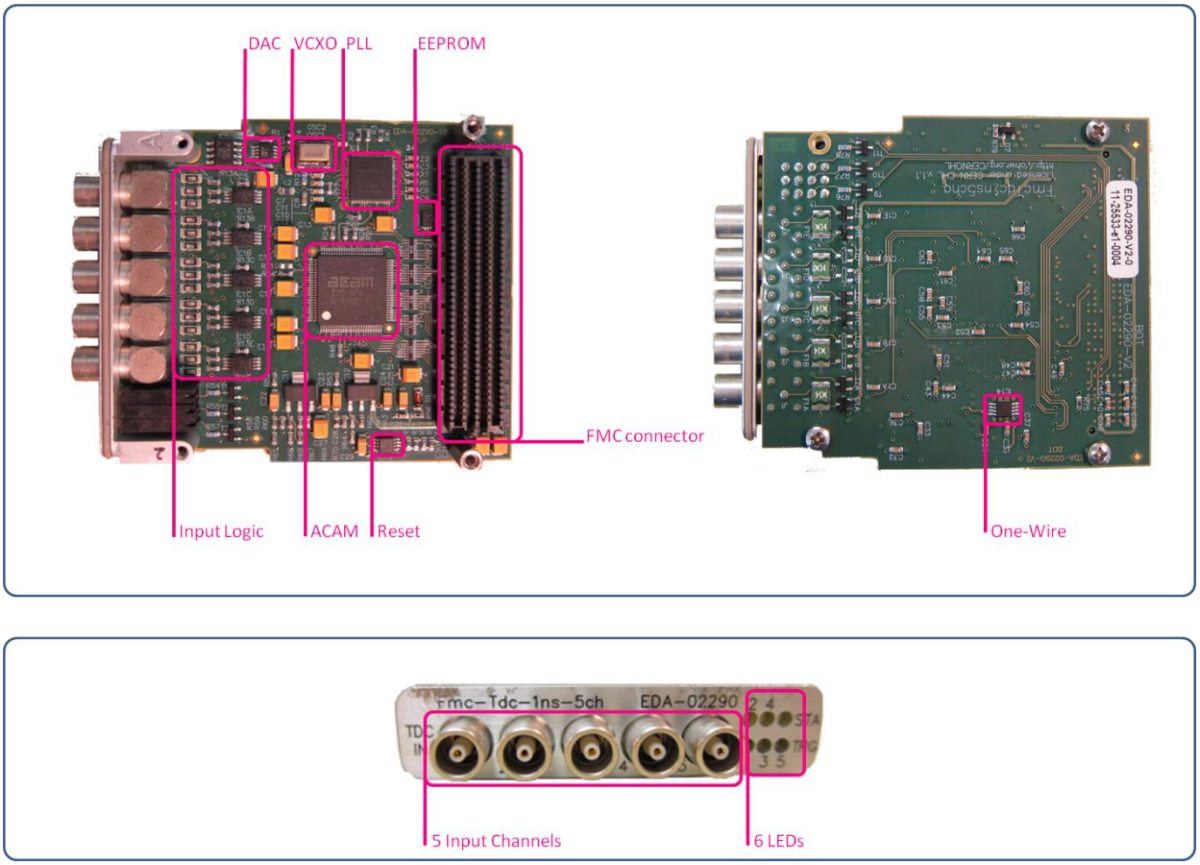


Figure 8: TDC main components

The TDC mezzanine board is tested while mounted on a SPEC carrier board. The SPEC provides FPGA logic, power supplies, memories, clocking resources and interface to the PCIe bus.

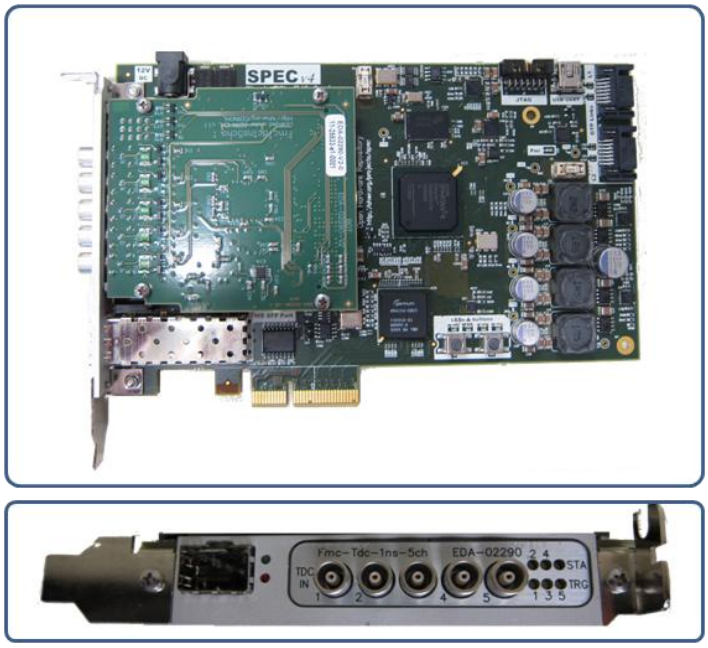


Figure 9: SPEC-TDC combination

PTS Software 3

The dedicated software running on the PTS computer provides the automated test environment.

The software automatically initiates a sequence of 13 tests. A TDC board is considered “PASSED” if it has successfully “PASSED” all the 13 tests. Each test verifies the functionality of different components and connections on the board. If a test fails the software continues with the following tests and the operator is informed at the end of all the failing parts. Table 2 lists the different tests.

Test	Short Description	Operator's Intervention
00	Mezzanine Presence	NO
01	Clocks	NO
02	Inputs to FPGA	NO
03	Inputs to FPGA Disable	NO
04	One Wire	NO
05	EEPROM	NO
06	ACAM Communication	NO
07	ACAM Timestamps	NO
08	Inputs to ACAM Disable	NO
09	ACAM Disable	NO
10	ACAM Errflag	NO
11	DAC	NO
12	LEDs	LEDs visual inspection when prompted

Table 2: List of tests

Log files retrieval 4

Log files holding all the information about the testing of a board are automatically generated and saved by the software at the location: **/home/user/pts/log_fmctdc1ns5cha**

For each test run, a .zip containing one file per test is created under the name: zip_run_<runid>_<timestamp>_FmcAdc100M14b4cha_<serial number>.zip.

Once the testing of all the boards has finished, the log files would need to be delivered to CERN. To do so, please follow the instructions:

- Plug a USB memory key on the computer
- Wait until Ubuntu mounts automatically the device and use the file explorer to navigate to /home/user/pts/log_fmctdc1ns5cha
- Select all the .zip files in this folder and copy them to the USB memory
- Use another computer with Internet access
- Send the files from the USB memory to the CERN responsible by email

First Time Setup 5

1) Make sure that the computer is switched off and plug the PCIe extender board into the computer slot indicated in Figure 10. Use the provided spacers and screws to mount the extender to the computer box.

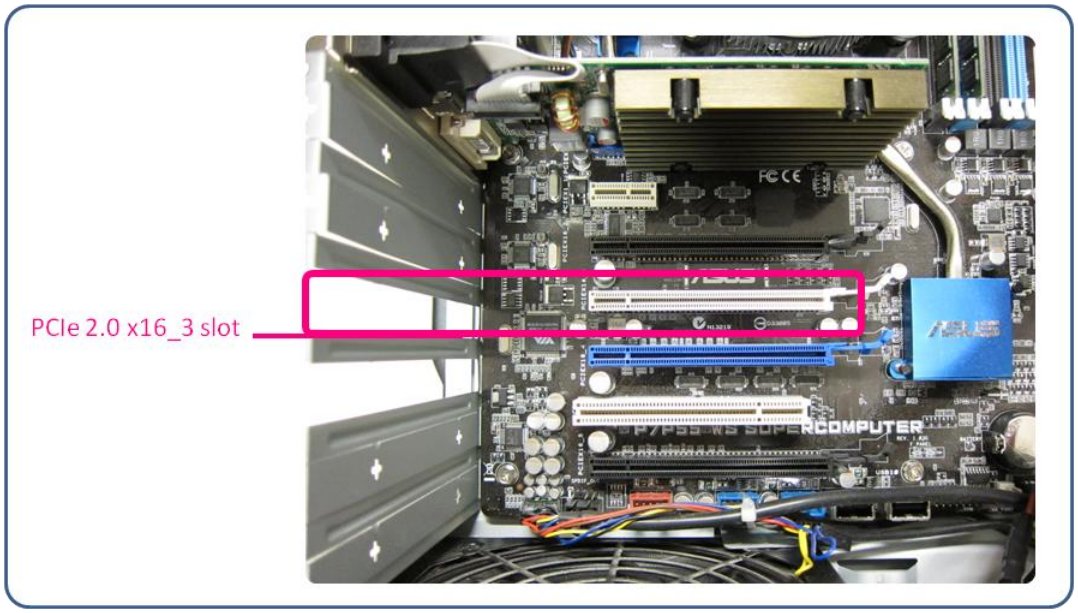


Figure 10: PCIe slot for extender

2) Plug the SPEC-Fine Delay combination into the computer slot indicated in Figure 11. Use the provided screws to mount it to the computer box.

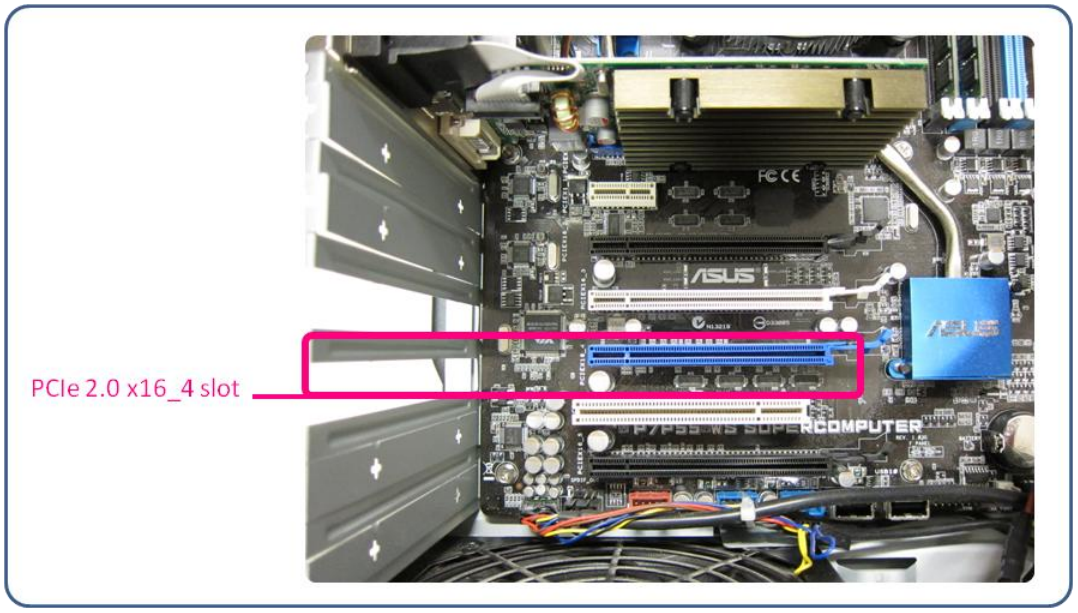


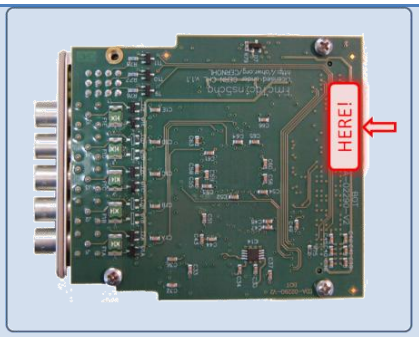
Figure 11: PCIe slot for SPEC-Fine Delay

3) Plug the barcode-reader into one available USB slot of the computer.
4) Connect the monitor, keyboard and mouse to the computer.
5) Plug the ESD strap in the yellow socket of the computer box.

Testing Procedure 6

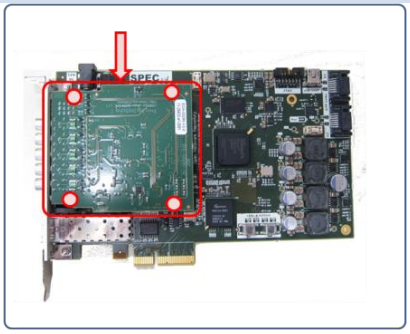
1) Place the **ESD strap** on your wrist.

2) Put the **barcode sticker** on the Bottom side of the TDC under test, in the position indicated in red.

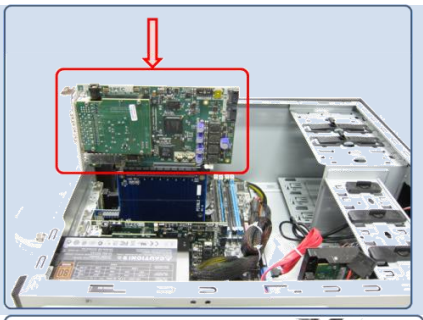


3) Mount the TDC board under test on the **SPEC board**.

   Fix using the provided **screws**.

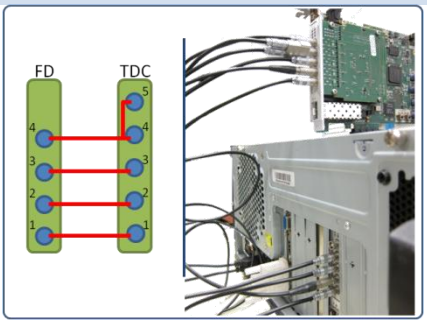


4) Plug the SPEC-TDC combination on the **extender board**.



5) Plug the **LEMO cables** between the four Fine Delay outputs and the five TDC inputs, as the figure shows.

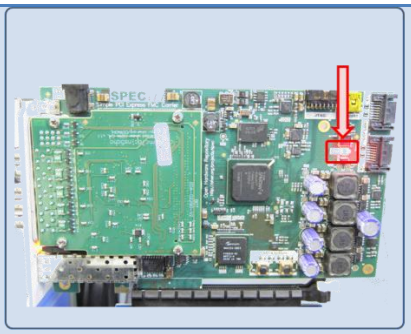
   Note that the TDC channels 4 and 5 are both connected to the Fine Delay channel 4.



6) Switch **ON** the **computer**.

Verify that the "Pwr" LED on the SPEC board is ON. This will confirm that the board is properly plugged.

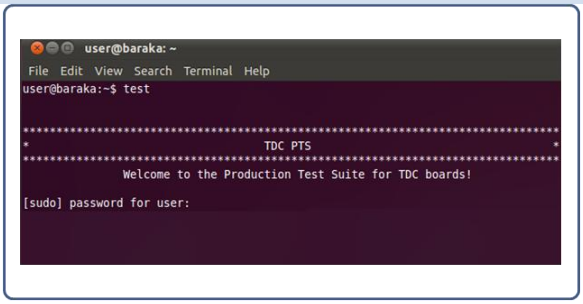
If the LED is OFF there is a problem with the power supply lines.



7) After the computer has finished with the booting procedure, a **terminal** appears automatically in the middle of the screen.

Type "**test**" and then [ENTER] to start the test program.

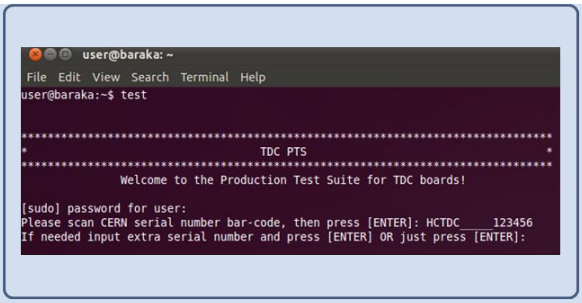
When asked, type the password: "**baraka**" and [ENTER]



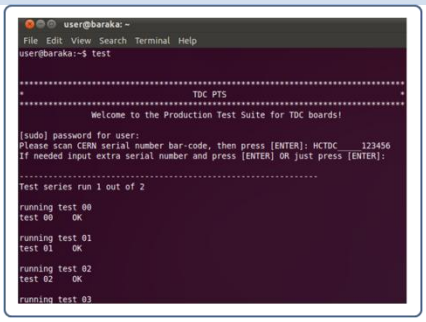
8) The program asks for the **barcode** of the board.

Check that the cursor is on the terminal,
press the barcode reader's button.
The code will appear on the terminal. Press [ENTER].

The program will ask for a second barcode, in case the manufacturer has a different serial number system.
Scan the second barcode and press [ENTER],
or if there is none, just press [ENTER].

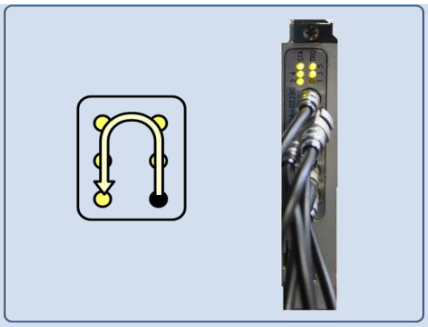


9) The program will automatically **execute tests 00 to 12**.

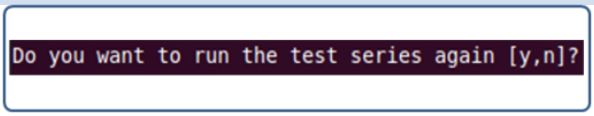


10) Test 12 requires the operator's intervention and will ask for a visual inspection of the TDC front panel **LEDs**.

As the picture shows the LEDs should be going OFF in a cyclic way, one at a time.



11) At the end the operator is informed of the **results** of all the tests and is asked if he wants to repeat the test.



If no error had occurred, type [n] and then [ENTER].

In case of error, you could repeat the tests once by typing [y] and [ENTER].

If you need to repeat the tests more than two times for one board, please report to the CERN responsible.

Common Causes of Test Failure 7

Once the testing has finished, all the errors that may have appeared are listed on the screen. The log files, located at **/home/user/pts/log_fmctdc1ns5cha** also hold all the details of the testing. The error messages are in principle self explanatory giving clear information on the failing component or connection, however for more insight information on the testing procedure and the common causes of failure you could consult the following sections.

Test 00: Mezzanine Presence test

Test of the presence of the mezzanine board, through the FMC signal PRSNT_M2C_N.

The following FMC signal is tested: PRSNT_M2C_N.

Possible reasons of failure:

- Bad soldering of the FMC connector
- Driver not properly installed
- Firmware not loaded

Test 01: Clocks test

Test of the PLL clocks: 31.25MHz FPGA_TDC_REF_CLK and 125MHz CLK125. The firmware loaded in the carrier FPGA starts by configuring the PLL IC4 through its SPI interface. In order to verify the clock frequencies, dedicated counters running at 200MHz are implemented in the FPGA.

The following components are tested: VXCO OSC1, PLL IC4.

The following FMC signals are tested: PLL_SCLK, PLL_SDI, PLL_SDO, PLL_CSN, STATUS, FPGA_TDC_REF_CLK_P, FPGA_TDC_REF_CLK_N, CLK125_P, CLK125_N.

Possible reasons of failure:

- Bad soldering of the FMC connector
- VCXO OSC1 defective
- PLL IC4 defective

Test 02: Inputs to FPGA test

Test of the TDC_IN_FPGA[5..1] signals. The test is using the Fine Delay board as pulse generator, sending pulses to each one of the TDC channels. In the firmware loaded on the carrier FPGA there are dedicated counters counting the duration of the received pulses.

The following FMC signals are tested: TDC_IN_FPGA[5..1], EN_INPUTS.

Possible reasons of failure:

- Bad soldering of the FMC connector
- Badly connected LEMO cables
- Input logic defective

Test 03: Disable Inputs to FPGA test

Test of the EN_INPUTS signal and its effect on the TDC_IN_FPGA[5..1] signals. The test is using the Fine Delay board as pulse generator, sending pulses to each one of the TDC channels. In the firmware loaded on the carrier FPGA there are dedicated counters counting the duration of the received pulses. When the EN_INPUTS signal is enabled pulses should be arriving to all the channels; when the EN_INPUTS is disabled no pulse should arrive.

The following components are tested: IC1A, IC1B, IC1C, IC1D, IC1E.

The following FMC signal is tested: EN_INPUTS (with respect to the TDC_IN_FPGA[5..1] signals).

Possible reasons of failure:

- Bad soldering of the FMC connector
- Badly connected LEMO cables
- Input logic defective

Test 04: One-Wire test

Test of the One-Wire thermometer with unique ID chip IC14. The test reads the serial unique ID and takes a temperature measurement of the board.

The following component is tested: IC14.

The following FMC signal is tested: g37.

Possible reasons of failure:

- Bad soldering of the FMC connector
- Pull-up R4 defective
- IC14 defective

Test 05: EEPROM test

Test of the I2C EEPROM chip IC5. The test starts by scanning the I2C bus and verifying that the EEPROM responds at the expected address. Then it writes data to the EEPROM and reads them back.

The following component is tested: IC5.

The following FMC signals are tested: SDA, SCL, GA0, GA1.

Possible reasons of failure:

- Bad soldering of the FMC connector
- IC5 defective

Test 06: ACAM Communication test

Test of the communication with the ACAM chip. The test is configuring the ACAM registers and then it is reading them back.

The following components are tested: IC8, PLL IC4, IC11, IC12.

The following FMC signals are tested: TDC_WRN, TDC_RDN, TDC_CSN, TDC_OEN, TDC_ADR[3..0], TDC_D[27..0].

The following board-internal signals are tested indirectly: RESET_N, TDC_REF_CLK

Possible reasons of failure:

- Bad soldering of the FMC connector
- ACAM IC8 defective

Test 07: ACAM Timestamps test

Test of the precision and accuracy of the ACAM timestamps. The test is using the Fine Delay board as pulse generator, sending several pulses to each one of the TDC channels. The firmware loaded on the carrier FPGA configures the ACAM chip and then retrieves and evaluates the generated timestamps.

The following component is tested: IC8.

The following FMC signals are tested: TDC_START_FPGA, TDC_INT, TDC_EMPTY_FLAG1, TDC_EMPTY_FLAG1

The following board-internal signals are tested indirectly: TDC_STOP[5..1]

Possible reasons of failure:

- Bad soldering of the FMC connector
- Badly connected LEMO cables
- Input logic defective
- ACAM IC8 defective

Test 08: ACAM Inputs Disable test

Test of the EN_INPUTS signal and its effect on the TDC_STOP[5..1] signals. The test is using the Fine Delay board as pulse generator, sending pulses to each one of the TDC channels. The firmware loaded on the carrier FPGA configures the ACAM and disables the EN_INPUTS signal. No timestamp should be registered by the ACAM.

The following components are tested: IC1A, IC1B, IC1C, IC1D, IC1E.

The following FMC signal is tested: EN_INPUTS (with respect to the TDC_STOP[5..1] signals)

Possible reasons of failure:

- Bad soldering of the FMC connector
- Badly connected LEMO cables
- Input logic defective
- ACAM IC8 defective

Test 09: ACAM Timestamps Disable test

Test of the TDC_START_DIS, TDC_STOP_DIS inputs to the ACAM chip. The Fine Delay board is used as pulse generator sending pulses to the five TDC channels. The test configures the ACAM and enables the TDC_START_DIS, TDC_STOP_DIS signals so as to prevent ACAM from registering pulses; the test confirms that no pulse is being registered.

The following component is tested: IC8.

The following FMC signals are tested: TDC_START_DIS, TDC_STOP_DIS.

Possible reasons of failure:

- Bad soldering of the FMC connector
- Input logic defective
- ACAM IC8 defective

Test 10: ACAM ErrFlag test

Test of the TDC_ERR output of the ACAM chip. The test configures the ACAM so that the Errflag is activated upon overflow on the interface FIFOs; an overflow occurs when the timestamps arrival rate is higher than 31.25MHz. The test is using the Fine Delay as pulse generator sending pulses to the five TDC channels with a total rate of 100MHz and is monitoring the TDC_ERR signal.

The following component is tested: IC8.

The following FMC signal is tested: TDC_ERR.

Possible reasons of failure:

- Bad soldering of the FMC connector
- Badly connected LEMO cables
- Input logic defective
- ACAM IC8 defective

Test 11: DAC test

Test of the DAC IC2. The test is using the Fine Delay board as pulse generator, sending 1 Hz pulses to TDC channel 1. The firmware loaded on the carrier FPGA configures the ACAM; it then configures the DAC. Two values are given to the DAC: first a low one (0V: 0x0000) and then a higher one (1.6V: 0xAA57). The ACAM timestamps are retrieved and evaluated: the pulse duration is expected to be higher when the DAC value is high and lower when the DAC value is low.

The following component is tested: DAC IC2

The following components are tested indirectly: VCXO OSC1, IC1, PLL IC4

Possible reasons of failure:

- DAC IC2 defective
- VCXO OSC1 defective
- IC1 defective
- Badly connected LEMO cable for Channel 1

Test 12: LEDs test

Test of the front panel LEDs. For this test the operator's intervention is needed; when prompted, the operator should visually inspect the LEDs. The FPGA forces a sequential blinking of the LEDs in orange color.

The following component is tested: front panel LEDs

The following FMC signals are tested: LED_TRIG[5..1], STATUS_LED

Possible reasons of failure:

- Bad soldering of the FMC connector
- T1, T2, T3, T9, T10, T11 defective
- LD1A, LD1B, LD3A, LD3B, LD3A, LD3B defective
- R54, R55, R57, R76, R77, R78 defective

Untested components and signals:

The following signals are not tested by the PTS:

- TERM_EN[5..1] (would require additional testing equipment)
- ALU_TRIGGER (used on different operational modes of the ACAM)
- TDC_START (not used, TDC_START_FPGA used instead)

The ACAM IC8 is tested only in I mode.

The functionality of the voltage supervisor IC13 is not tested thoroughly; in principle the voltages are within limits and the RESET_N is inactive.

| TDC PTS realized by | Evangelia Gousiou | Matthieu Cattin | Tomasz Wlostowski |
| Benjamin Ninet |Erik Van der Bij |